

DATA SHEET

BLS2731-50 Microwave power transistor

Product specification
Supersedes data of 1997 Nov 05

1998 Jan 30

Microwave power transistor

BLS2731-50

FEATURES

- Suitable for short and medium pulse applications
- Internal input and output matching networks for an easy circuit design
- Emitter ballasting resistors improve ruggedness
- Gold metallization ensures excellent reliability
- Interdigitated emitter-base structure provides high emitter efficiency
- Multicell geometry improves power sharing and reduces thermal resistance.

APPLICATIONS

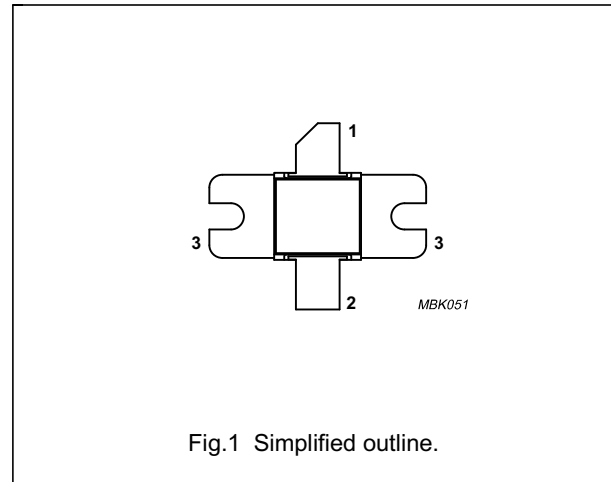
- Common base class-C pulsed power amplifiers for radar applications in the 2.7 to 3.1 GHz band.

DESCRIPTION

NPN silicon planar epitaxial microwave power transistor in a 2-lead rectangular flange package with a ceramic cap (SOT422A) with the common base connected to the flange.

PINNING - SOT422A

PIN	DESCRIPTION
1	collector
2	emitter
3	base; connected to flange



QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^\circ\text{C}$ in a common base class-C test circuit.

MODE OF OPERATION	f (GHz)	V_{CB} (V)	P_L (W)	G_p (dB)	η_c (%)
Pulsed, class-C	2.7 to 3.1	40	60	typ. 9	typ. 40

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	75	V
V_{CES}	collector-emitter voltage	$R_{BE} = 0$	–	75	V
V_{EBO}	emitter-base voltage	open collector	–	2	V
I_{CM}	peak collector current	$t_p \leq 100 \mu\text{s}$; $\delta \leq 10\%$	–	6	A
P_{tot}	total power dissipation	$t_p = 100 \mu\text{s}$; $\delta = 10\%$; $T_{mb} = 25 \text{ }^\circ\text{C}$	–	80	W
T_{stg}	storage temperature		–65	+200	$^\circ\text{C}$
T_j	operating junction temperature		–	200	$^\circ\text{C}$
T_{sld}	soldering temperature	up to 0.2 mm from ceramic cap; $t \leq 10 \text{ s}$	–	235	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j-h}$	thermal impedance from junction to heatsink	$t_p = 100 \mu\text{s}$; $\delta = 10\%$; note 1	0.3	K/W

Note

1. Equivalent thermal impedance under pulsed microwave operating conditions.

CHARACTERISTICS

 $T_j = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 15 \text{ mA}$; open emitter	75	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 15 \text{ mA}$; $V_{BE} = 0$	75	–	–	V
I_{CBO}	collector leakage current	$V_{CB} = 40 \text{ V}$; $I_E = 0$	–	–	1.5	mA
I_{CES}	collector leakage current	$V_{CE} = 40 \text{ V}$; $V_{BE} = 0$	–	–	3	mA
I_{EBO}	emitter leakage current	$V_{EB} = 1.5 \text{ V}$; $I_C = 0$	–	–	0.3	mA
h_{FE}	DC current gain	$V_{CB} = 5 \text{ V}$; $I_C = 1.5 \text{ A}$	40	–	–	
C_c	collector capacitance (die only)	$V_{CE} = 1 \text{ V}$; $I_E = i_e = 0$; $f = 1 \text{ MHz}$	–	30	–	pF

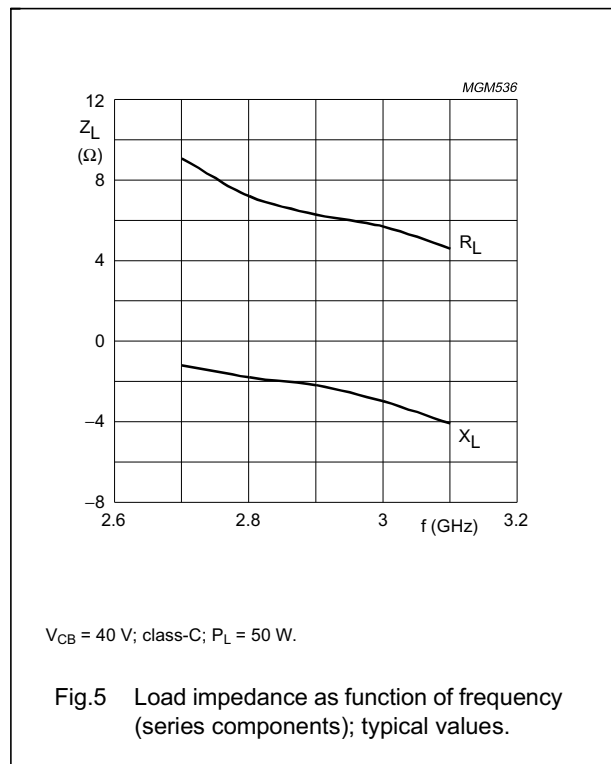
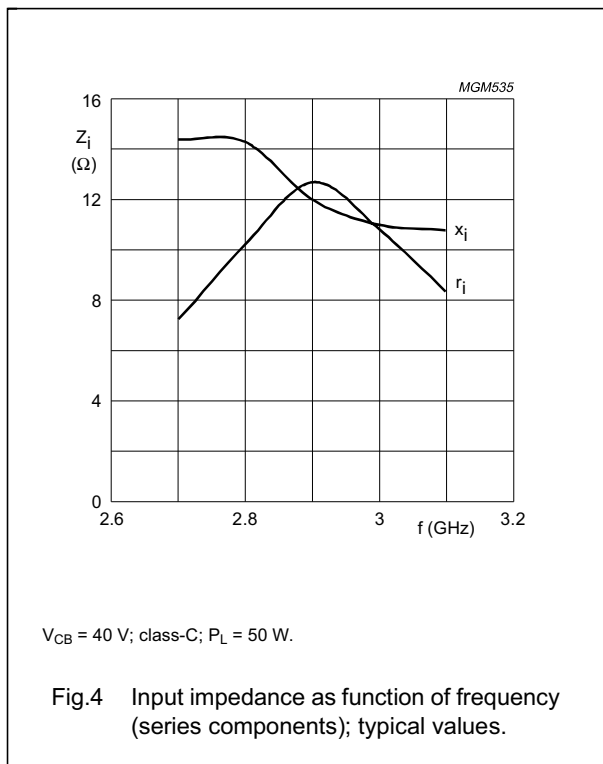
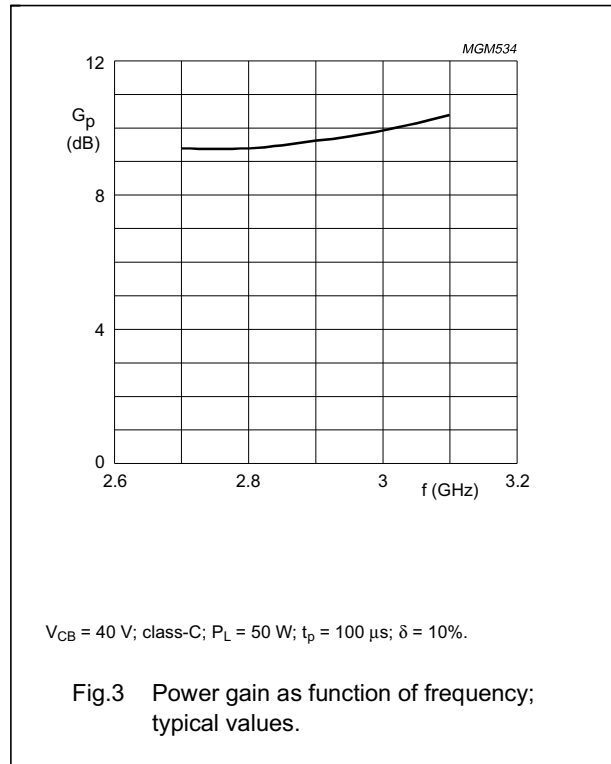
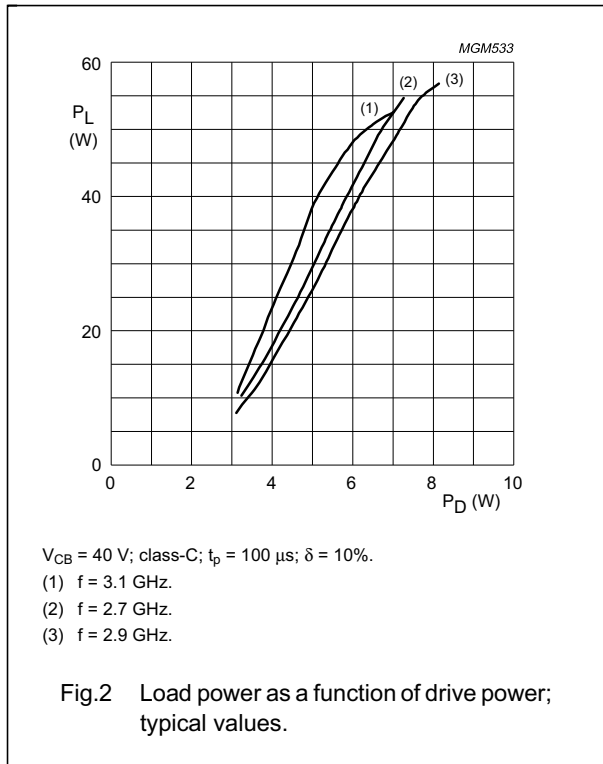
APPLICATION INFORMATION

RF performance at $T_n = 25 \text{ }^\circ\text{C}$ in a common-base test circuit.

MODE OF OPERATION	f (GHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)
Class-C; $t_p = 100 \mu\text{s}$; $\delta = 10\%$	2.7 to 3.1	40	≥ 50 typ. 60	≥ 8 typ. 9	≥ 35 typ. 40

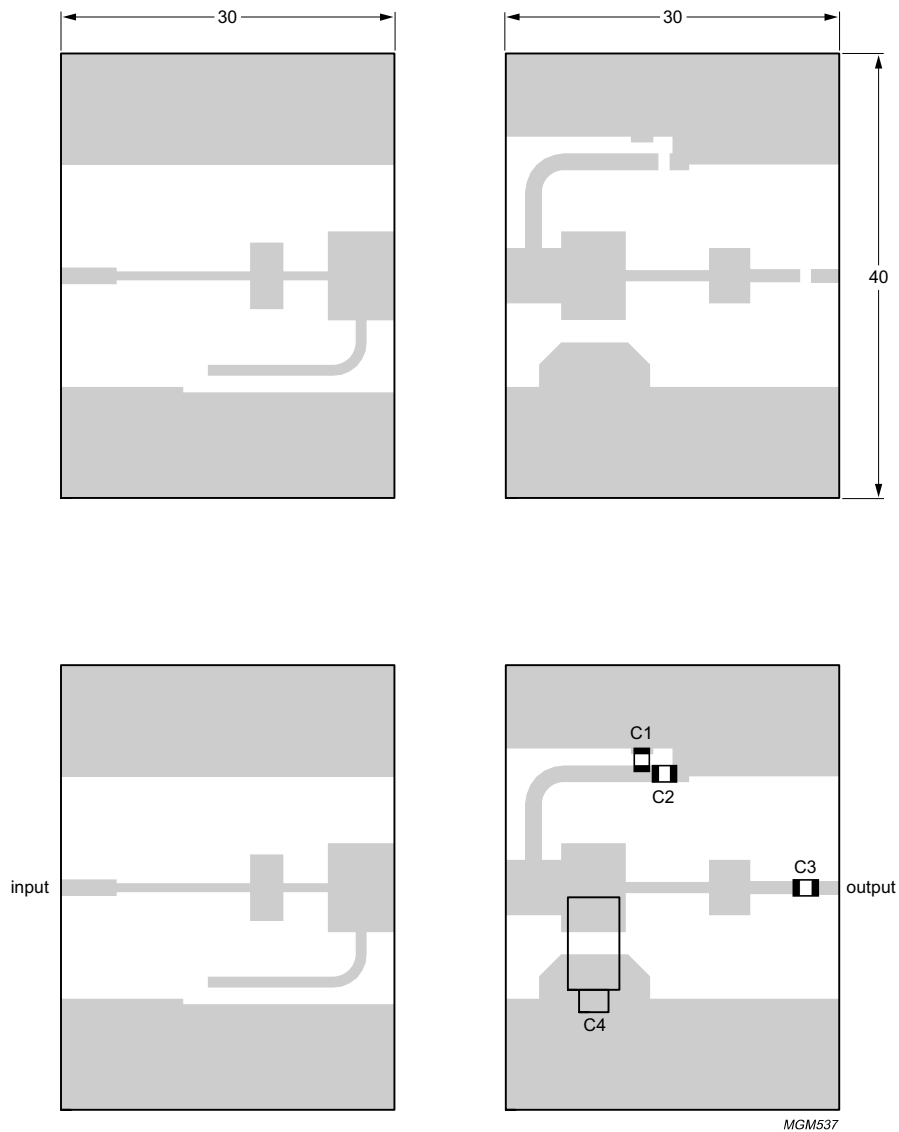
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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Duroid dielectric ($\epsilon_r = 2.2$), thickness 0.38 mm. The other side is unetched and serves as a ground plane.

C1 = ATC 200A 10 nF

C2 = ATC 100A 10 pF

C3 = ATC 700A 150 pF

C4 = Tekelec trimmer 37281SL 0.4 to 2.5 pF.

Fig.6 Component layout for 2.7 to 3.1 GHz class-C test circuit.

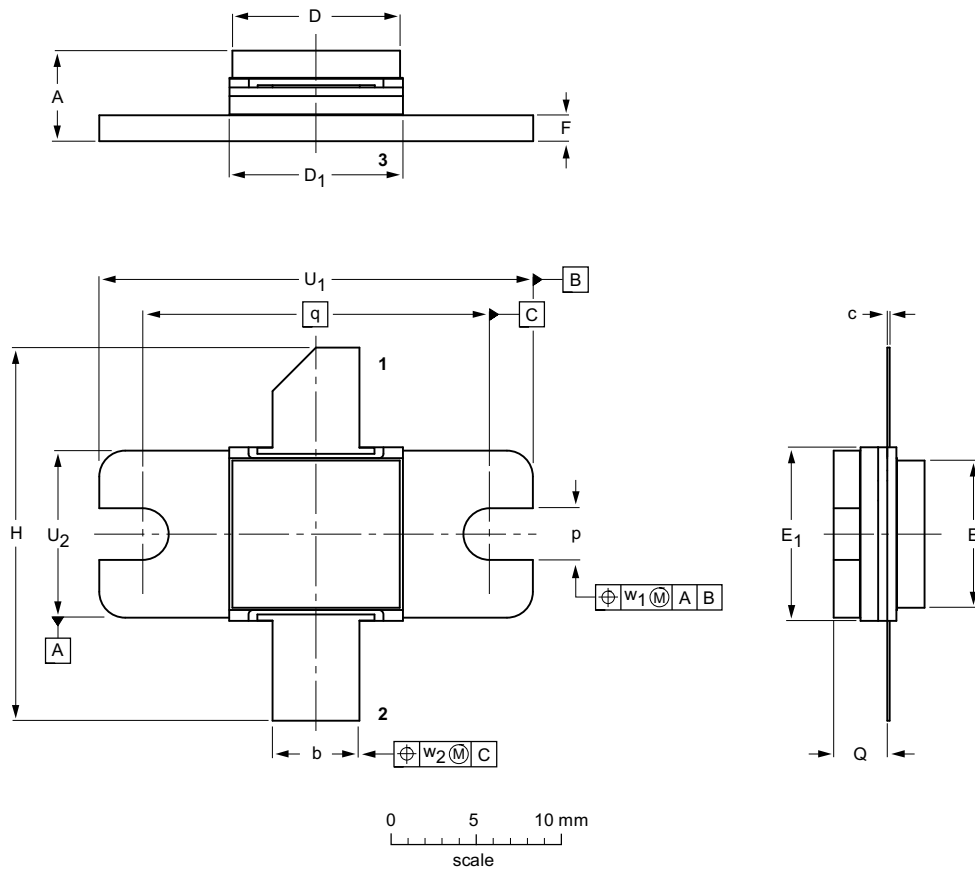
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PACKAGE OUTLINE

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT422A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	5.72 4.83	5.21 4.95	0.13 0.08	9.93 9.68	10.29 10.03	8.76 8.51	10.29 10.03	1.58 1.47	21.61 21.08	3.43 3.18	3.35 2.92	16.51	22.99 22.73	9.91 9.65	0.25	0.76
inches	0.225 0.190	0.205 0.195	0.005 0.003	0.391 0.381	0.405 0.395	0.345 0.335	0.405 0.395	0.062 0.058	0.89 0.83	0.135 0.125	0.132 0.115	0.65	0.905 0.895	0.390 0.380	0.01	0.03

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT422A						97-12-24

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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