Using the TPS51100

User's Guide

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TEXAS INSTRUMENTS

Using the TPS51100

The TPS51100EVM evaluation module (EVM) includes an LDO for DDRI and DDRII memory modules with the necessary termination and reference voltages for DDR Memory modules. The EVM is designed to use a 1.5-V to 3.4-V VDDQ voltage and a 4.75 V to 5.25 V controller core supply to generate the necessary ½ VDDQ termination voltage with ± 2-A of sink/source current capacity for dual data rate (DDR) memory modules.

The TPS51100EVM allows the user to evaluate the TPS51100 using an external reference voltage or the VDDQ LDO supply voltage to test it with DDRI or DDRII voltage standards and the S3 and S5 sleep states.

1 Description

The TPS51100 is designed to provide proper termination voltage for DDR memory modules covering both the DDRI (2.5 V/1.25 V) and DDR2 (1.8 V/0.9 V) specifications with minimal external components. The high-speed LDO allows designs with fewer and smaller external capacitors, reducing the size and cost of the dual data rate memory power solution. With the addition of an external regulator to generate the necessary core and I/O voltage for the memory module, the TPS51100 provides both the termination voltage and a 10-mA buffered reference voltage necessary to complete the DDRI or DDRII memory power supply solution.

1.1 Applications

- Dual data rate (DDR) high-speed RAM termination
- High performance AGP video cards
- Notebook, desktop and sever motherboards
- High performance computer
- High memory content consumer electronics

1.2 Features

- High-speed LDO requires only 20-μF (2 × 10-μF) VTT capacitance
- LDO output for DDR termination and buffered reference voltages
- ± 2-A sink/source termination voltage LDO regulator
- 10-mA termination reference voltage for DDR input reference
- User selectable VDDQ or externally referenced supply voltages
- Switches available for testing S3 and S5 sleep states

2 Electrical Performance Specifications

Table 1. Electrical Performance Specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{V5IN}	Supply voltage		4.75		5.25	V
V_{VDDQ}	LDO supply voltage		1.5		3.4	
V_{VTT}	Termination voltage	$V_{VDDQSNS}$= V_{VDDQ}		V_{VDDQ}/2		
$V_{VTT(tol)}$	Termination voltage tolerance		-40		40	mV
$V_{VTT(RIPPLp-p)}$	Termination voltage ripple (1)		0		20	
I_{VTT}	Termination current	$V_{VIN\ LDO}$= V_{VDDQ}	-2		2	A
$V_{Vtt\_ref(tol)}$	Reference voltage tolerance	I_{Vtt_ref} < 10 mA	-10		10	mV
I_{Vtt_ref}	Reference current				10	mA

(1) VTT output tracks theripple voltage on VDDQSNS input per DDR specification.

3 Schematic

The TPS51100EVM schematic is shown in Figure 1.

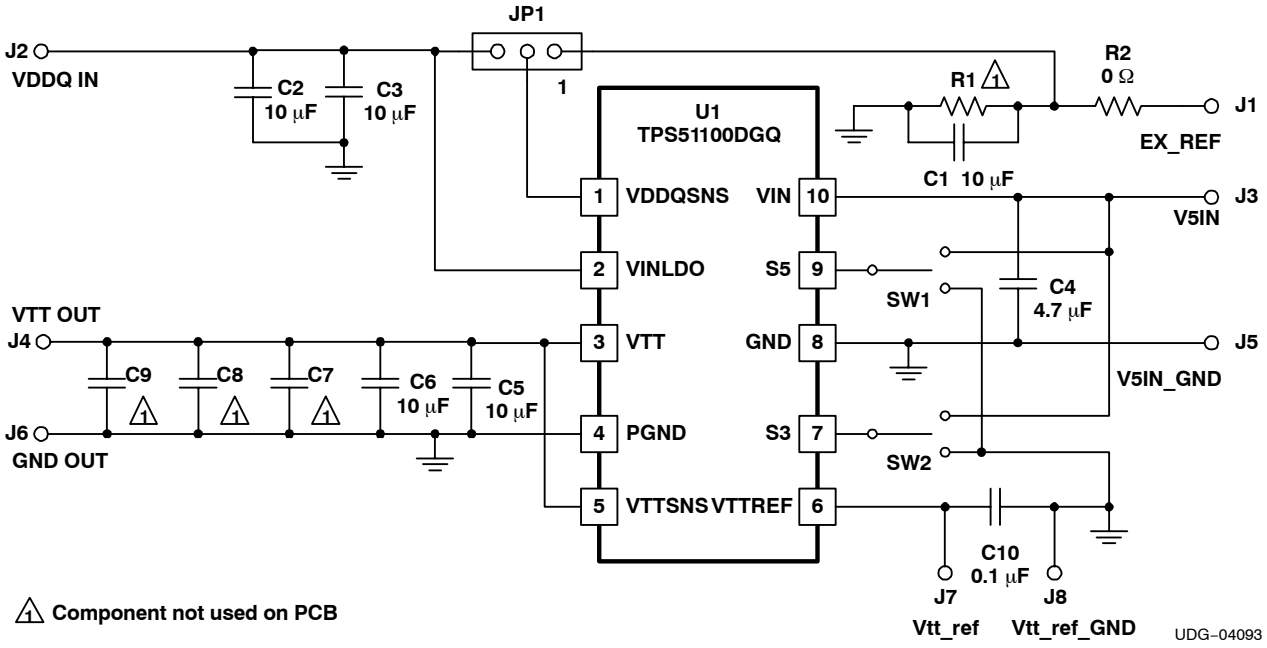

Figure 1. TPS51100EVM Schematic

3.1 JP1 Jumper

A Standard 100 mil spacing header (JP1) provides the user the ability to select either the VDDQ voltage or an external reference voltage for the TPS51100's VDDQSNS voltage. The TPS51100 produces a termination voltage and buffered reference voltage equal to ½ this VDDQSNS voltage. This allows the user to evaluate the TPS51100 under a variety of conditions. The TPS51100EVM should not be operated when this jumper is not in place and the EVM should be powered down prior to changing the jumper position.

3.2 Sleep State Switches

Switches SW1 and SW2 select the S5 and S3 sleep states respectively allowing the user to examine the reaction of the TPS51100 controller to these memory sleep states.

3.3 Resistors R1 and R2

Resistors R1 and R2 allow the user to provide a divided reference voltage to the VDDQSNS pin of the TPS51100. If a divided external reference voltage is desired, replace R1 and R2 with the desired resistor ratio. C1 provides some filtering to keep noise from coupling through the TPS51100, which will attempt to track any noise on the VDDQSNS voltage.

3.4 User Selectable Configuration Modes

Figure 2 shows the location of the jumper block and two switches used to adjust the configuration of TPS51100EVM. The jumper allows the user to select either an external reference voltage or the VDDQ voltage for the TPS51100's sense voltage for the VTT and VTT_REF voltages. In either case, VDDQ must be between 1.5 V and 3.4 V to provide the LDO source voltage for the TPS51100.

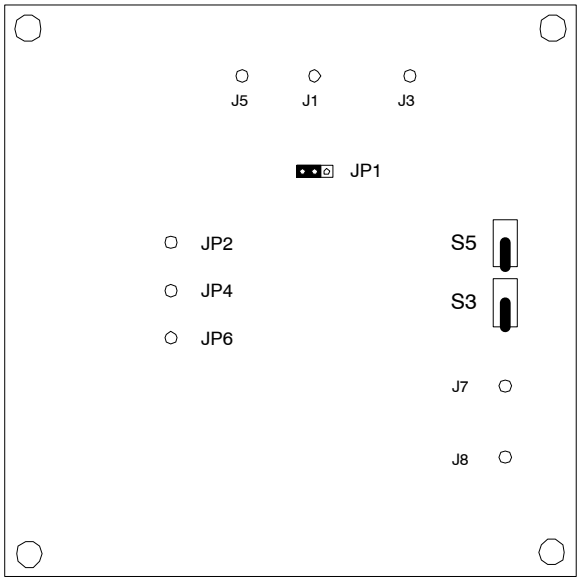

Figure 2. TPS51100EVM Jumper Location and Default Position

3.4.1 JP1 VDDQ Reference Voltage

The TPS51100EVM ships preconfigured to use the VDDQ input voltage as both the LDOIN and VDDQSNS voltage for the TPS51100. In this configuration, the outputs VTT andVTTREF is ½ the VDDQ voltage. This is the most common configuration for the TPS51100 as the DDRI/DDRII specifications require the termination voltage be ½ the core and I/O (VDDQ) voltages. To configure the TPS51100EVM for VDDQ reference voltage, set JP1 jumper in the left horizontal position.

3.4.2 JP1 External Reference Voltage

The TPS51100EVM can be configured to use an external reference voltage (EX_REF) to generate the VTT and VTTREF termination and buffered reference voltages. This allows the user to evaluate the TPS51100 under a variety of conditions or adjust the output voltage with an external system. Even in this configuration, VDDQ must be connected to provide the LDOIN source voltage and current. To configure the TPS51100EVM for external reference voltage, set the JP1 jumper in the right horizontal position.

4 Test Set-Up

Figure 3 shows the basic test set up recommended to evaluate the TPS51100EVM. Please note that although all grounds are common, their connections should remain separate as noted in.

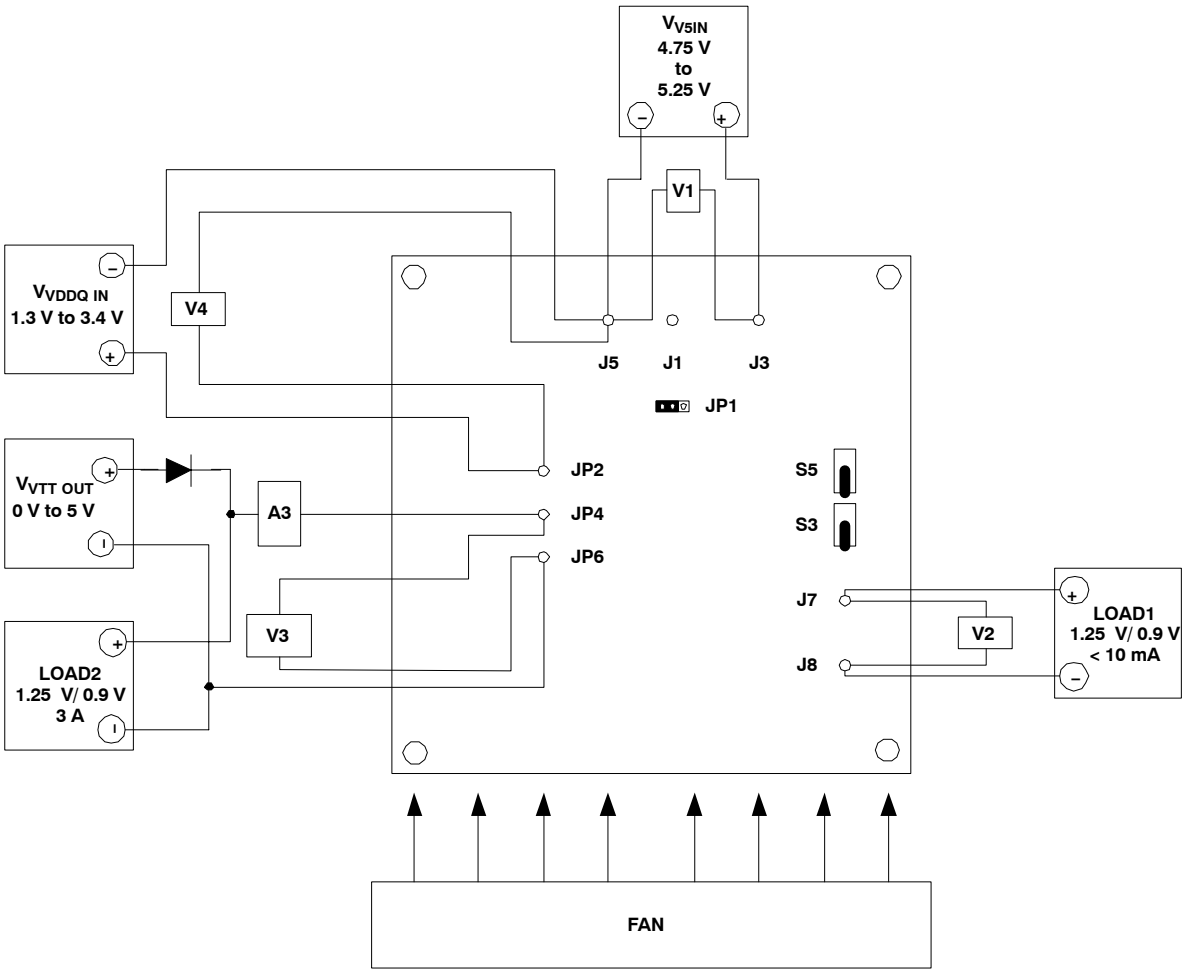

Figure 3. TPS51100EVM Recommended Test Set-Up

4.1 5-V DC Source (V_{V5IN})

V_{V5IN} should be a DC voltage source capable of delivering 5 V at 500 mA with a power handling capability of at least 2.5 W. V_{V5IN} should be connected between pins V5IN and V5IN_GND. V_{V5IN} supplies the TPS51100 operating current and powers the S3 and S5 sleep state switches.

4.2 Core Voltage Source ($V_{VDDQ\ IN}$)

$V_{VDDQ\ IN}$ is a DC voltage source capable of delivering 1.5 VDC to 3.4 VDC at 3.5 ADC with a power handling capability of at least 12 W. $V_{VDDQ\ IN}$ should be connected to between pins VDDQ IN and V5IN GND. $V_{VDDQ\ IN}$ supplies the source current for VLDOIN and the VDDQSNS reference voltage for the TPS51100.

4.3 Termination Voltage Source ($V_{VTT\ OUT}$)

$V_{VTT\ OUT}$ source is used to test the sink capability of the VTT pin. $V_{TT\ OUT}$ must be able to source 3 A of current at 5 V. A blocking diode should be placed in series with $V_{VTT\ OUT}$ to limit the sink current and prevent reverse current into $V_{VTT\ OUT}$. $V_{VTT\ OUT}$ should be connected between pins VTT OUT and GND OUT. $V_{VTT\ OUT}$ and LOAD2 should never be on at the same time.

4.4 Memory Cell Reference Voltage Load (LOAD1)

LOAD1 is an electronic or resistive load sinking less than 10 mA from the VTTREF pin voltage of 1.25 V (DDRI Mode) or 0.9 V (DDRII Mode). LOAD1 should be connected between pins Vtt_Ref and Vtt_Ref_GND

4.5 Termination Voltage Load (LOAD2)

LOAD2 is an electronic load set in constant current mode capable of sinking 0 A to 3 A of current at 1.25 V (DDRI Mode) or 0.9 V (DDRII Mode). LOAD2 needs to be connected between pins VTT OUT and GND OUT. LOAD2 and $V_{VTT\ OUT}$ should never be on at the same time.

4.6 Fan

Most power converters include components that can get hot to the touch when operating, approaching temperatures of 60°C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 LFM is recommended to reduce component temperatures when operating the evaluation module.

4.7 Power Up/Power Down Procedure

The following test procedure is recommended primarily for power up and shutting down the EVM. Whenever the EVM is running, the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Connect power supplies, loads, voltage meters and current meters as shown in Figure 1.
3. Set 100mil shunt jumper as described in User Configuration Jumper Settings for desired operational configuration. (Note: Do not attempt to change jumper settings during operation)
4. Increase V_{VDDQ} from 0 V to 1.8 or 2.4V DC. Using V4, verify V_{VDDQ} voltage between 1.5 and 3.4V.
5. Increase V_{V5IN} from 0 V to 5.0 VDC. Using V1, verify V_{V5IN} voltage between 4.75 V and 5.25 V.
6. Vary $V_{VTT\ OUT}$ for A3 from 0 A to -2 A. (Note: Do not run both $V_{VTT\ OUT}$ and LOAD2 at the same time)
7. Set $V_{VTT\ OUT}$ to 0 V and disconnect.
8. Vary LOAD2 for A3 from 0 A to 2 A. (Note: Do not run both $V_{VTT\ OUT}$ and LOAD2 at the same time)
9. Vary LOAD1 from 0 mA to 10 mA. (Note: Do not exceed 10 mA on LOAD1)
10. Vary $V_{VDDQ\ IN}$ from 1.5 V to 3.4 V
11. Vary V_{V5IN} from 4.75 V to 5.25 V
12. Use state S3 and state S5 switches to test sleep states.
13. Decrease LOAD1 to 0 mA.
14. Decrease LOAD2 to 0 A.
15. Decrease V_{V5IN} to 0 V.
16. Decrease $V_{VDDQ\ IN}$ to 0 V.

5 EVM Assembly Drawing and Layout

TPS51100 is built on a double sided copper clad FR4 PCB 3.0”× 3.0” and 0.062 thick. Figure 4 through Figure 7 detail the PCB assembly, silk screen and copper layers for TPS51100EVM. These figures are provided for reference and evaluation purposes only.

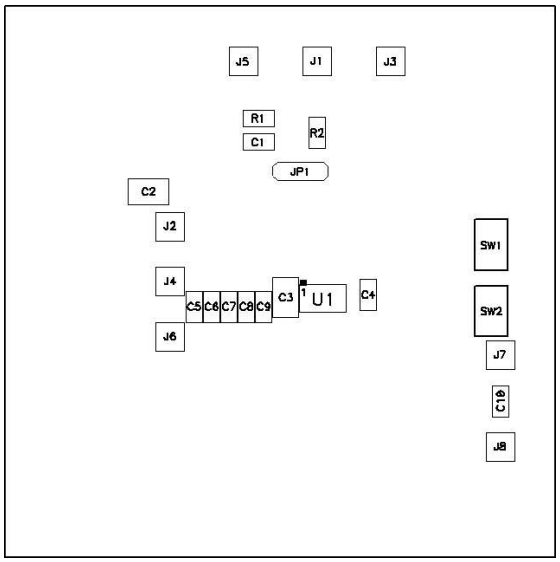

Figure 4. Top Side Component Output (Top View)

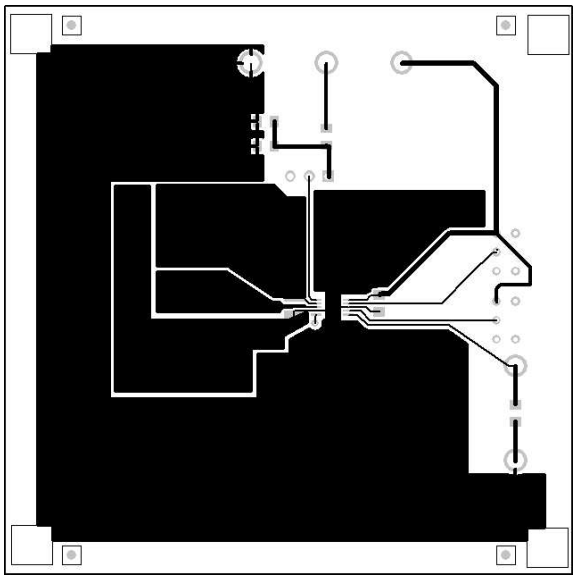

Figure 6. Top Copper Layer (Top View)

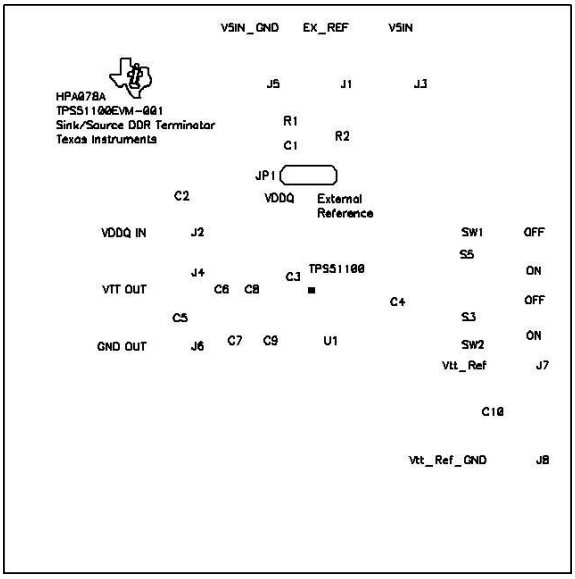

Figure 5. Top Silk Screen (Top View)

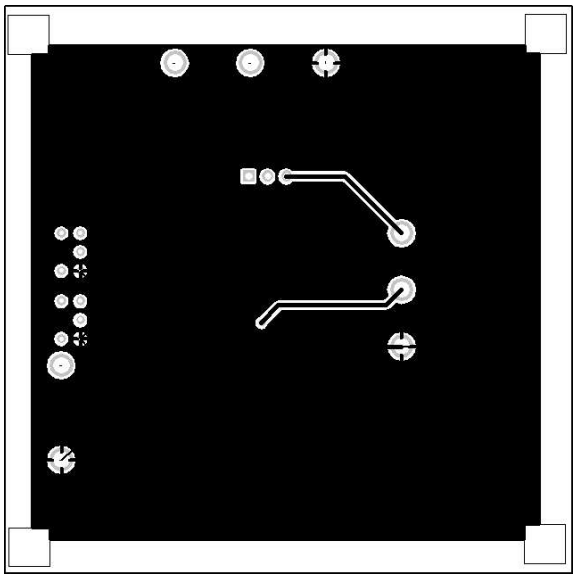

Figure 7. Bottom Copper Layer (Bottom View)

6 List of Materials

Table 2. List of Materials

QTY	REFERNCE DESIGNATOR	DESCRIPTION	SIZE	MRF	PART NUMBER
3	C1, C5, C6	Capacitor, ceramic, 10 μF, 6.3 V, X5R, 10%	805	TDK	C2012X5R0J106K
2	C2, C3	Capacitor, ceramic, 10 μF, 6.3 V, X5R, 10%	1210	TDK	C3225X7R1C106M
1	C4	Capacitor, ceramic, 4.7 μF, 6.3-V, X5R, 10%	805	TDK	C2012X5R0J475K
0	C7, C8, C9	Capacitor, ceramic, X5R, 6.3V	805		
1	C10	Capacitor, ceramic, 0.1 μF, 50 V, X7R, 10%	805	TDK	C2012X7R1H104K
8	J1, J2, J3, J4, J5, J6, J7, J8	Header, single pin	0.125 × 1	Keystone Electronics	1573-2
1	JP1	Header, 3-pin, 100 mil spacing	0.1 × 0.3	Sullins	PTC36SAAN
0	R1	Resistor, chip, 1/10W, 1%	805		
1	R2	Resistor, chip, 0 Ohms, 1/10-W, 1%	805	Std	Std
2	SW1, SW2	Switch, ON-ON Mini Toggle	0.28 × 0.18	NKK	G12AP
1	U1	IC, High Performance DDRI&II 3A LDO & Buffered Reference	HTTSOP-10	TI	TPS51100DGQ
1		PCB, 2-layer FR4, 3.0" x 3.0" 0.063thk	2.25 × 3.20	Any	HPA078A
1		Shunt, 100 mil jumper	0.1 × 0.2	Sullins	PJ-19-2-0
4		Bumpon, Transparent	0.44 × 0.2	3M	SJ5303

FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.5 V to 3.4 V and 4.75 V to 5.25 V and the output voltage range of 0.75 V to 1.70 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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