FURUNO GNSS Receiver

Model GT-88

Hardware Specifications

(Document No. SE19-410-004-00)

FURUNO ELECTRIC CO., LTD.

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- Galileo(Europe)
- QZSS(Japan)
- SBAS(USA: WAAS, Europe: EGNOS, Japan: MSAS)

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We pay through attention about the software of this product. But, if perchance you found a bug or a trouble, please feel free to contact us directly. We will check it, and if it is a bug, we may send you a new version with a bug fix. If perchance we found a bug or a trouble, we may send you a new version after we contact you.

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Revision History

Version	Change contents	Date
0	Initial release	2019.04.18

Table of Contents

1 Outline

This document describes hardware specifications of GT-88 which is the FURUNO Multi-GNSS timing receiver. This document uses GNSS as general term of GPS, GLONASS, Galileo and QZSS.

2 Function overview

This product is a stand-alone, complete GNSS timing receiver module that can provide accurate PPS signal with GNSS PVT (Position, Velocity & Time) information through serial communication channel. The key device inside is *eRide*OPUS 7, the latest monolithic GNSS receiver chip that contains ARM9™ processor for signal tracking and processing, high performance integrated LNA, PLL Synthesizer, Down-converter, ADC and DSP. This product also contains Flash ROM for firmware and data storage, TCXO for reference clock, 32 kHz crystal for RTC (Real time clock), L1 band SAW filter and power-on reset circuit.

The block diagram is shown in figure 2-1.

PPS pin provides accurate timing pulse which is synchronized to UTC (GPS) time system. The frequency of PPS signal is configurable by commands through serial communication channel (RXD1). Also GCLK pin provides clock output synchronized to PPS. The frequency of GCLK is configured by serial command from 10 Hz up to 40 MHz with 1 Hz step, and the rising edge of PPS pulse is synchronized to GCLK rising.

FLNA pin has a special function to configure LNA gain. In case this pin is connected to VCC, internal LNA is set to low gain mode. And in case of no connection (open), high gain mode is selected. So for active antenna, this pin should be connected to VCC, and for passive antenna open.

ANT_DET0/ANT_DET1 pins are used to feed the status of active antenna connection to ARM™ subsystem from the antenna current detection circuit placed outside of this product. These signals can show three (3) states of antenna connection; normal, open (low current) and short (high current). For details, please refer “User's Design Guide (SE13-900-001)”.

Reserved pins have pull-up or pull-down resistors inside adequately, so please do not connect anything.

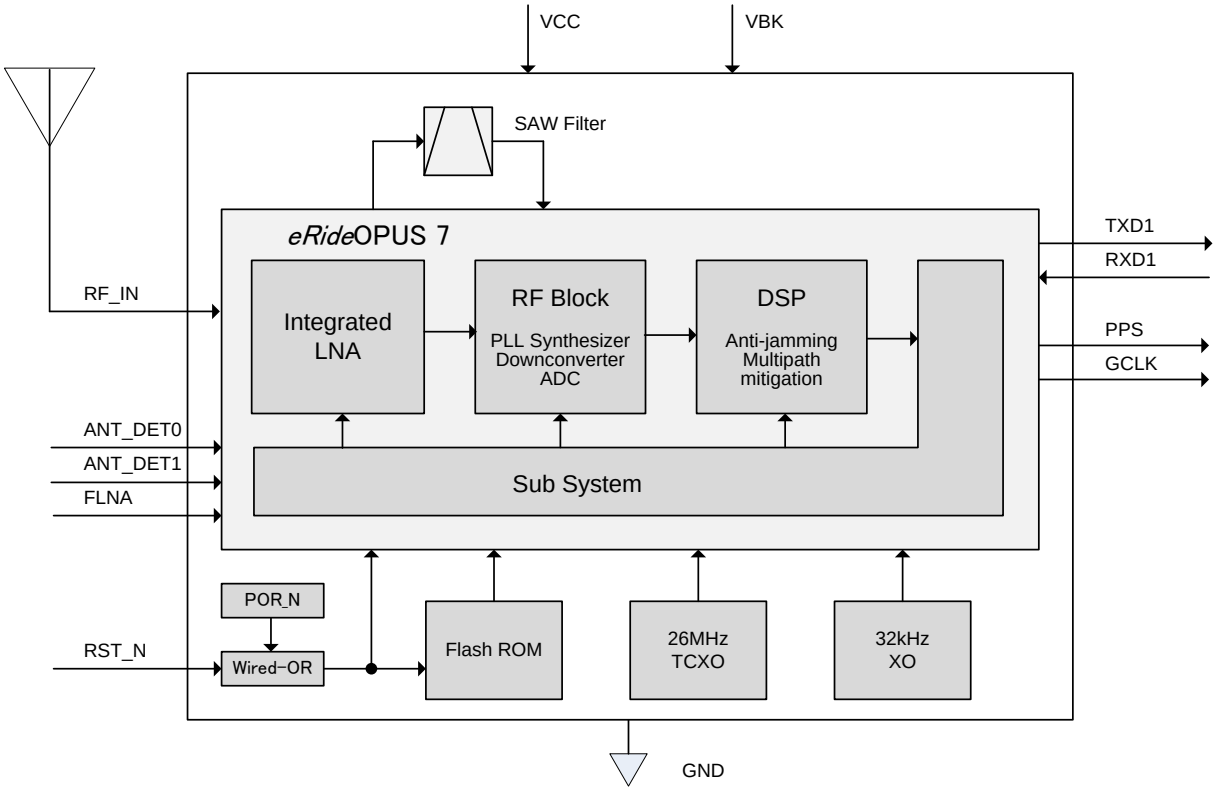


Figure 2-1. Block Diagram

3 GNSS General Performance

The below is a specification on GNSS general performance.

The performance described in this chapter is measured and evaluated under the environment shown in Figure 3-1. In addition, the measurement conditions are the default setting, 25 degree constant. When signal level masking is done by command, it is limited by that mask.

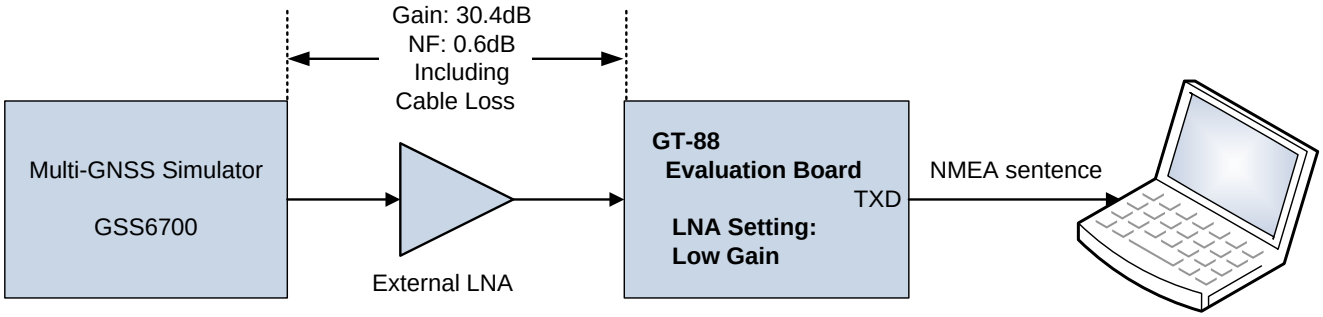


Figure 3-1. Measurement Platform

Table 3-1. Time To First Fix (TTFF)

Item	Specification	Note
TTFF (HOT)	< 5 sec	[*1] [*2]
TTFF (COLD)	< 35 sec	[*1] [*3]

Table 3-2. GPS performance

Item	Specification	Note
Signal type	GPS L1C/A	
Channel	MAX 12	[*4]
HOT acquisition sensitivity	> -162 dBm	[*5]
COLD acquisition sensitivity	> -148 dBm	[*6]
Tracking sensitivity	> -162 dBm	
Re-acquisition sensitivity	> -162 dBm	[*7]

Table 3-3. GLONASS performance

Item	Specification	Note
Signal type	GLONASS L1OF	
Channel	MAX 10	[*4]
HOT acquisition sensitivity	> -158 dBm	[*5]
COLD acquisition sensitivity	> -144 dBm	[*6]
Tracking sensitivity	> -158 dBm	
Re-acquisition sensitivity	> -158 dBm	[*7]

Table 3-4. Galileo performance

Item	Specification	Note
Signal type	Galileo E1B/E1C	[*8]
Channel	MAX 8	[*4]
HOT acquisition sensitivity	> -136 dBm	[*5]
COLD acquisition sensitivity	> -136 dBm	[*6]
Tracking sensitivity	> -146 dBm	
Re-acquisition sensitivity	> -136 dBm	[*7]

Table 3-5. QZSS L1C/A performance

Item	Specification	Note
Signal type	QZSS L1C/A	
Channel	MAX 4	[*4] [*11]
HOT acquisition sensitivity	> -136 dBm	[*5]
COLD acquisition sensitivity	> -131 dBm	[*6]
Tracking sensitivity	> -147 dBm	
Re-acquisition sensitivity	> -136 dBm	[*7]
GEO satellite	available	SVID=199 is supported.

Table 3-6. QZSS L1S performance

Item	Specification	Note
Signal type	QZSS L1S	[*9] [*12]
Channel	MAX 2	[*4]
COLD acquisition sensitivity	> -130 dBm	[*6]
Tracking sensitivity	> -134 dBm	
Re-acquisition sensitivity	> -130 dBm	[*7]
SLAS	available	[*10]

Table 3-7. SBAS performance

Item	Specification	Note
Signal type	SBAS L1C/A	SVID=120 to 138 are supported. [*9]
Channel	MAX 2	[*4] [*13]
COLD acquisition sensitivity	> -130 dBm	[*6]
Tracking sensitivity	> -139 dBm	
Re-acquisition sensitivity	> -130 dBm	[*7]

[*1] In the case that the signal of -130 dBm is input to the antenna end by the simulator (In figure 3-1)
[*2] The time from sending HOT restart command to re-acquisition
[*3] The time from sending COLD restart command to re-acquisition
[*4] The maximum number of channels throughout the GNSS is 32.
[*5] After sending HOT restart command during satellite receiving
[*6] After sending COLD restart command during satellite receiving
[*7] Within 250 seconds after the last signal receiving
[*8] Due to the composition of the message broadcast by Galileo, TTFF of Galileo may take about 100 seconds.
[*9] Only one of QZSS L1S and SBAS L1C / A can be used. It can't receive simultaneously.
[*10] SLAS correction is performed to GPS and QZSS.
[*11] Up to 4 satellites can be received simultaneously among 193, 194, 195, 196 and 199.
[*12] Up to 2 satellites can be received simultaneously among 183, 184, 185, 186 and 189.
[*13] WAAS, MSAS, EGNOS and GAGAN are supported.

4 1PPS･CLOCK (GCLK) signal specifications

The follow is the specifications of 1PPS and clock (GCLK). Please refer to the eSIP Protocol Specification for switching setting etc. The performance described in this chapter is measured and evaluated under the environment shown in Figure 4-1 and 4-2 below. In the absence of any notes, measurement conditions are default setting, open sky, constant at 25 degree (no wind).

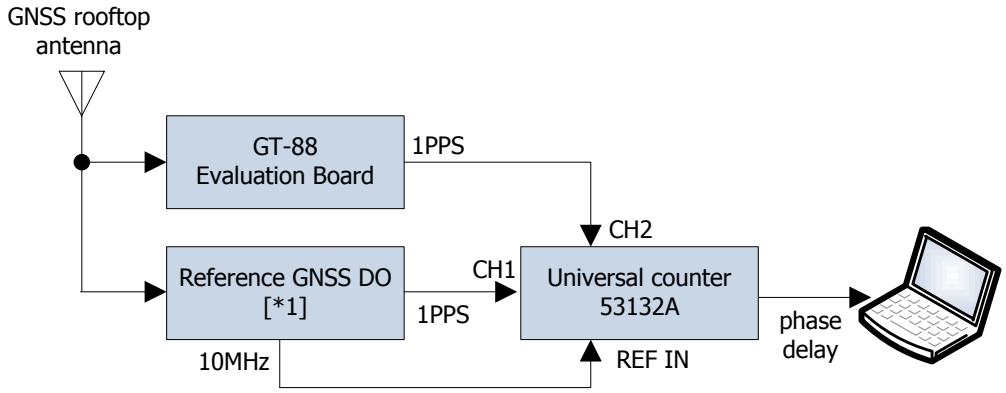


Figure 4-1. 1PPS measurement environment

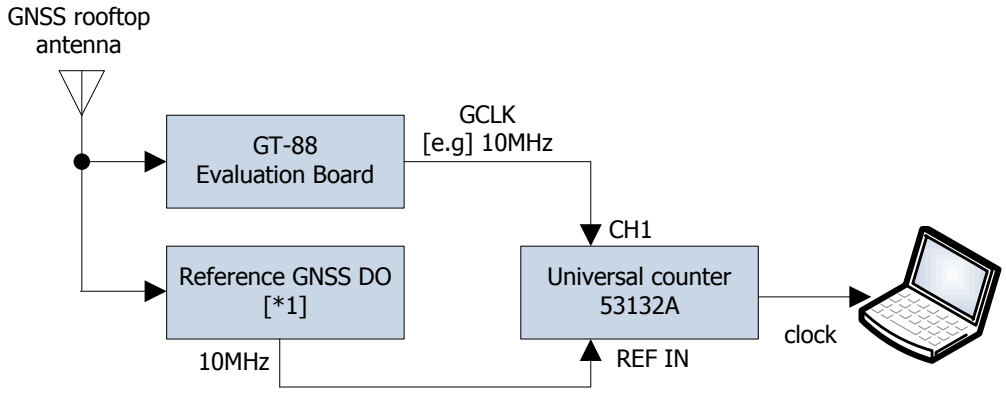
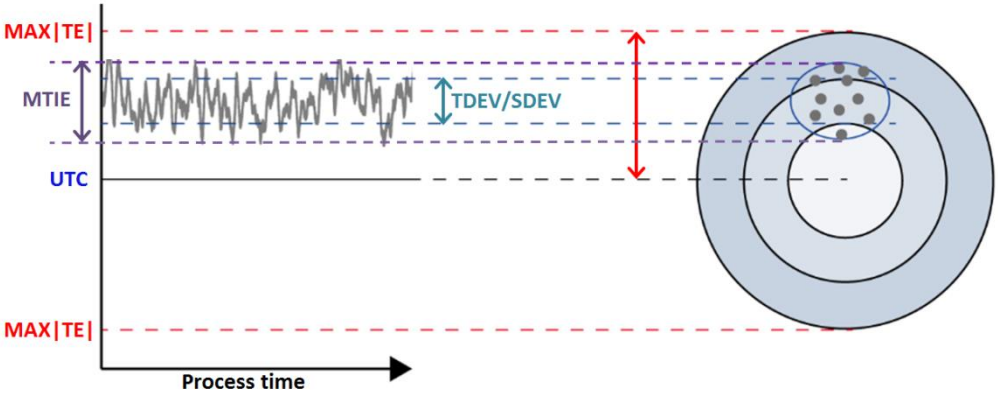


Figure 4-2. GCLK measurement environment

[*1] GNSS Disciplined Oscillators which has rubidium and which has been calibrated by USNO (United States Naval Observatory)

For the specification of 1PPS stability and accuracy, this document defines the follow term.

MAX|TE|: Absolute value of maximum time error. It indicates the maximum deviation of 1PPS from UTC time.
MTIE: Maximum time interval error. It indicates relative MIN-MAX value of 1PPS.
SDEV, TDEV: Standard deviation and Time deviation. They indicate fluctuation condition of 1PPS.



4.1 1PPS

Table 4.1-1. 1PPS general specifications

Item	Specification	Note
1PPS output resolution	+/- 1.75 nsec	time pulse jitter / [*1]
Accuracy of 1PPS output resolution correction	0.001 nsec	[*2]
Holdover function	Available	[*3]
Synchronized target	GPS, UTC	[*4]

[*1] This is hardware resolution of 1PPS output. If this is small, 1PPS can be output with higher stability.
[*2] Please refer to the eSIP Protocol Specification for details.
[*3] By preparing an external oscillator and inputting its frequency to this product, even in a free running state where GNSS can't receive it, this product can output stable 1PPS continuously according to the precision of that oscillator. Please refer to the eSIP Protocol Specification for details.
[*4] 1PPS output is possible in synchronization with GPS or UTC time. Please refer to the eSIP Protocol Specification for details.

Table 4.1-2. 1PPS output specifications

Item	Specification	Note
1PPS accuracy (MAX|TE|)	< 40 nsec	MIN-MAX value from UTC time / [*1][*2]
1PPS stability (Standard deviation)	< 4.5 nsec	@ 1sigma / [*2]
1PPS stability (Time deviation)	G.8272 PRTC-A compliant	@ 1sigma / [*2][*3]
1PPS stability (MTIE)	G.8272 PRTC-A compliant	Relative MIN-MAX value / [*2][*4]

[*1] It is necessary to adjust cable offset beforehand. In addition, it may be necessary to adjust the hardware offset of the entire device incorporating this product.
[*2] After SS mode or CSS mode for more than 24 hours, or after TO mode via it
[*3] TDEV (time deviation) of G.8272 PRTC-A compliant means that it meets the following specifications.

Time deviation limit [nsec]	Observation interval τ [sec]
3	1<τ<100
0.03τ	100<τ<1000
30	1000<τ<10000

[*4] MTIE (maximum time interval error) of G.8272 PRTC-A compliant means that it meets the following specifications.

MTIE limit [nsec]	Observation interval τ [sec]
0.275τ+ 25	1<τ<273
100	273<τ

4.2 Clock (GCLK)

Table 4.2-1. Clock (GCLK) output specifications

Item	Specification	Note
GCLK setting range	10 Hz to 40 MHz	[*1]
GCLK stability	< ± 1 ppb	@ 1sigma / [*2]
GCLK output resolution	< ± 8 nsec	clock total jitter / [*3]
Relation between 1PPS and GCLK	Can be coherent	[*4]

[*1] Please refer to the eSIP Protocol Specifications for GCLK frequency setting.
[*2] It is when the GCLK frequency is 100 Hz or more. When less than 100 Hz, output is possible, but there is no stability specification.
[*3] It is a mechanism to generate arbitrary frequency by using the system clock of this product and built-in adder. By receiving the GNSS satellite, it is possible to output arbitrary frequency accurately. Since the frequency is generated using the adder, it is recommended to check in advance whether jitter and spurious included in the GCLK frequency are within the allowable range of the application to be used.
[*4] GCLK frequency and pulse edge of PPS are synchronized when using GCLK PPS. Please refer to the eSIP Protocol Specifications for details.

5 Environment robustness performance

Table 5-1. Environment robustness performance

Item	Specification	Note
Active anti-jamming	8 CW	[*1]
Multipath mitigation	Available	
T-RAIM function	Available	[*2]
Antenna current detection	Available	[*3]
Spoofing signal mitigation	Available	[*4]
Operating temperature	-40 to +85 degree	[*5]
Storage temperature	-40 to +85 degree	
Operation humidity	< 85 %R.H	[*6]

[*1] It has eight anti-jamming functions for CW waves.
[*2] Time Receiver Autonomous Integrity Monitoring (T-RAIM) is a mechanism to identify and eliminate satellites that may have a bad influence on the positioning calculation by combining and principle of majority when the number of satellites in use is larger than the minimum number of satellites required for positioning.
[*3] The antenna connection state (open, short) can be detected by providing an antenna detection circuit outside. Please refer to the Design Guide (SE13-900-001) for details of the antenna detection circuit.
[*4] This product has a function to notify an alarm by detecting a spoofing signal, and to eliminate the decoding of spoofing signal. Please refer to the eSIP Protocol Specifications for details.
[*5] A sudden temperature change may disturb the frequency of the TCXO installed inside, possibly causing instantaneous satellite reception failure. Especially when installing a fan, it is recommended to take care not to blow the wind directly to this product.
[*6] Ta=60 degree, No condensation

6 Operation restriction

Operation of this product is limited to the following conditions based on the Wassenaar Arrangement (The Wassenaar Arrangement on Export Controls for Conventional Arms and Dual-Use Goods and Technologies).

Table 6-1. Operation restriction

Item	Specification	Note
Altitude	< 18300 meters	
Velocity	< 515 m/s	

7 I/O signal description

The below is name of each terminal of this product, and its details.

Table 7-1. I/O signal description

	Pin name	Type	PU/PD [*1]	Note
1	RESERVED	-	-	Don't connect anything
2	FLNA	Digital input	PD	LNA gain select pin [*2]
3	PPS	Digital output	PD	PPS output pin / Don't pull-up externally [*3]
4	RESERVED	-	-	Don't connect anything
5	ANT_DET1	Digital input	PU	Antenna detection input pins
6	ANT_DET0	Digital input	PU	Antenna detection input pins
7	RESERVED	-	-	Don't connect anything
8	RST_N	Digital input/output	PU	External reset signal input pin [*4][*5][*6]
9	RESERVED	-	-	Don't connect anything
10	GND	-	-	Ground
11	RF_IN	Analog input	-	GNSS signal input pin
12	GND	-	-	Ground
13	GND	-	-	Ground
14	EPPS	Digital input	-	Don't connect anything
15	GCLK	Digital output	PD	Clock output pin / Don't pull-up externally [*3]
16	ECLK	Digital input	PD	External clock input pin for holdover Please leave open if not used.
17	RESERVED	-	-	Don't connect anything
18	RXD2	Digital input	-	Don't connect anything
19	TXD2	Digital output	-	Don't connect anything
20	TXD1	Digital output	-	UART1 transmission output pin
21	RXD1	Digital input	PU	UART1 reception input pin
22	VBK	Power input	-	Backup power supply input pin [*7]
23	VCC	Power input	-	Main power supply input pin
24	GND	-	-	Ground

[*1] PU: Pull-Up, PD: Pull-Down. See Section 9.4 for each resistor values.
[*2] Logic L (leave open): High gain / Logic H (connect to VCC): Low gain
[*3] These pins have pull-down resistors inside to ensure power-on configuration, so it is prohibited to connect any pull-up resistor outside of the module.
[*4] RST_N is Wired-OR with internal power-on reset (POR_N) signal.
[*5] Please drive with an open-drain or an open-collector device.
[*6] Logic L: Reset / Logic H (Open): Normal Operation
[*7] Please leave open if battery backup function is not used.

The pin arrangement is as follows.

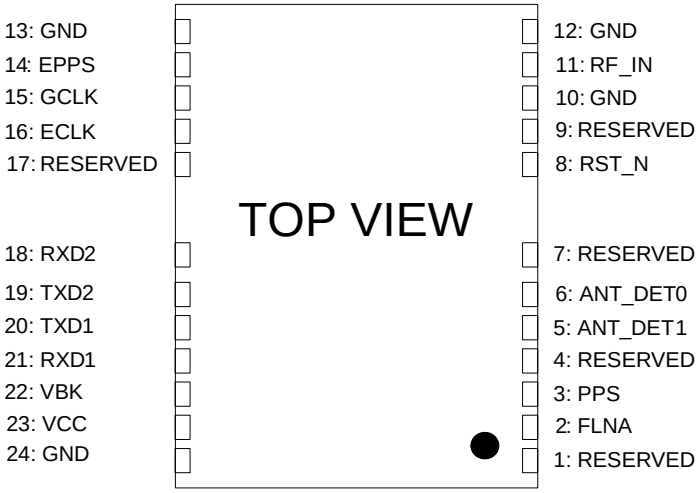


Figure 7-1. Pin arrangement

Precaution on using the input pin with pull-up resistor

When the input pin with a pull-up resistor is connected to a signal source through an in-series resistor R_{in} (that includes the output impedance of the signal source), R_{in} must be less than or equal to 180Ω.

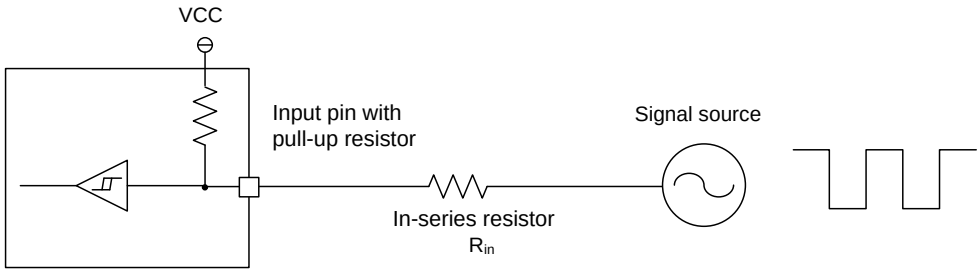


Figure 7-2. Precaution on using the input pin with pull-up resistor

8 Communication specifications

This product can send commands and receive sentences by the eSIP protocol which complies NATIONAL MARINE ELECTRONICS ASSOCIATION (NMEA0183 Ver.4.10). Please refer to the eSIP Protocol Specifications for details.

9 Electrical characteristics

9.1 Absolute Maximum Rating

Table 9.1-1 shows the values when used in the operating temperature range shown in Chapter 5. Stresses beyond those listed under those range may cause permanent damage to module.

Table 9.1-1. Absolute Maximum Rating

Item	Symbol	MIN	MAX	Unit	Note
Supply voltage	V_{CC_ABS}	-0.3	4.0	V	
Backup supply voltage	V_{BK_ABS}	-0.3	4.0	V	
Digital input (DI) voltage	-	-0.3	4.0	V	
Digital output (DO) current	-	-	± 7	mA	
VCC_RF output current	$I_{CC\_RF\_ABS}$	-	150	mA	
RF_IN input power (High Gain mode)	P_{RFINH_ABS}	-	-20	dBm	[*1]
		-	1		[*2]
		-	1		[*3]
RF_IN input power (Low Gain mode)	P_{RFINL_ABS}	-	-5	dBm	[*1]
		-	0		[*2]
		-	-1		[*3]

[*1] at 1575.42 MHz & 1602 MHz
[*2] at 900 MHz
[*3] at 1800 MHz

9.2 Power supply

Below are power supply specifications.
The conditions satisfying this specification are Ta = 25 ° C.

Table 9.2-1. Power Supply Characteristics

Item	Symbol	MIN	TYP	MAX	Unit	Note
Supply voltage to VCC	V_{CC}	3.0	3.3	3.6	V	
Backup supply to VBK	V_{BK}	1.4	-	3.6	V	
Rising slew rate of VCC	V_{CC_SR}	-	-	$3.6x10^4$	V/s	[*1][*7]
Rising slew rate of VBK	V_{BK_SR}	3.6	-	$3.6x10^4$	V/s	[*1][*7]
Output voltage from VCC_RF	V_{CC_RF}	V_{CC} -0.2	-	V_{CC}	V	[*2]
VCC current consumption Low Gain mode (FLNA: High)	I_{CCAL}	-	60	108	mA	[*3][*6]
	I_{CCTH}	-	55	-		[*4][*6]
VCC current consumption High Gain mode (FLNA: Open)	I_{CCAH}	-	68	116	mA	[*3][*6]
	I_{CCTH}	-	62	-		[*4][*6]
VBK current consumption at back up	I_{BKN}	-	9	20	μA	[*5]
VBK current consumption at normal operation	I_{BKB}	-	0.4	2	μA	[*6]

[*1] About rising slew rate、please see figure 9.2-1.
[*2] Icc_RF = 100 mA
[*3] In case of Ta=85 degree and Full Search condition (GPS+GLONASS+Galileo+QZSS+SBAS)
[*4] GNSS setting: GPS+GLONASS+Galileo+QZSS+SBAS, Open sky, Tracking
[*5] Vcc = 0 V
[*6] Vcc = 3.3 V
[*7] When the rising slew rate is more than $3.6x10^4$ V/s, the internal ESD protection circuit turns on during the voltage rising and the inrush current of the power supply may be increased. However, it does not cause damage to the module.

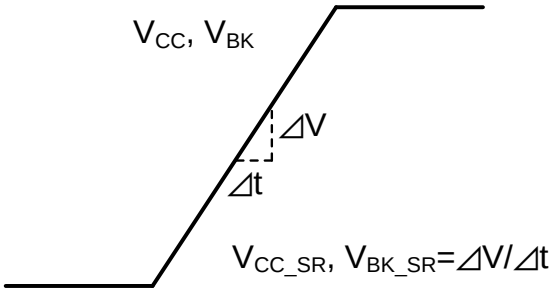


Figure 9.2-1. Rising Slew Rate

9.3 Reset

This product contains an internal power-on reset circuit which detects VCC voltage and creates POR_N (power-on reset) signal for initializing module.

The follow shows the threshold voltages to detect and create POR_N signal.

Table 9.3-1. Power-on Reset Voltage

Item	Symbol	MIN	TYP	MAX	Unit	Note
Power On Reset threshold voltage (rising)	V_{RTH_POR}	-	-	3.0	V	
Power On Reset threshold voltage (falling)	V_{FTH_POR}	2.7	-	-	V	

In most cases, it is not required to drive external reset input (RST_N) pin. However, if it is needed to force being in reset state externally for e.g. synchronizing reset state with application circuitry, RST_N can be used for this purpose. RST_N should be driven by open-drain or open-collector device for avoiding any collision with internal power-on reset driver.

CPU reset is released when both the internal power on reset and the external reset (RST_N) are released.

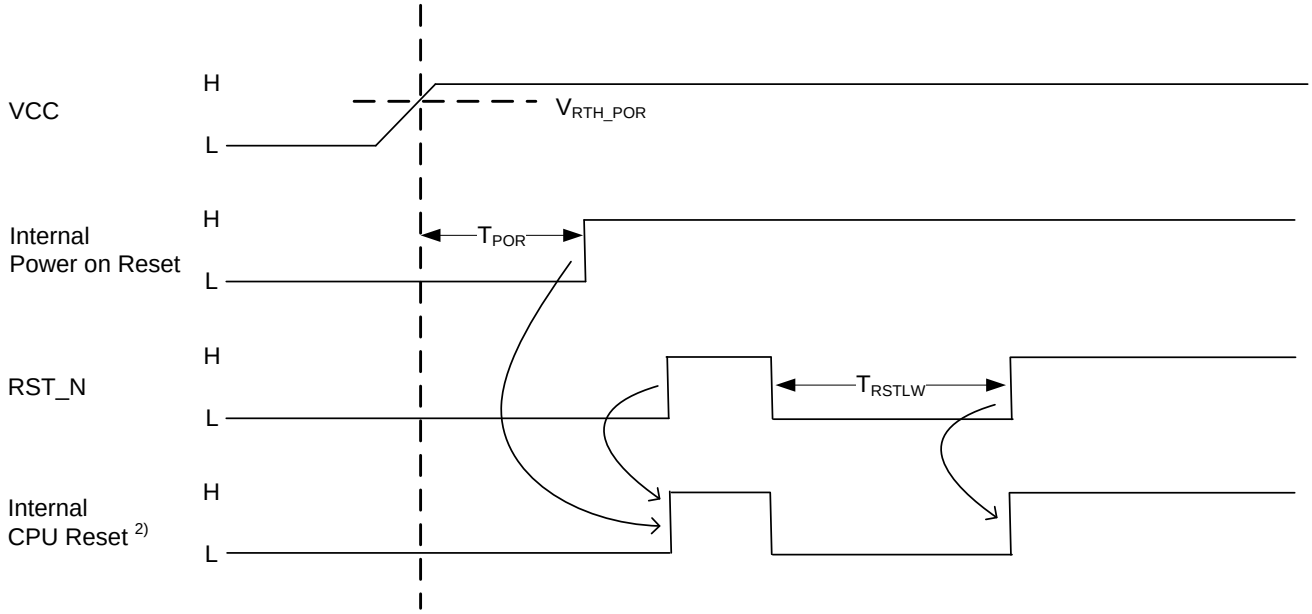


Figure 9.3-1. Reset Sequence

Table 9.3-2. Reset Sequence

Item	Symbol	MIN	MAX	Unit	Note
Internal power on reset released time	T_{POR}	150	250	msec	[*1]
Reset pulse width	T_{RSTLW}	300	-	msec	

[*1] after VCC reaches V_{RTH_POR}

9.4 Interface Signal

Table 9.4-1. Interface signal

Item	Symbol	MIN	TYP	MAX	Unit	Note
Logic L input voltage	V_{IL}	-	-	0.8	V	
Logic H input voltage	V_{IH}	2.0	-	-	V	
Hysteresis voltage	V_{hst}	0.31	-	-	V	
Logic L output voltage	V_{OL}	-	-	0.4	V	[*1]
Logic H output voltage	V_{OH}	2.4	-	-	V	[*2]
Equivalent pull-up resistor	R_{PU}	29	41	62	kΩ	[*3]
Equivalent pull-down resistor	R_{PD}	30	44	72	kΩ	[*4]

[*1] at $|I_{OL}|$ = 2 mA
[*2] at $|I_{OH}|$ = 2 mA
[*3] at V_I = 3.3 V
[*4] at V_I = 0 V

9.5 Baud rate setting

Table 9.5-1. Baud rate vs. Deviation error

Baud rate [bps]	Deviation error [%]
4800	+0.00
9600	+0.11
19200	-0.11
38400	+0.32
57600	-0.54
115200	-0.54
230400	+2.08
460800	-3.02

9.6 UART Wake-up Timing after Reset

Below is the specification of the start timing of UART input / output.
If external reset is not used, it is as follows.

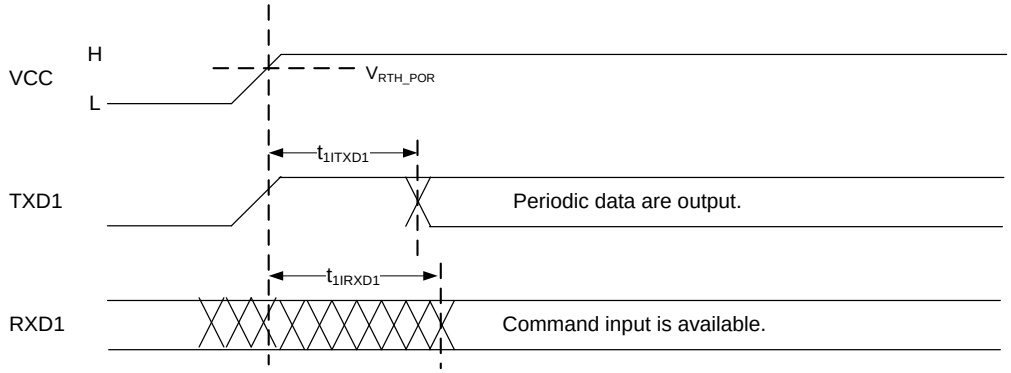


Figure 9.6-1. UART Wake-up Timing after V_{RTH_POR}

Table 9.6-1. UART Wake-up Timing after V_{RTH_POR}

Item	Symbol	TYP	MAX	Unit	Note
Time delay until periodic data output	t_{1ITXD1}	3.3	6	sec	[*1]
Time delay until the command input is available	t_{1IRXD1}	3.3	6	sec	[*1]

[*1] after VCC reaches V_{RTH_POR}

If external reset is used, it is as follows.

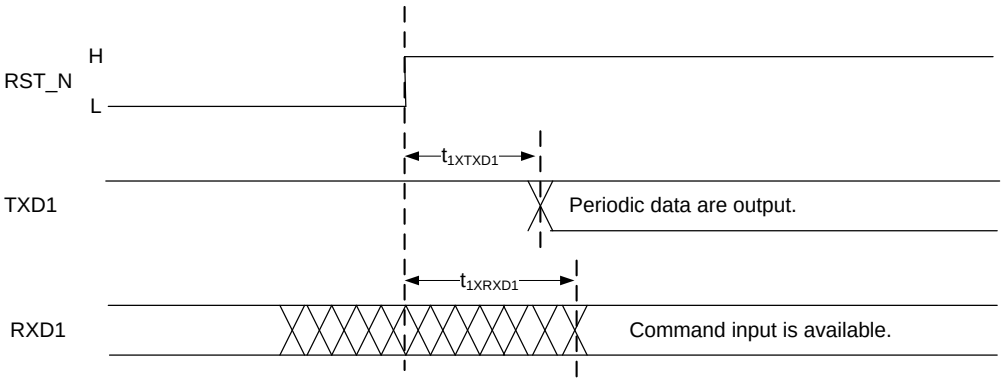


Figure 9.6-2. UART Wake-up Timing after RST_N

Table 9.6-2. UART Wake-up Timing after RST_N

Item	Symbol	TYP	MAX	Unit	Note
Time delay until periodic data output	t_{1ITXD1}	3.1	6	sec	[*1]
Time delay until the command input is available	t_{1IRXD1}	3.1	6	sec	[*1]

[*1] after RST_N set to H

9.7 Recommended GNSS Antenna

For examples of the use of each antenna, please refer to Module Design Guide (SE13-900-001).

Table 9.7-1. Recommended Active Antenna

Item	MIN	TYP	MAX	Unit	Note
GPS/QZSS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Galileo center frequency	-	1575.42	-	MHz	4.092 MHz bandwidth
Antenna element gain	0	-	-	dBi	
Amplifier gain1	10	-	35 [*3]	dB	[*1]
Amplifier gain2	15	-	50 [*3]	dB	[*2]
Amplifier NF	-	1.5	3	dB	
Impedance	-	50	-	Ω	
VSWR	-	-	2	-	

[*1] Including cable loss / High Gain mode (FLNA: Open)
[*2] Including cable loss / Low Gain mode (FLNA: High)
[*3] For best jammer resistance (and lower power consumption), use 10 dB lower gain than the max gain.

Table 9.7-2. Recommended Passive Antenna

Item	MIN	TYP	MAX	Unit	Note
GPS/QZSS center frequency	-	1575.42	-	MHz	2.046 MHz bandwidth
GLONASS center frequency	-	1602	-	MHz	9 MHz bandwidth
Galileo center frequency	-	1575.42	-	MHz	4.092 MHz bandwidth
Antenna element gain	0	-	-	dBi	[*1]
Impedance	-	50	-	Ω	
VSWR	-	-	2	-	

[*1] High Gain mode (FLNA: Open)

10 Equivalent circuit

Table 10-1. Equivalent circuit list

	Pin Name	Equivalent circuit
1	RESERVED	**Figure 10-1**
2	FLNA	**Figure 10-5**
3	PPS	**Figure 10-5**
4	RESERVED	**Figure 10-5**
5	ANT_DET1	**Figure 10-1**
6	ANT_DET0	**Figure 10-1**
7	RESERVED	**Figure 10-5**
8	RST_N	**Figure 10-2**
9	VCC_RF	**Figure 10-3**
10	GND	-
11	RF_IN	**Figure 10-6**
12	GND	-
13	GND	-
14	EPPS	**Figure 10-5**
15	GCLK	**Figure 10-5**
16	ECLK	**Figure 10-5**
17	RESERVED	**Figure 10-1**
18	RXD2	**Figure 10-1**
19	TXD2	**Figure 10-1**
20	TXD1	**Figure 10-4**
21	RXD1	**Figure 10-1**
22	VBK	**Figure 10-3**
23	VCC	**Figure 10-3**
24	GND	-

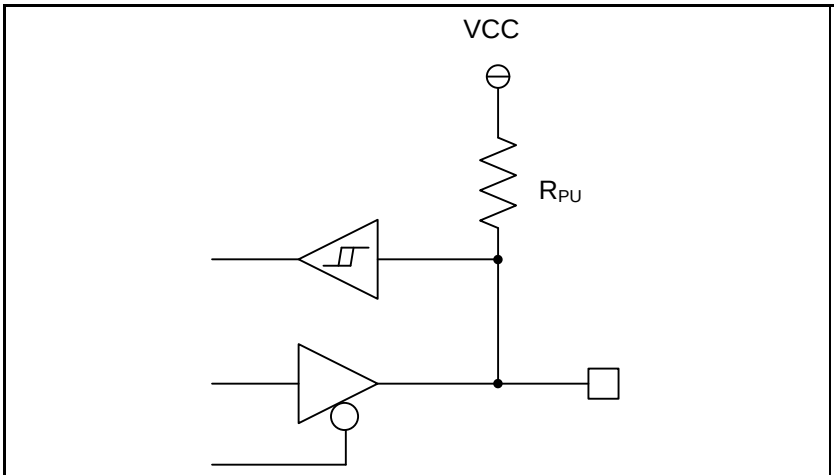


Figure 10-1. Equivalent circuit 1

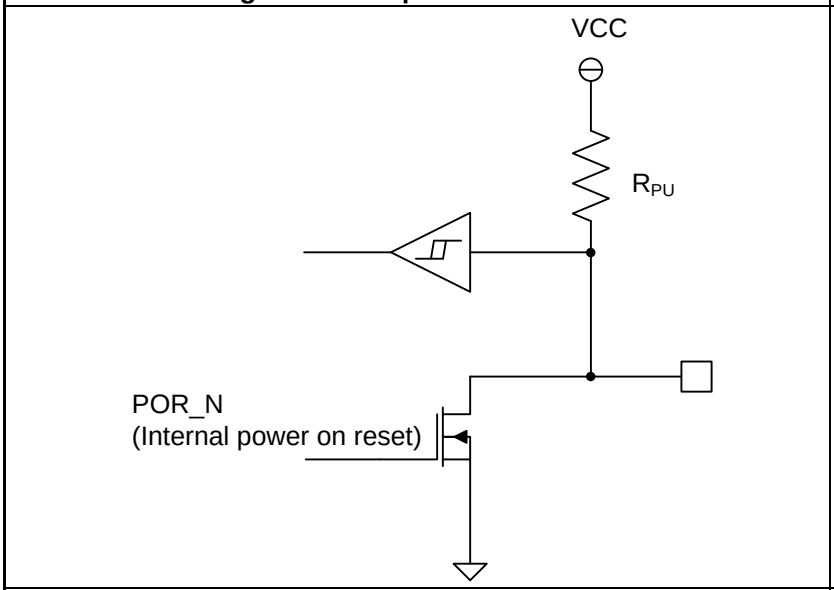


Figure 10-2. Equivalent circuit 2

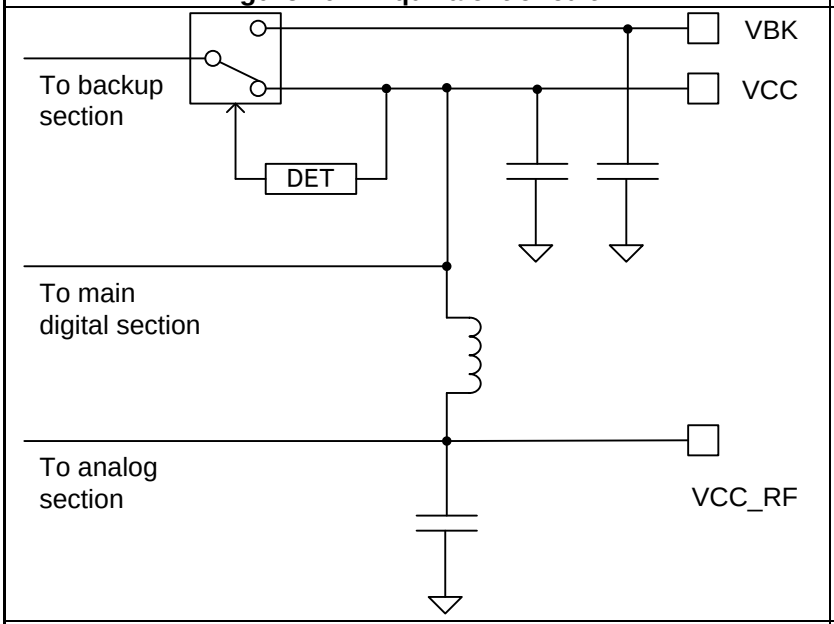


Figure 10-3. Equivalent circuit 3

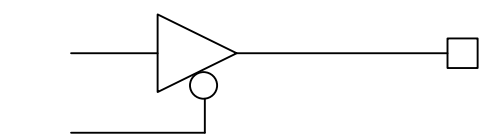


Figure 10-4. Equivalent circuit 4

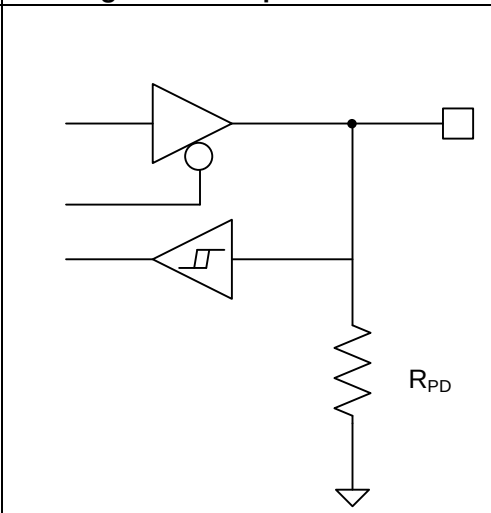


Figure 10-5. Equivalent circuit 5

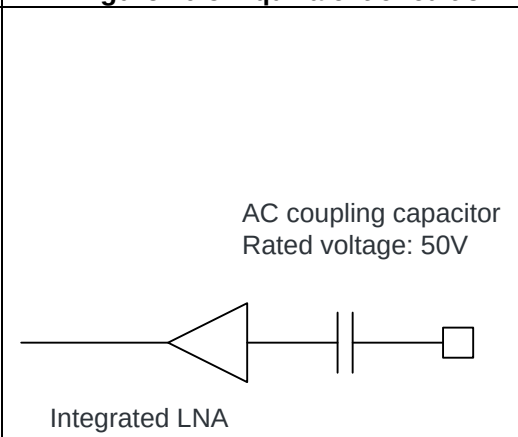


Figure 10-6. Equivalent circuit 6

11 Mechanical Specifications

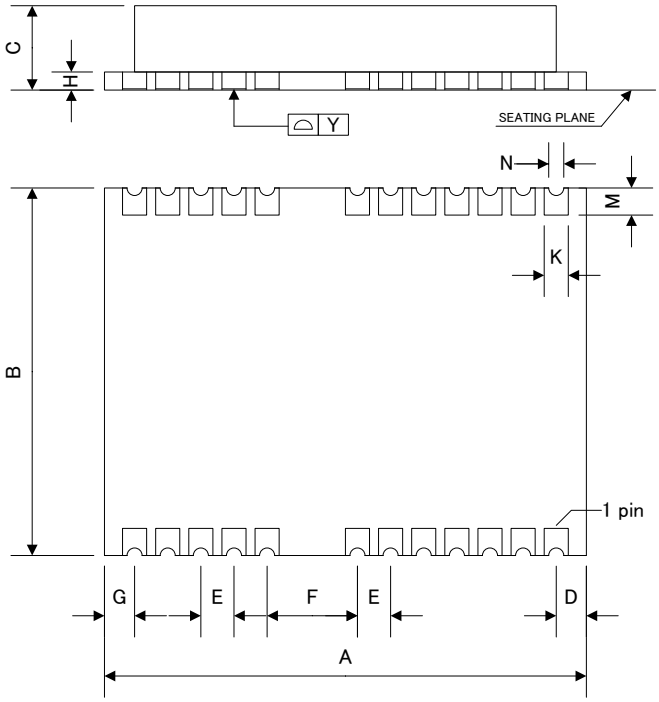


Figure 11-1. Package dimension

Table 11-1. Package dimension

	MIN	TYP	MAX	unit	Notes
A	15.8	16.0	16.2	mm	
B	12.0	12.2	12.4	mm	
C	2.6	2.8	3.0	mm	
D	0.9	1.0	1.1	mm	
E	1.0	1.1	1.2	mm	
F	2.9	3.0	3.1	mm	
G	0.9	1.0	1.1	mm	
H	-	0.6	-	mm	
K	0.7	0.8	0.9	mm	
M	0.8	0.9	1.0	mm	
N	0.4	0.5	0.6	mm	
Y	-	-	0.1	mm	[*1]

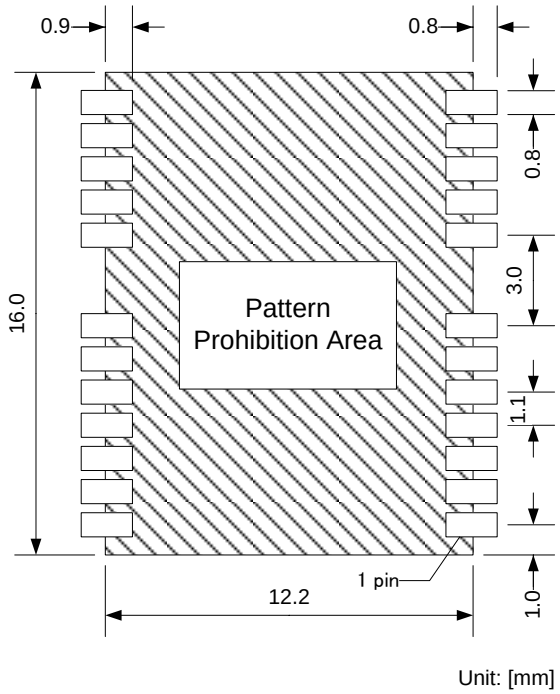
[*1] The height of the terminals to the mounting surface

Table 11-2. Mechanical specifications

Items	Description	Notes
Electrode material	Cu	[*1]
Weight	1.01g (TYP)	
RoHS	complied	

[*1] Metallic Finishing: Electroless gold flashing (Au: 0.03 μ and over, Ni: 3 μ and over)

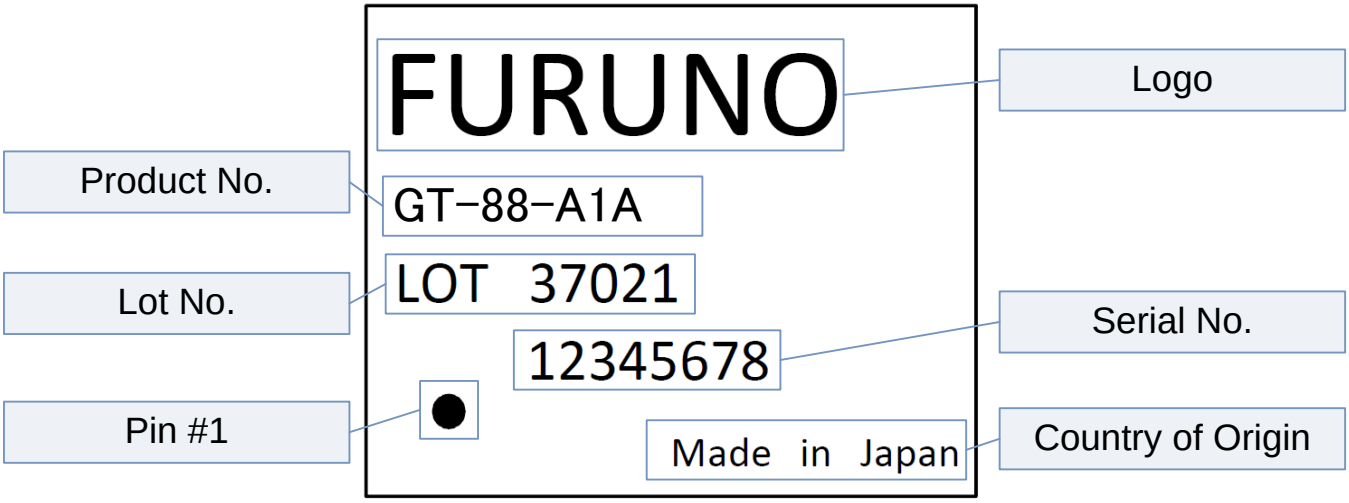
There are some signal lines and via holes on the bottom of the module. For avoiding any signal shortage, do not put any signal line nor via hole at the part of the user's board where is facing to the bottom of the module.



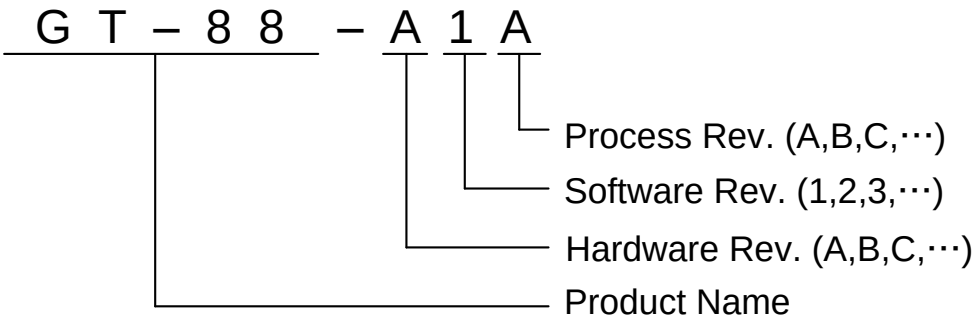
Unit: [mm]

Figure 11-2. Recommended Land Pattern

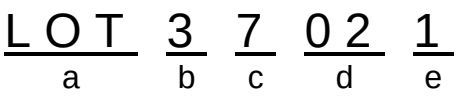
12 Marking



(1) Logo FURUNO
(2) Product No. GT-88-A1A



(3) Lot No. LOT 37021



#	Code	Description
a	LOT	"LOT"
b	3	Year (last digit of the year number: 2023=3)
c	7	Month (1 to 9, X, Y, Z)
d	02	Date (01 to 31)
e	1	Internal control number

(4) Serial No. 12345678
Individual unique number
(5) Country of origin Japan
(6) Pin 1 symbol

13 Packing Specifications

Please refer to the module packing specifications (SE13-600-024).

14 Reliability Test

Please refer to the module reliability test (SE16-600-012).

15 Special Instruction

(1) Components in the module are planned to be purchased from multiple manufacturers / vendors according to FURUNO's procurement policy. Therefore, multiple components from multiple manufacturers / vendors may be used even in the same production lot.

(2) This product contains semiconductor inside. While handling this, be careful about the static electrical charge (less than 100V). To avoid it, use conductive mat, ground wristband, anti-static shoes, ionizer, etc. as may be necessary.

(3) Avoid mechanical shock and vibration. Do not drop this product.

(4) When mounting this product, be aware of the location of the electrode.

(5) This product should not be washed.

(6) The reflow conditions are as shown in Chapter 16.

(7) This product includes a crystal oscillator. It may not be able to maintain the characteristics under the vibrating condition, windy and cold conditions and noisy conditions. Please evaluate the module on ahead, if it may be used under these conditions.

(8) Surface mount products may have a crack when thermal stress is applied during surface mount assembly after they absorb atmospheric moisture. Therefore, please observe the following precautions:
   ① Store the moisture barrier bag in an environment of 30 °C / RH 90% or less, and use it within 12 months.
   ② After opening, this product should be assembled within one week in an environment of 30 °C / RH 60% or less.
   ③ If, upon opening, the moisture indicator card in the bag shows humidity above 30% or the expiration date has passed, they may still be used with the addition of a bake of 24 hours at 125 °C.
   Caution: If the packing material is likely to melt at 125 °C, heat-proof tray or aluminum magazine, etc. must be used for high temperature.
   ④ Expiration date: 12 months from the sealing date.

(9) If the internal temperature exceeds 215 °C when the product is heated partially with, for example, a soldering iron, a hot air or a light beam welder, the internal wiring may be disconnected by a thermal stress.

16 Solder Profile

The reflow profile is based on the IPC/JEDEC J-SED-020D.

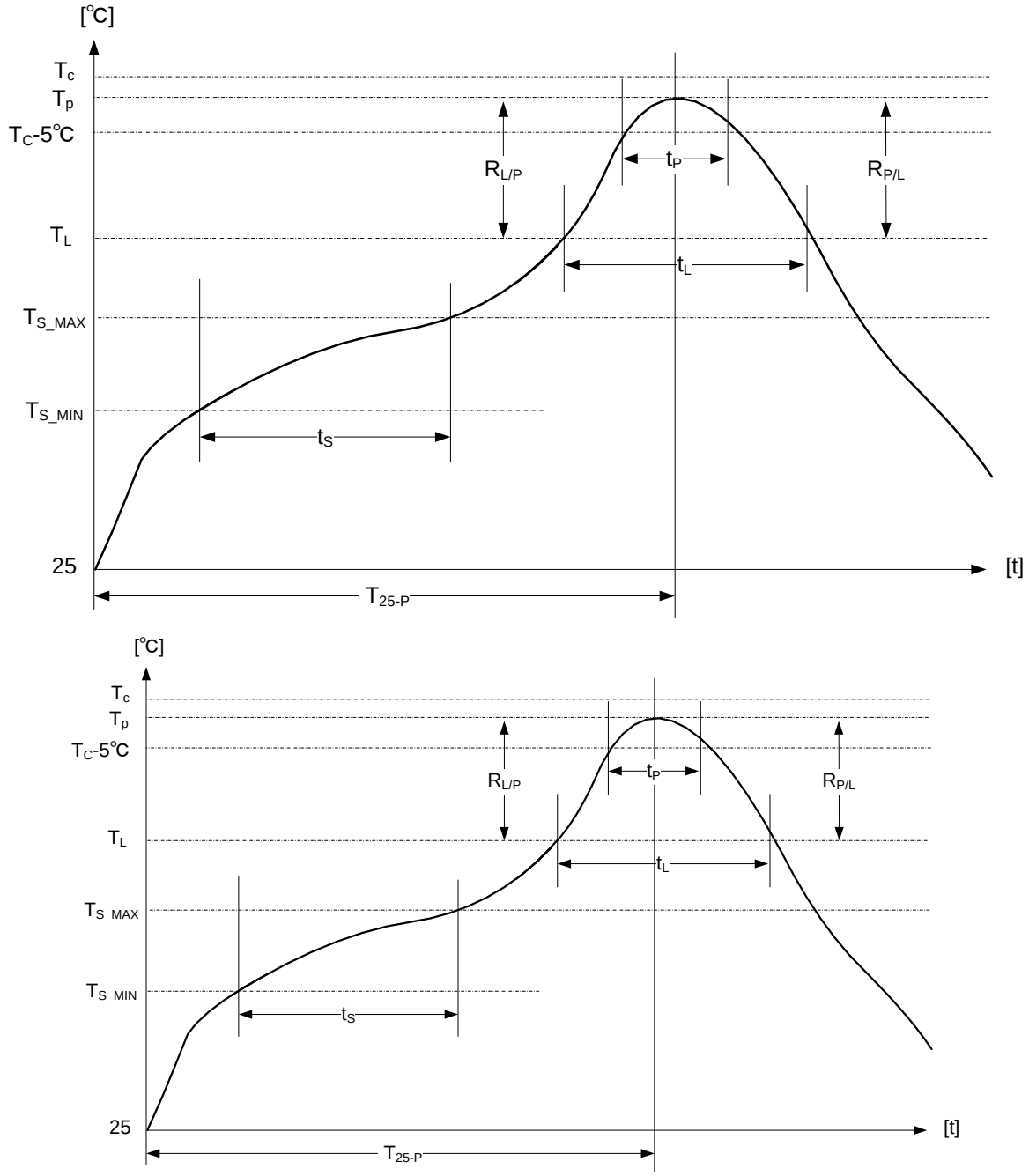


Figure 16-1. Reflow condition

Table 16-1. Reflow condition (Pb-free)

Item	Symbol	Condition	Notes
Preheat/soak minimum temperature	$T_{S\text{-}MIN}$	150°C	
Preheat/soak maximum temperature	$T_{S\text{-}MAX}$	200°C	
Preheat/soak time from $T_{S\text{-}MIN}$ to $T_{S\text{-}MAX}$	t_S	60 to 120 s	
Ramp-up rate T_L to T_P	$R_{L/P}$	3°C/s (Max)	

Liquidus temperature	T_L	217 to 220°C	
Time maintained above T_L	t_L	60 to 150 s	
Specified classification temperature	T_C	260°C	
Time within 5°C of T_C	t_P	30 s	Tolerance for t_P is defined as a user maximum
Ramp-down rate T_P to T_L	$R_{P/L}$	6°C/s (Max)	
Time from 25°C to peak temperature	$T_{25\text{-}P}$	8 min. (Max)	

Notes:

- Lead free solder is recommended.
- Recommended atmosphere in chamber is Nitrogen.
- Oxygen density level is less than 1500 ppm.
- Profile temperature should be measured on top of the shielding case.
- Packing condition except IPC/JEDEC J-STD-020D needs pre-baking.
- When reflowing under conditions different from the recommended reflow profile, please do so at your own risk. It may affect the solder connection between the module and the customer's board and the solder re-melting of components mounted on the module.
- Moisture Sensitivity Level is 3.
- Number of reflow for assembly at user side is 2.