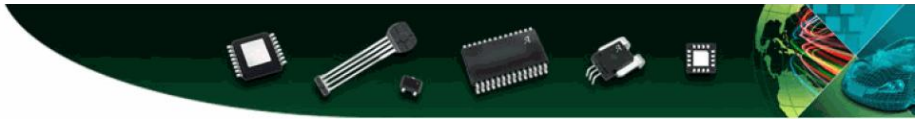

PCN Number:05302017
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Product/Process Change Notification (PCN)

Customer: Digi-Key **Date: 06-02-2017**

Customer Part #: A3980KLPTR-T

Originator: R. Fennelly **Phone: (508) 853-5000**

Duration of Change: Permanent [X] Temporary (explain) [ ]

Summary description of change: Part Change: [ ] Process Change: [X] Other: [ ]

Allegro currently manufactures the A3980KLPTR-T at wafer fab, Polar Semiconductor LLC (PSL), Bloomington, MN, USA, utilizing 6" ABCD3 technology. The 6" wafer line is closing. Allegro will be changing wafer fab manufacturing to the 8" ABCD3 technology wafer line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA.

Allegro will permanently close its wafer probe operations in Worcester, Massachusetts, USA by March 31, 2018. Wafer probe operations will be moved to Allegro MicroSystems Philippines, Inc. (AMPI) located in Manila, Philippines for the part numbers listed in this PCN.

In addition to the current Allegro MicroSystems, LLC test facility location in Manila Philippines, a new test facility referred to as Allegro MicroSystems (Thailand) Co., Ltd. (AMTC) located in Saraburi, Thailand will be added as a primary test location.

What is the part or process changing from (provide details)?

Wafer fab for the device (s) listed is currently out of Polar Semiconductor LLC (PSL), Bloomington, MN, USA, utilizing 6" ABCD3 technology.

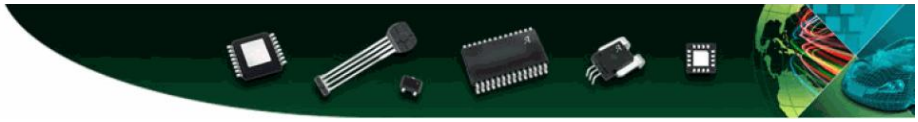
Currently the device (s) listed is probed in Allegro's Worcester facility.

The listed device is currently tested at the Allegro MicroSystems, LLC test facility located in Manila Philippines.

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

Allegro will be changing wafer fab manufacturing to the 8" ABCD3 technology wafer line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA.

Probe location for the listed device(s) will be moved to AMPI. Allegro is utilizing the same probe equipment, test programs and test methodologies in the Philippine facility as are currently being used in



the US facility. Relocation of probe operations reduces movement of wafers between factories shortening overall cycle time and minimizing wafer handling. All expansions of probe capability and capacity will now occur at AMPI to support Allegro's future business growth.

The primary test location for the listed device will be the Allegro MicroSystems (Thailand) Co., Ltd. (AMTC) located in Saraburi, Thailand location.

Is a PPAP update required? Yes [ ] No [X]

Is reliability testing required?

(If Yes, refer to attached plan)

Reliability Qualification Results

Device: **3980 (7880)**
Assy Lot #: **1642978UAAA**
Number of Leads: **28**
Fab Location: **PSL**

Package: **LP (TSSOP)**
Assembly Location: **Unisem**
Lead Finish: **100% Tin**
Tracking Number: **3764**

Reason for Qualification: ***3980 (7880) – DMOS Microstepping Driver with Translator***

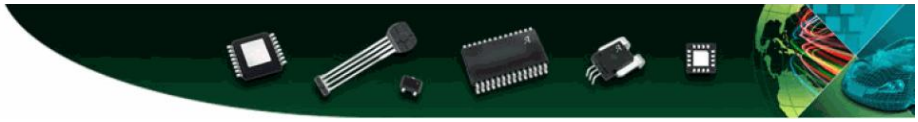
Reliability Qualification Results

3980 (7880), STR#3764					Requirements	
Stress Test	**Abv.**	**Test #**	**Test Method**	**Test Conditions**	**S.S.**	**Results**
Preconditioning	PC	A1	JESD22-A113 / J-STD-020	85°C/60% RH, 168 hrs, Peak Reflow=260°C; MSL2, (HAST, AC, TC)	231	0 Rejects
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 85% RH, 0, 96 hrs	77	0 Rejects
Autoclave	AC	A3	JESD22-A102	Ta=121°C, 100% RH, 15 psig, 0, 96 hrs	77	0 Rejects
Temperature Cycle	TC	A4	JESD22-A104	Ta = -65°C to +175°C, 0, 500, 1000 Cycles	77	0 Rejects
Wire Bond Shear	WBS	C1	JESD22-B116	Test conditions described in Test Method	5	0 Rejects; Ppk>1.67
Wire Bond Pull	WBP	C2	Mil-Std-883 Method 2011	Temp conditions and sample size are defined in the test method. (after TC)		0 Rejects; Ppk>1.67
Solderability	SD	C3	JESD22-B102	Meniscograph	10	0 rejects; > 95% Lead Coverage
High Temperature Operating Life	HTOL	B1	JESD22-A108	Ta = 125°C, 0, 1000 hrs	77	0 Rejects
Early Life Failure Rate	ELFR	B2	AEC-Q100-008 / JESD22-A108	Ta = 125°C, 0, 48 hrs	800	0 Rejects
Electrostatic Discharge Human Body Model(STR#3813)	HBM	E2	AEC-Q100-002 / JS-001-2014	Test Conditions, Sampling Size are defined in the Test Method		Classification 2, HBM =2.0 kV
Electrostatic Discharge Charged Device Model	CDM	E3	AEC-Q100-011	Test Conditions, Sampling Size are defined in the Test Method		Classification = C6, > 1kV
Latch-Up	LU	E4	JESD78	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level B
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions	30 pcs	0 Rejects; Cpk>1.67

This device qualification is considered to be passing all environmental stress evaluations per the Allegro MicroSystems, 900019 specification and AEC-Q100.

Approved by:

Bob Demers
Bob Demers
Product Safety and Reliability
Allegro MicroSystems, LLC



Expected completion date for internal qualification: Complete

Expected Data availability date: May 2017

Target implementation date: March 2018

Estimated date of first shipment: April 2018

Expected sample availability date: Upon request

Customer Approval Required:	**Yes**		**Date Required:**
	No	X	**Notification Only**

Please note: It is our intention to inform our customer of changes as early as possible. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled.

Customer comments/Conditions of Acceptance:

Approved by: Date: Title:

cc: Allegro Sales/Marketing/Quality