Product/Process Change Notice - PCN 22_0184 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: AD9544 Data Sheet Specification Changes

Publication Date: 08-Aug-2022

Effectivity Date: 10-Nov-2022 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

Revision of the AD9544 Product Data Sheet from Rev0 to RevA.

The following summarizes the data sheet specification changes...

1) System Clock Inputs, XOA and XOB Table 4:
1a) The Slew Rate for Sinusoidal Input expands to two line items below:
1b) Functional, >6 V/us TYP.
1c) Operational, >31 V/us TYP (formerly 50 V/us MIN).
1d) Comment added to DIRECT path heading: "Do not enable the frequency doubler when using the direct path."
1e) Removal of the System Clock Input Doubler specification from the Input Frequency Range specification in the DIRECT path section of the table.
1f) Removal of the System Clock Input Doubler Duty Cycle specification from the DIRECT path section of the table.
1g) Addition of a Duty Cycle specification to the DIRECT path section of the table with 40%/60% Min/Max limits.
1h) Comment added to the CRYSTAL path heading: "The crystal resonator path includes an optional frequency doubler".
1i) The Max specification for the crystal resonator increases from 60 MHz to 80 MHz.

2) Reference Inputs Table 5:
2a) Differential Mode Slew Rate limit change; from 20 V/us MIN to >4.1 V/us TYP.
2b) Addition of DC-Coupled, LVDS-Compatible Mode Slew Rate line item; >1.2 V/us TYP.
2c) Addition of Single-Ended Mode Slew Rate, 1.2V CMOS line item; >8 V/us TYP.
2d) Addition of Single-Ended Mode Slew Rate, 1.8V CMOS line item; >8 V/us TYP.
2e) Addition of Single-Ended Mode Slew Rate, AC-Coupled line item; >8 V/us TYP.

3) Distribution Clock Outputs Table 8:
3a) Differential Mode; addition of Rise/Fall Time line items.
3b) Differential Mode; addition of Duty Cycle line items.
3c) Single-Ended Mode; addition of Rise/Fall Time line items.
3d) Single-Ended Mode; addition of Duty Cycle line items.

4) Time Duration of Digital Functions Table 9:
4a) Addition of "Time from Release of Power Down to Completion of System Clock PLL Calibration" line item.
4b) Addition of "Time from Release of Power Down to System Clock PLL Locked and Calibrated" line item.

5) Holdover Specifications Table 12:
5a) Relative Frequency Accuracy, Cascaded DPLL Operation limit change; from 0 ppb TYP to 0 ppb MAX.
5b) Addition of Relative Frequency Accuracy, Non-Cascaded DPLL Operation line item; <1 ppb TYP.

6) Logic Output Specifications (M0 to M6) Table 20:
6a) Addition of Rise/Fall Time line items.

7) Temperature Sensor Specifications Table 16:
7a) Accuracy, Absolute line item changes to Accuracy, Absolute Die Temperature
7b) Accuracy, Relative line item changes to Accuracy, Relative Die Temperature.

8) Serial Port Specification, I2C Mode Table 18:
8a) In the Conditions/Comments column of the SCL/SDA Fall Time, tF line item, addition of the following: Min specification requires configuring SDIO/SDA pin for low drive strength (bit 7 in register 0x0109 set to 1).
8b) In the Conditions/Comments column of the Data Hold Time, tHD;DAT line item, addition of the following: Not compliant with the I2C

specification of 0 µs min, 0.9 µs max in fast mode.

9) Addition of new tables:
9a) Operating Temperature
9b) Reference-to-Reference Coupling
9c) Output-to-Output Timing Skew
9d) DPLL Propagation Delay
9e) DPLL Propagation Delay Variation
9f) Mx-to-Mx Pin Output Timing Skew

10) Absolute Maximum Ratings
10a) Addition of Output Drivers line item.
10b) Removal of Operating Temperature Range line item (moved to the new Operating Temperature table in the Specifications section).

11) Addition of new Typical Performance Characteristics plots:
11a) Mx Pin Waveforms for Various Load Conditions
11b) DPLL Delay Compensation Versus Temperature, Differential AC-Coupled Input Reference Mode
11c) DPLL Delay Compensation Versus Temperature, 1.8V CMOS Input Reference Mode
11d) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 50 ppb
11e) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 4.6 ppm
11f) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 100 ppm

Reason For Change:

The data sheet is in the process of revision to more thoroughly and accurately specify device performance and functionality.

Impact of the change (positive or negative) on fit, form, function & reliability:

The changes described above have no impact on fit, form or reliability of the device.

Summary of Supporting Information:

This change will be reflected in Rev A of the Product Data Sheet.

Supporting Documents None

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (2)				
AD9544 / AD9544BCPZ	AD9544 / AD9544BCPZ-REEL7			

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	08-Aug-2022	10-Nov-2022	Initial Release.