

# **Process Change Notification**

PCN Number: PCN-2015-25 PCN Notification Date: 12/02/2015

#### **FINAL**

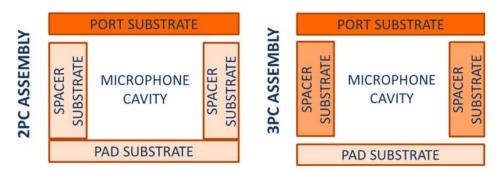
WM7121PIMSE/RV package assembly change

Dear Customer,

This notification is to advise you of the following change(s).

WM7121PIMSE/RV package assembly is changing from a 2-piece construction to a 3-piece construction.

- No change to the assembly house which remains Amkor Philippines.
- No change to package dimensions, part performance or reliability.
- Change to substrate vendor (existing qualified supplier to Amkor).
- Modified assembly flow to account for package changing from 2pc to 3pc type.



If you have any questions, please contact your Sales Representative.

Sincerely,

Quality Systems Administrator Cirrus Logic Corporate Quality Phone: +1(512) 851-4000



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#### **Products Affected:**

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

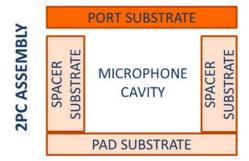
Technical details of this Process / Product Change follow on the next page(s).

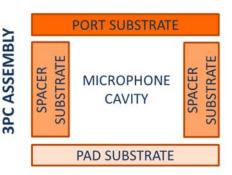
Title	e:	WM7121PIMSE/RV package assembly change							
Customer Contact: Local Field Sales R		Representative Phone:		1.512.851.40	000	Dept:	Sales		
Proposed 1 <sup>st</sup> Ship Date:		02 2	02 2016 Estimated Sample Availa		ability Date: 11 2015				
Change Type:					-			·	
	Assembly Site		X Assembly Process			Assembly Materials			
	Wafer Fab Site		Wafer Fab Process			Wafer Fab Materials			
	Wafer Bump Site		Wafer Bump Process		SS		Wafer Bump Material		
	Test Site	e Test		Test Proce	st Process			Design	
	Electrical Specifica	ation	Mechanical Specification		cation		Part Number		
	Packing/Shipping/	Labeling	Other						
Comments: The MMC produc			ct ma	rking will cha	nge fror	n DAP to AAA	\		

#### **PCN Details**

#### **Description of Change:**

Modified assembly flow to account for package changing from 2pc to 3pc type.





The MMC product marking will change from DAP to AAA

#### Reason for Change:

WM7121P package design is now several years old and is assembled using legacy processes. This change will enable turn-key construction at Amkor simplifying the supply chain and assembly process.

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<b>Anticipated Im</b>	pact on Form	, Fit, Function.	Quality	or Reliability:

There will be no impact from this change.

## **Product Affected:**

Device	Cirrus Logic Part Number	Customer Part Number
1	WM7121PIMSE/RV	

## **Changes To Product Identification Resulting From This PCN:**

The MMC product marking will change from DAP to AAA

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The Qualification Plans are designed using JEDEC and other applicable industry standards. The interim qualification report created following 168 hours of testing has been summarized below. The final report will be released in November following completion of testing.

#### **Silicon Level Tests**

Stress Test	Test Conditions	JESD22 Spec	Pre- condition	Test Duration	Fails/Passes (Lot)
High Temperature Operating Life (HTOL) testing	105°C V1= 3.7V Bias	A108	-	1000 hours	0/39*(1)
Low Temperature Operating Life (LTOL) testing	-40°C V1= 3.7V Bias	A108	-	1000 hours	0/40 (2)
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	>= Class 2 ESD pulse of 2000V HBM	A114	-	-	0/3 (2)
Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)	>= Class B ESD pulse of 200V MM	A115	-	•	0/3 (2)
IC Latch-Up Test	Class II Level A +/-100mA Current Injection and 1.5xMax Vsupply Overvoltage	JESD78	-	-	0/3 (2)

#### **Package Level Tests**

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Stress Test	Test Conditions	JESD22 Spec	Pre- condition	Test Duration	Fails/Passes (Lot)
High Temperature Storage (HTS) testing	150°C No bias	A103	-	168 hours	0/40 (3)
Low Temperature Storage (LTS) testing	-40°C No bias	A119	-	168 hours	0/40 (3)
Temperature & Humidity (TH) testing	85°C / 85% R.H. No bias	N/A	(a)	168 hours	0/40 (3)
Temperature, Humidity & Bias (THB) testing	85°C/85%RH V1= 3.7 V Bias	A101	(a)	168 hours	0/40 (3)
Moisture Sensitivity Level (MSL) testing	MSL 2A (Peak IR reflow temperature = 260°C)	J-STD-020	-	-	0/40 (3)

Pre-condition: JEDEC Moisture Sensitivity Level 2A (JESD22 - A113)

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<sup>\*</sup>Sample size reduced due to mechanical damage unrelated to the stress



# Reliability Engineering Interim Qualification Report

# **WM7121P**

Wafer Fabrication – X-fab Dresden, Magnachip GF3
Package Assembly – Amkor P3, 4 pin LGMA 3 pcs laminate package

Approved:	Dan Liu Sanjar Reliability Engineer	Date :	2/10/15
Approved:	Dan Liu, Senior Reliability Engineer  Russell McMillan, Senior Reliability Engineer	Date :	2/10/15
Approved:	Gary Morton, Manager of Supply Chain PTE	Date :	2/10/15.
Approved:	Andrew McLean, Director of Quality		2/10/15.
		Issue:	1.0

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## **Summary**

The WM7121P device is being tested to Cirrus product qualification requirements.

The silicon level reliability was qualified by similarity to the WM7121 device and 7121P (2pcs laminate).

#### Silicon level reliability

- 1000 hours of High Temperature Operating Life (HTOL) testing.
- 1000 hours of Low Temperature Operating Life (LTOL) testing.
- Electrostatic Discharge (ESD) testing.
- Latch-Up testing.

## Package level reliability

- 168 hours of High Temperature Storage (HTS) testing.
- 168 hours of Low Temperature Storage (LTS) testing.
- 168 hours of Temperature & Humidity (TH) testing.
- 168 hours of Temperature, Humidity & Bias (THB) testing.
- Moisture Sensitivity Level (MSL) testing at MSL2A.

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# **Reliability Test Results**

**Test Lots:** (1) Lot: 49770C (44ABDAP)

(2) Lot: 38851 (28AAGRD) (3) Lot: 425095 (57BWAAA)

## **Silicon Level Tests**

Stress Test	Test Conditions	JESD22 Spec	Pre- condition	Test Duration	Fails/Passes (Lot)
High Temperature Operating Life (HTOL) testing	105°C V1= 3.7V Bias	A108	-	1000 hours	0/39*(1)
Low Temperature Operating Life (LTOL) testing	-40°C V1= 3.7V Bias	A108	-	1000 hours	0/40 (2)
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	>= Class 2 ESD pulse of 2000V HBM	A114	-	•	0/3 (2)
Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)	>= Class B ESD pulse of 200V MM	A115	-	•	0/3 (2)
IC Latch-Up Test	Class II Level A +/-100mA Current Injection and 1.5xMax Vsupply Overvoltage	JESD78	-	-	0/3 (2)

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# Package Level Tests

Stress Test	Test Conditions	JESD22 Spec	Pre- condition	Test Duration	Fails/Passes (Lot)
High Temperature Storage (HTS) testing	150°C No bias	A103	-	168 hours	0/40 (3)
Low Temperature Storage (LTS) testing	-40°C No bias	A119	-	168 hours	0/40 (3)
Temperature & Humidity (TH) testing	85°C / 85% R.H. No bias	N/A	(a)	168 hours	0/40 (3)
Temperature, Humidity & Bias (THB) testing	85°C/85%RH V1= 3.7 V Bias	A101	(a)	168 hours	0/40 (3)
Moisture Sensitivity Level (MSL) testing	MSL 2A (Peak IR reflow temperature = 260°C)	J-STD-020	-	-	0/40 (3)

<sup>(</sup>a) Pre-condition: JEDEC Moisture Sensitivity Level 2A (JESD22 – A113)

# **Revision History**

Revision	Date	Originator	Change
1.0	02/10/2015	Dan Liu	Initial release

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<sup>\*</sup>Sample size reduced due to mechanical damage unrelated to the stress