Process Change Notification

PCN Number: PCN-2016-51 **PCN Notification Date:** 09/28/2016

Initial PCN

STATS ChipPAC* Probe, Assembly, Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA

Dear Customer,

This is notification of the STATS ChipPAC* Probe, Assembly, Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA. STATS ChipPAC* was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015. All assets will be consolidating to the JCET site location in Jiangyin CHINA targeted for the end of Q1_2017.

The described change(s) within this PCN will not take effect (i.e. Shipped) any earlier than **90** days from Initial PCN notification or the successful completion of the Cirrus Logic qualification, unless a customer agreement has been reached on an earlier implementation of the identified process change.

Cirrus Logic requests acknowledgement of receipt for this Initial PCN notification within 30 calendar days and acceptance of the identified change(s) within 90 days from receipt. Shipment of said material will commence after the 90 day period or upon successful completion of the Cirrus Logic defined qualification; lack of acknowledgement / communication is considered as acceptance.

Cirrus Logic would like to take this opportunity to thank our customers for their cooperation and assistance in this respective matter. Any specific or immediate inquiries should be directed to your local Field Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

* - STATS ChipPAC was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015.

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Products Affected:

The devices listed on subsequent pages are the complete list of affected devices. According to our records, one or more of these devices have been purchased by your organization within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:	STATS ChipPAC* Probe, Assembly, Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA						
Customer Contact:	Local Field Sales Representative		**Phone:**	(512) 851-4000		**Dept:**	Corporate Quality
Proposed 1st Ship Date:	Q1_2017		**Estimated Sample Availability Date:**				Q1_2017
Change Type:	Site Transfer: Change Type = Major, but considered Minor; as the subcontractor (STATS ChipPAC*) is an existing qualified supplier for Cirrus Logic and there are no changes to the equipment or material.						
X	Assembly Site		Assembly Process			Assembly Materials	
	Wafer Fab Site		Wafer Fab Process			Wafer Fab Materials	
	Wafer Bump Site		Wafer Bump Process			Wafer Bump Material	
X	Test Site		Test Process			Design	
	Electrical Specification		Mechanical Specification			Part Number	
X	Packing/Shipping/Labeling	X	Other				
Comments:	Wafer Probe						

PCN Details

Description of Change:

Cirrus Logic is qualifying the STATS ChipPAC* Probe, Assembly, Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA.

Below you will find an outline of the described changes for these components:

Special Note: Change Type = Major, but considered Minor.
The subcontractor (STATS ChipPAC*) is an existing qualified supplier and all material as well as equipment associated with the Probe, Assembly, Test and Final Pack processes will not change.

- **Probe, Assembly, Test and Final Pack Site Change:**

  From: **STATS ChipPAC* site location in Shanghai CHINA**
  To: **STATS ChipPAC* site location in Jiangyin CHINA**

Reason for Change:

STATS ChipPAC* was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015. All assets will be consolidating to the JCET site location in Jiangyin CHINA targeted for the end of Q1_2017.

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Special Note:

Earlier production level material may be available from the qualified Jiangyin CHINA site location, but shipment(s) from Cirrus Logic are contingent on successful qualification completion of the designated site transfer.

Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No anticipated adverse impact to the Quality and/or Reliability of said product; as the transfer site is part of an already existing Cirrus Logic qualified subcontractor STATS ChipPAC* and there are no changes to the equipment or material.

Product Affected:

Cirrus Logic Part Number(s):

CS8952-CQZ[R]/F
CS8952-IQZ[R]/F

Changes To Product Identification Resulting From This PCN:

There is "NO CHANGE" to the external face of the designated components.
Below is a 2D representative image of the Package: MF (Mark Format) = 190 Rev A

TOP SIDE BRAND
Logo Lines (Crystal Lan Logo, Crystal Logo)
LINE 1 (PART NUMBER, 14 SPACES MAX)
LINE 2 (DATE CODE, 14 SPACES MAX.)

Probe Site Qualification Plan

The Probe Site Correlation involves the following:

- Test and collection of data on the same material from the 3 independent lots at SCC (Shanghai CHINA) and JSCC (Jiangyin CHINA)

Detail Description	# of Lots	Qty per Lot (units)	Failure Criteria / Notes	Results (Pass / Fail)
Data log Correlation of critical measures	3	1 Wafer / Lot	Allowable variance < 10%	
Gage R & R	---	---	All system variances are explained	

Family Qualification Data:

This qualification has been specifically developed for the validation of this change. The qualification data validates that the proposed change meets the applicable released technical specifications.				
Qualification Schedule	**Start:**	Sep 2016	**End:**	Dec 2016

Qualification Device Family Construction Details				
Detail Description	**Device 1**	**Device 2**	**Device 3**	**Device 4**
Part Number(s):	CS4243x-xMZ[R]/x	CS43x5[A]-xQZ[R]/Bx	CS425xx-xQZ[R]/D	CS8900A-xQ[3]Z[R]/H
Wafer Fab Site Code/Name:	YF / YG (MagnaChip)	YF (MagnaChip)	YF (MagnaChip)	YF (MagnaChip)
Wafer Technology:	350 nm	250 nm	350 nm	500 nm
Die Size:	28.650 mm	7.952 mm	22.287 mm	20.339 mm
Assembly Site Code/Name:	BB (STATS ChipPAC*) Jiangyin CHINA	BB (STATS ChipPAC*) Jiangyin CHINA	BB (STATS ChipPAC*) Jiangyin CHINA	BB (STATS ChipPAC*) Jiangyin CHINA
Package Type/Code:	52L MQFP	48L QFP	64L QFP	100L QFP

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The Qualification Plans are designed using JEDEC and other applicable industry standards. An overall summary of the Qualification results will be submitted upon completion.

Package Level Qualification Plan

Purpose
STATS ChipPAC* Package level Qualification for Assembly Site Transfer from Shanghai to Jiangyin CHINA

Stress Name	Stress Method	Conditions	# of Lots	Qty per Lot	Read Points	Failure Criteria	Results (PASS/FAIL)
PC (Pre-Condition)	JESD22-A113 Per component MSL classification per J-STD-020	Bake: 24Hr +125'C; MSL 3 192Hr 30'C / 60% RH Soak, (Reflow 260'C x 3)	6	Sufficient for stress test coverage	Precon MSL3	0 fails	
TC (Temperature Cycle)	JEDEC JESD22-A104	-65°C to +150°C/ 1000 Cycles Post Precondition	6	77	1000 Cycles	0 fails	
THB (Temperature- Humidity-Bias)	JEDEC JESD22-A101	85°C/85% RH/1000 Hrs Post Pre-Condition	6	77	1000 Hrs	0 fails	
UHAST (Unbiased HAST)	JEDEC JESD22-A118	+110'C/85% RH, 17.7 PSIA, 264Hrs Post Pre-condition	6	77	264 Hrs	0 fails	
HTSL (High Temperature Storage Life)	JEDEC JESD22-A103	+150°C for 1000Hrs	5	45	1000 Hrs	0 fails	
WBP (Wire Bond Pull)	MIL-STD-883 M2011	Paragraph 3 of Reference Specification Table 1 Figure 2011-2	6			0 fails	
WBS (Wire Bond Shear)	JESD22-B116	Paragraph 4 (Procedure)	6			0 fails	
SD (Solderability)	J-STD-002		6		95% coverage	0 fails	
PPD (Package Physical Dimensions)	JESD22 B100 + B108	Package outline per JESD95 Cpk > 1.50 per JESD95	6	10	Meet all case outline drawing tolerances	No deviations from package drawing	

Notes:

- Qualification tests "pass" on zero fails for each test

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Test Site Qualification Plan

Purpose
STATS ChipPAC* Test Site Transfer from Shanghai to Jiangyin CHINA

The Equipment Platform Technology, Hardware and Software remain the same.
The Visual / Mechanical inspection and Tape and Reel operations are compliant to JEDEC industry standards.

The Test Equipment Correlation involves the following:

- Running the new site program with an OPEN Socket (No Unit) to ensure “All” tests fail.
- Serializing Control (Known Good) Units and testing the material on both test platforms (Existing and New Location) at all applicable test temperatures utilizing the same load-board and test site(s). A correlation comparison will be made on “All” individual components. If there is a concern or a discrepancy exists, a bench level correlation will be performed to ensure new site meets data sheet requirements.
- Performing Bin yield and Bin movement correlation by running samples at the existing Shanghai (SCC) site and at new Jiangyin site (JSCC). The results from each site will be compared.
- Running (the same) sample non-continuity failures (different failing tests) and testing them at the existing site and at the new site. All units are expected to fail at the new site location.
- Performing GR&R (Gauge Repeatability & Reproducibility)

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Final Pack Review and Results

Purpose
STATS ChipPAC* Final Pack Site transfer from Shanghai to Jiangyin CHINA

Lead Inspection: Sample lot run

ESD Management System: Compliant to ANSI / ESD S20.20 and ISO/TS16949: 2009 Standard Requirements

Final Pack Criteria Representative Flow: (Example Only)

Final Pack Label Formatting: (Example Only)

Final Pack Representative Label: (Example Only)

Final Pack Drop Test Methodology and Results: Compliant to EIA-481 and ISTA 2A

Methodology:

Success Criterion:

Results Summary: