

PCN Number: PCN-2017-88 PCN Notification Date: 01/16/2018

# Informational PCN: Amended ver. 2.0

ANST Site 24LD TSSOP High Density Lead Frame Change

Dear Customer,

This notification is to advise you of the following ANST Site 24LD TSSOP High Density Lead Frame change(s).

The described change(s) within this PCN will not take effect (i.e. Ship) any earlier then 60 days from this notification. Cirrus Logic has already successfully completed the qualification of this change.

Cirrus Logic would like to take this opportunity to thank our customers for their cooperation and support in this respective matter.

If you have any questions, please contact your Sales Representative.

Sincerely,

**Quality Systems Administrator** Cirrus Logic Corporate Quality Phone: +1(512) 851-4000

\* Note: Amended for inclusion of "[R]" in all part numbers to support Tape N

Reeled Material.

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### **Products Affected:**

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:		ANST Site 24LD TSSOP High Density Lead Frame Change							
Customer Contact: Local Field Sales			s Representative		Phone: (512) 851-400		Dept:	Corporate Quality	
Proposed 1st Ship Date:			NA Estimated Sample			e Availability Date: NA			
Cha	nge Type:								
	Assembly Site		Χ	Assembly Process		Χ	Assembly Materials		
	Wafer Fab Site			Wafer Fab Process			Wafer Fab Materials		
	Wafer Bump Site			Wafer Bump Process			Wafer Bump Material		
	Test Site			Test Process			Design		
	Electrical Specification			Mechanical Specification			Part Number		
	Packing/Shipping/Labeling			Other					
Comments: 24LD TSSOP Lead Frame Vendor									

## **PCN Details**

## **Description of Change:**

Vendor Change:

From: QPL To: Poongson

Strip Size: (Reference Appendix A)

From: 50units / Strip To: 128 units / Strip

DIE Pad Size:

From: 0.118" x 0.165" To: 0.120" x 0.180"

Frame Process Methodology

From: Etched To: Stamped

Trim/Form Tool

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To: GPM/GMP-SE From: HANMI/HTS-AF01

### Reason for Change:

The existing process is outdated being brought current to ensure overall quality and maintain continuity of supply.

### Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No anticipated adverse impact to the Quality and/or Reliability of said product; as the process migration being performed is in an effort to ensure and maintain the level of overall quality by bring the processes current and in line with today's level of processing.

Special Note: There are no changes to the BOM (Bill of Material).

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	No Impact to the Material Declaration		Material Declarations or Product Content reports are driven from production data and will be available following the production release.			
Produc	ct Affected:					
	Device	Cirrus Logic Part Number				
	1	CS4270-xZZ[R]/C0				
	2	CS5351-xZZ[R]/E				
	3	CS5361-xZZ[R]/E				
	4	CS5363-DZZ[R]/E				
	5	CS4349-xZZ[R]/C2				
	6	CS4350-xZZ[R]/C2				
	7	CX4350-DZZ[R]/C2				
	8	CS5381-KZZ[R]/D				

# **Changes To Product Identification Resulting From This PCN:**

The Cirrus Logic component symbolization on the external face of the device reflects the designated Assembly Site.

There is "NO CHANGE" to the external face of the designated components.

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The Qualification Plans are designed using JEDEC and other applicable industry standards. An overall summary of the Qualification results will be submitted upon completion.

# Qualification

CS5363-DZZ[R] DZZ[R]/C2 & C	]/E, CS4350- S5381-KZZ[R]/D	Qualification:  Plan  Test Results						
Reliability Test	Standard	Conditions	# of Lots	Qty/ Lot	Read Point(s)	Fail Criteria	Results (PASS/FAIL)	
WBP MIL-STD-883 (Wire Bond Pull) Method 2011		Paragraph 3 (Procedure) 30 Bonds	1 lot / Device	5	Pre- Encapsulation	0 fails	Pass	
WBS (Wire Bond JESD22-B116 Shear)		Paragraph 4 (Procedure) 30 Bonds	1 lot / Device	5	Pre- Encapsulation	0 fails	Pass	
SD (Solderability) JESD22-B102		93°C / 8 Hr steam age and then 245°C solder bath / 5 seconds before SD		15	Solderability	0 fails	Pass	
ED (Electrical Distribution)	JESD86A	Parametric limits per datasheet or user spec	1 lot / Device	5	Zero Hours	0 fails	Pass	
Pre-Conditioning	JESD22-A113	24 Hr Bake, 192Hr -30℃/ 60%RH Soak, 3x 260℃ Peak Reflow	1 lot / Device	200	Pre-Con MSL3	0 fails	Pass	
Temperature Cycle	JESD22- A104	Condition C -65°C to +150°C / Air to Air / Post Pre-Condition 500 Cycles	1 lot / Device	80	500 Cycles	0 fails	Pass	
Tomography	J-STD_035	C-SAM	1 lot / Device	22, 22, 22	Zero Hrs, Pre-Condition, TC 500 Cycles	0 fails, 0 fails, 0 fails	Pass	
uHAST	JESD22-A118	130°C/85%RH Post Precondition	1 lot / Device	80	96 hours	0 fails	Pass	
Notes: The CS4270-xZZ[R]/C0, CS5351-xZZ[R]/E, CS5361-xZZ[R]/E, CS4349-xZZ[R]/C2 & CX4350-DZZ[R]/C2 material is QBS (Qualified By Similarity).  Reliability Qualification Results:  • Qualification tests "pass" on zero fails for each test								

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Appendix A: Lead Frame Strip Comparison

