CHANGE NOTIFICATION



June 05, 2015

Dear Sir/Madam:

PCN# 060515

Subject: Notification of Change to LTC2410 LTC2411/LTC2411-1, LTC2412, LTC2413, LTC2414/LTC2418, LTC2415/LTC2415-1 Datasheet

Please be advised that Linear Technology Corporation has made a change to the datasheet specifications of subject devices in order to improve device manufacturability.

The Maximum External Oscillator Frequency (f_{EOSC}) in the Timing Characteristics is being reduced from 2000 kHz to 500 kHz. There are many applications that are using the parts at 2000 kHz and the performance is perfectly adequate. But at 2000 kHz, performance is significantly reduced from the limits guaranteed in the specification table, as shown in the graphs at the end of the datasheet.

This change is intended to apply to future customer designs. No changes are being made to the circuit or the test methodology, so customers that are using these devices with FO frequencies between 500 kHz and 2000 kHz and are satisfied with performance will continue to receive the same product.

Should you have any further questions or concerns please contact your local Linear Technology Sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at <u>JASON.HU@LINEAR.COM</u>. If I do not hear from you by August 05, 2015, we will consider this change to be approved by your company.

Sincerely,

Jason Hu Quality Assurance Engineer

TIMING CHARACTERISTICS The • denotes specifications which apply over the full operating temperature

SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
feosc	External Oscillator Frequency Range		•	2.56	500) - 2000 -	kHz
t _{HEO}	External Oscillator High Period		•	0.25		390	μs
t _{LEO}	External Oscillator Low Period		•	0.25		390	μs
tcowv	Conversion Time	F ₀ = 0V F ₀ = V _{CC} External Oscillator (Note 11)	•	130.86 157.03 205	133.53 160.23 510/f _{EOSC} (in	136.20 163.44 kHz)	ms ms ms
fisck	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 f _{EOSC} /8		kHz kHz
DISCK	Internal SCK Duty Cycle	(Note 10)	•	45		55	%
f _{esck}	External SCK Frequency Range	(Note 9)	•			2000	kHz
t _{lesck}	External SCK Low Period	(Note 9)	•	250			ns
t _{HESCK}	External SCK High Period	(Note 9)	•	250			ns
t _{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	•	1.64 25	1.67 56/f _{EOSC} (in k	1.70 Hz)	ms ms
tdout_esck	External SCK 32-Bit Data Output Time	(Note 9)	•	3	2/f _{ESCK} (in kl	Hz)	ms
t ₁	$\overline{CS} \downarrow$ to SDO Low Z		•	0		200	ns
t2	CS ↑ to SDO High Z		•	0		200	ns
t3	$\overline{CS} \downarrow$ to SCK \downarrow	(Note 10)	•	0		200	ns
t4	$\overline{CS} \downarrow$ to SCK \uparrow	(Note 9)	•	50			ns
t _{komax}	SCK ↓ to SDO Valid		•			220	ns
t _{KOMIN}	SDO Hold After SCK ↓	(Note 5)	•	15			ns
t ₅	SCK Set-Up Before CS ↓		•	50			ns
t ₆	SCK Hold After CS ↓		•			50	ns

range, otherwise specifications are at $T_A = 25^{\circ}C$. (Note 3)

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified.

 $V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$; $V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: Fo pin tied to GND or to VCC or to external conversion clock source with fEOSC = 153600Hz unless otherwise specified. Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization hand

Note 7: Fo = 0V (internal oscillator) or fEOSC = 153600Hz ±2% (external oscillator).

Note 8: Fo = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is fESCK and is expressed in kHz. Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the

SCK pin has a total equivalent load capacitance CLOAD = 20pF. Note 11: The external oscillator is connected to the Fo pin. The external

oscillator frequency, fEOSC, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

 $F_0 = 0V \text{ or } F_0 = V_{CC}$

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.



TIMING CHARACTERISTICS The • denotes specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
feosc .	External Oscillator Frequency Range		•	2.56	500	-2800-	kHz
1 _{HEO}	External Oscillator High Period		•	0.25		390	μs
t _{leo}	External Oscillator Low Period		•	0.25		390	μs
tCONV	Conversion Time	$ \begin{array}{l} F_0 = 0 V \; (LTC2411) \\ F_0 = V_{CC} \; (LTC2411) \\ F_0 = 0 V \; (LTC2411-1) \\ External \; Oscillator \; (Note \; 11) \end{array} $	••••	130.86 157.03 143.78 205	133.53 160.23 146.71 i10/f _{EOSC} (in	136.20 163.44 149.64 kHz)	ms ms ms
f _{ISCK}	Internal SCK Frequency	Internal Oscillator (LTC2411) (Note 10) Internal Oscillator (LTC2411-1) (Note 10) External Oscillator (Notes 10, 11)		19.2 17.5 f _{EOSC} /8			kHz kHz kHz
DISCK	Internal SCK Duty Cycle	(Note 10)	٠	45		55	%
1ESCK	External SCK Frequency Range	(Note 9)	•			2000	kHz
LESCK	External SCK Low Period	(Note 9)		250			ns
THESCK	External SCK High Period	(Note 9)	•	250			ns
t _{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (LTC2411) (Notes 10, 12) Internal Oscillator (LTC2411-1) (Notes 10, 12) External Oscillator (Notes 10, 11)	••••	1.64 1.80 25	1.67 1.83 i6/f _{EOSC} (in k	1.70 1.86 Hz)	ms ms ms
TDOUT_ESCK	External SCK 32-Bit Data Output Time	(Note 9)	•	3	2/fesck (in kl	łz)	ms
t ₁	CS ↓ to SDO Low Z		•	0		200	ns
t2	CS ↑ to SDO High Z			0		200	ns
13	CS ↓ to SCK ↓	(Note 10)	•	0		200	ns
t4	CS ↓ to SCK ↑	(Note 9)		50			ns
t _{KOMAX}	SCK ↓ to SDO Valid		•			220	ns
tkomin	SDO Hold After SCK J	(Note 5)	•	15			ns
t ₅	SCK Set-Up Before CS ↓		•	50			ns
te	SCK Hold After CS ↓		•			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified.

 $V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$; $V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: Fo pin tied to GND or to V_{CC} or to external conversion clock source with fEOSC = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Fo = 0V (internal oscillator) or fEOSC = 153600Hz ±2% (external oscillator).

Note 8: $F_0 = V_{CC}$ (internal oscillator) or $f_{EOSC} = 128000 \text{Hz} \pm 2\%$ (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is fESCK and is expressed in kHz. Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the

SCK pin has a total equivalent load capacitance CLOAD = 20pF.

Note 11: The external oscillator is connected to the FD pin. The external oscillator frequency, fFOSC, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

 $F_0 = 0V \text{ or } F_0 = V_{CC}.$

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: Fo = 0V (internal oscillator) or fEDSC = 139800Hz ±2% (external oscillator).



TIMING CHARACTERISTICS The • denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25$ °C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
feosc	External Oscillator Frequency Range		•	2.56	50	0 -2000-	kHz
t _{HEO}	External Oscillator High Period		•	0.25		390	μs
t _{LEO}	External Oscillator Low Period		•	0.25		390	μS
tCONV	Conversion Time	F _O = 0V F _O = V _{CC} External Oscillator (Note 11)	•	130.86 157.03 205	133.53 160.23 510/f _{EOSC} (in	136.20 163.44 kHz)	ms ms ms
fisck	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 f _{EOSC} /8		kHz kHz
DISCK	Internal SCK Duty Cycle	(Note 10)	•	45		55	%
f _{ESCK}	External SCK Frequency Range	(Note 9)	•			2000	kHz
t _{lesck}	External SCK Low Period	(Note 9)	•	250			ns
tHESCK	External SCK High Period	(Note 9)	•	250			ns
t _{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	:	1.64 25	1.67 56/f _{EOSC} (in k	1.70 (Hz)	ms ms
tDOUT_ESCK	External SCK 32-Bit Data Output Time	(Note 9)	•	3	2/f _{ESCK} (in k	ms	
t ₁	CS ↓ to SDO Low Z		•	0		200	ns
t2	CS ↑ to SDO High Z		•	0		200	ns
t3	$\overline{CS} \downarrow$ to SCK \downarrow	(Note 10)	•	0		200	ns
t4	$\overline{CS} \downarrow$ to SCK \uparrow	(Note 9)	•	50			ns
t _{KOMAX}	SCK ↓ to SD0 Valid		•			220	ns
t _{KOMIN}	SDO Hold After SCK ↓	(Note 5)	•	15			ns
t ₅	SCK Set-Up Before CS ↓		•	50			ns
t ₆	SCK Hold After CS ↓		•			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.

VREF = REF* - REF*, VREFCM = (REF* + REF*)/2; VIN = IN* - IN*, VINCM = (IN+ + IN⁻)/2, IN+ and IN⁻ are defined as the selected positive (CH0⁺ or CH1⁺) and negative (CH0⁻ or CH1⁻) input respectively.

Note 4: Fo pin tied to GND or to Voc or to external conversion clock source with fEOSC = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Fo = 0V (internal oscillator) or fEOSC = 153600Hz ±2% (external oscillator).

Note 8: $F_0 = V_{CC}$ (internal oscillator) or $f_{EOSC} = 128000$ Hz $\pm 2\%$ (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is fESCK and is expressed in kHz. Note 10: The converter is in internal SCK mode of operation such that

the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance CLOAD = 20pF.

Note 11: The external oscillator is connected to the Fo pin. The external oscillator frequency, fEOSC, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

 $F_0 = 0V \text{ or } F_0 = V_{CC}$

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.



TIMING CHARACTERISTICS The e denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
fEOSC	External Oscillator Frequency Range		•	2.56	50	0 - 2000 -	kHz
t _{HEO}	External Oscillator High Period		•	0.25		390	μs
tLEO	External Oscillator Low Period		•	0.25		390	μs
t _{CONV}	Conversion Time	F ₀ = 0V External Oscillator (Note 10)	•	20	146.71 510/f _{EOSC} (ir	ı kHz)	ms ms
f _{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9) External Oscillator (Notes 9, 10)			17.5 f _{EOSC} /8		kHz kHz
DISCK	Internal SCK Duty Cycle	(Note 9)	•	45		55	%
f _{ESCK}	External SCK Frequency Range	(Note 8)	•			2000	kHz
t _{lesck}	External SCK Low Period	(Note 8)	•	250			ПS
t _{HESCK}	External SCK High Period	(Note 8)	•	250			ns
t _{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11) External Oscillator (Notes 9, 10)	•	1.80 2	1.83 56/f _{EOSC} (in	1.86 kHz)	ms ms
t _{dout esck}	External SCK 32-Bit Data Output Time	(Note 8)	•	2	32/f _{ESCK} (in k	Hz)	ms
t ₁	CS ↓ to SDO Low Z		•	0		200	ns
t2	CS ↑ to SD0 Hi-Z		•	0		200	ns
t3	$\overline{CS} \downarrow$ to SCK \downarrow	(Note 9)	•	0		200	ns
t4	CS ↓ to SCK ↑	(Note 8)	•	50			ns
t _{KOMAX}	SCK ↓ to SDO Valid		•			220	ns
t _{KOMIN}	SD0 Hold After SCK ↓	(Note 5)	•	15			пs
t ₅	SCK Set-Up Before CS ↓		•	50			ns
t ₆	SCK Hold After CS ↓		•			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified. V_{REF} = REF⁺ - REF⁻, V_{REFCM} = (REF⁺ + REF⁻)/2;

 $V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: Fo pin tied to GND or to external conversion clock source with fEOSC = 139800Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Fo = 0V (internal oscillator) or fEOSC = 139800Hz ±2% (external oscillator).

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is fESCK and is expressed in kHz. Note 9: The converter is in internal SCK mode of operation such that

the SCK pin is used as digital output. Note 10: The external oscillator is connected to the Fo pin. The external

oscillator frequency, fEOSC, is expressed in kHz. Note 11: The converter uses the internal oscillator. $F_0 = 0V$.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.



DIGITAL INPUTS AND DIGITAL OUTPUTS The \bullet denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Vol	Low Level Output Voltage SDO	I ₀ = 1.6mA	•			0.4	V
VoH	High Level Output Voltage SCK	I ₀ = -800μA (Note 10)	•	V _{CC} - 0.5			V
Vol	Low Level Output Voltage SCK	I ₀ = 1.6mA (Note 10)	•			0.4	V
l _{oz}	Hi-Z Output Leakage SDO		•	-10		10	μA

POWER REQUIREMENTS The \bullet denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{CC}	Supply Voltage		٠	2.7		5.5	V
Icc	Supply Current Conversion Mode Sleep Mode Sleep Mode	$\frac{\overline{CS}}{\overline{CS}} = 0V \text{ (Note 12)}$ $\frac{\overline{CS}}{\overline{CS}} = V_{CC} \text{ (Note 12)}$ $\overline{CS} = V_{CC}, 2.7V \le V_{CC} \le 3.3V \text{ (Note 12)}$	•		200 4 2	300 10	μА μΑ μΑ

TIMING CHARACTERISTICS The \bullet denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
feosc	External Oscillator Frequency Range		٠	2.56	50	0 2000	kHz
t _{HEO}	External Oscillator High Period		٠	0.25		390	μs
t _{LEO}	External Oscillator Low Period		٠	0.25		390	μs
t _{conv}	Conversion Time	$F_0 = 0V$ $F_0 = V_{CC}$ External Oscillator (Note 11)	:	130.86 157.03 205	133.53 160.23 i10/f _{EOSC} (in	136.20 163.44 kHz)	ms ms ms
fisck	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 f _{EOSC} /8		kHz kHz
DISCK	Internal SCK Duty Cycle	(Note 10)	٠	45		55	%
f _{ESCK}	External SCK Frequency Range	(Note 9)	•			2000	kHz
t _{lesck}	External SCK Low Period	(Note 9)	٠	250			ns
t _{HESCK}	External SCK High Period	(Note 9)	٠	250			ns
tdout_isck	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	•	1.64 25	1.67 6/f _{EOSC} (in k	1.70 (Hz)	ms ms
tDOUT_ESCK	External SCK 32-Bit Data Output Time	(Note 9)	٠	3	2/f _{ESCK} (in kl	Hz)	ms





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LTC2415/LTC2415-1

TIMING CHARACTERISTICS The • denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
feosc	External Oscillator Frequency Range		•	2.56	500	2000	kHz
theo	External Oscillator High Period		•	0.25		390	μs
t _{LEO}	External Oscillator Low Period		•	0.25		390	μs
t _{CONV}	Conversion Time (LTC2415)	$F_0 = 0V$ $F_0 = V_{CC}$ External Oscillator (Note 11)	•	65.43 78.52 102	66.77 80.12 278/f _{EOSC} (in	68.1 81.72 kHz)	ms ms ms
	Conversion Time (LTC2415-1)	F ₀ = 0V External Oscillator (Note 11)	•	71.3 102	72.8 78/f _{EOSC} (in	74.3 kHz)	ms ms
f _{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10), LTC2415 Internal Oscillator (Note 10), LTC2415-1 External Oscillator (Notes 10, 11)			19.2 17.5 f _{EOSC} /8		kHz kHz kHz
DISCK	Internal SCK Duty Cycle	(Note 10)	•	45		55	%
fesck	External SCK Frequency Range	(Note 9)	٠			2000	kHz
t _{lesck}	External SCK Low Period	(Note 9)	٠	250			ns
t _{HESCK}	External SCK High Period	(Note 9)	•	250			ns
t _{dout_isck}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12), LTC2415 Internal Oscillator (Notes 10, 12), LTC2415-1 External Oscillator (Notes 10, 11)	•	1.64 1.80 25	1.67 1.83 6/f _{EOSC} (in k	1.70 1.86 Hz)	ms ms ms
tDOUT_ESCK	External SCK 32-Bit Data Output Time	(Note 9)	•	3	2/f _{ESCK} (in kH	łz)	ms
t ₁	CS ↓ to SDO Low Z		•	0		200	ns
t2	CS ↑ to SDO High Z		•	0		200	ns
t3	CS ↓ to SCK ↓	(Note 10)	•	0		200	ns
t4	CS ↓ to SCK ↑	(Note 9)	•	50			ns
t _{komax}	SCK \downarrow to SDO Valid		•			220	ns
t _{каміл}	SDO Hold After SCK \downarrow	(Note 5)	٠	15			ns
t ₅	SCK Set-Up Before $\overline{\text{CS}}\downarrow$		•	50			ns
t ₆	SCK Hold After CS ↓		•			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND. Note 3: $V_{CC} = 2.7$ to 5.5V unless otherwise specified. $V_{REF} = REF^+ - REF^-, V_{REFCM} = (REF^+ + REF^-)/2;$

 $V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: Fo pin tied to GND or to V_{CC} or to external conversion clock source with fEOSC = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F₀ = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: Fo = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is fESCK and is expressed in kHz. Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance CLOAD = 20pF.

Note 11: The external oscillator is connected to the Fo pin. The external oscillator frequency, fEOSC, is expressed in kHz.

Note 12: The converter uses the internal oscillator.

 $F_0 = 0V \text{ or } F_0 = V_{CC}$

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Refer to Offset Accuracy and Drift in the Applications Information section.





Confidential Statement This change notice is for Linear Technology's Customers only. Distribution or notification to third parties is prohibited.