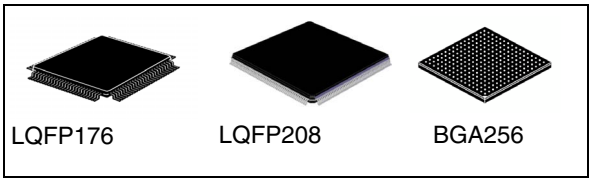
SPC564Bxx
SPC56ECxx

32-bit MCU family built on the Power Architecture® for automotive body electronics applications

Data brief

Features

- e200z4d, 32-bit Power Architecture®
  - up to 120MHz and 200MIPs operation
- e200z0h, 32-bit Power Architecture
  - up to 80MHz and 75MIPs operation
- Memory
  - Up to 3MByte on-chip Flash with ECC
  - Up to 256KByte on-chip SRAM with ECC
  - 64KByte on-chip Data Flash with ECC
  - 16-entry memory protection unit (MPU)
  - User selectable Memory BIST
- Interrupts
  - 255 interrupt sources with 16 priority levels
  - Up to 54 ext. IRQ including 30 wake-up
- GPIOs: from 147 (QFP176) to 199 (BGA256)
- System timer units
  - 8-ch. 32-bit periodic interrupt timer (PIT)
  - 4-channel 32-bit system timer (STM)
  - Safety System Watchdog Timer (SWT)
  - Real-time clock timer (RTC/API)
- eMIOS, 16-bit counter timed I/O units
  - Up to 64 channels with PWM/MC/IC/OC
- Two ADC (10-bit and 12-bit)
  - Up to 62 channels extendable to 90 ch.
  - Multiple Analog Watchdog
- Dedicated diagnostic features for lighting
  - Advanced shifted PWM generation
  - ADC conversion synchronized on PWM
- Communication interfaces
  - Up to 6 FlexCAN with 64 buffers each
  - Up to 10 LINFlex/UART channels
  - Up to 8 buffered DSPI channels
  - I^2C interface
  - One FleyRay (dual-ch.) with 128 buffers
  - Fast Ethernet Controller
- Cryptographic Services Engine (CSE)



  - AES-128 en/decryption, CMAC auth.
  - Secured device boot mode
- 32-ch. eDMA with multiple request sources
- Clock generation
  - 4 to 40 MHz main oscillator
  - 16 MHz internal RC oscillator
  - Software-controlled FMPLL
  - 128 kHz internal RC oscillator
  - 32 kHz auxiliary oscillator
  - Clock Monitoring Unit (CMU)
- Low power capabilities
  - Ultra low power STANDBY
  - CAN Sampler to store CAN ID in STBY
  - Fast wake-up and execute from RAM
- Exhaustive debugging capability
  - Nexus 3+ interface on LBGA256 only
  - Nexus 1 on all devices
- Voltage supply
  - Single 5 V or 3.3 V supply
  - On-chip V_{reg} with external ballast transitor
- Operating temperature range -40 to 125 °C

Contents

List of tables

List of figures

1 Introduction

1.1 Document overview

This document provides an overview and describes the features of the SPC564Bxx and SPC56ECxx series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. For electrical specifications, pin assignments, and package diagrams, refer to the device data sheet.

1.2 Description

The 32-bit SPC564Bxx and SPC56ECxx automotive microcontrollers are a family of System-on-Chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, high end gateway, smart junction box, front module and combined body controller and gateway applications.

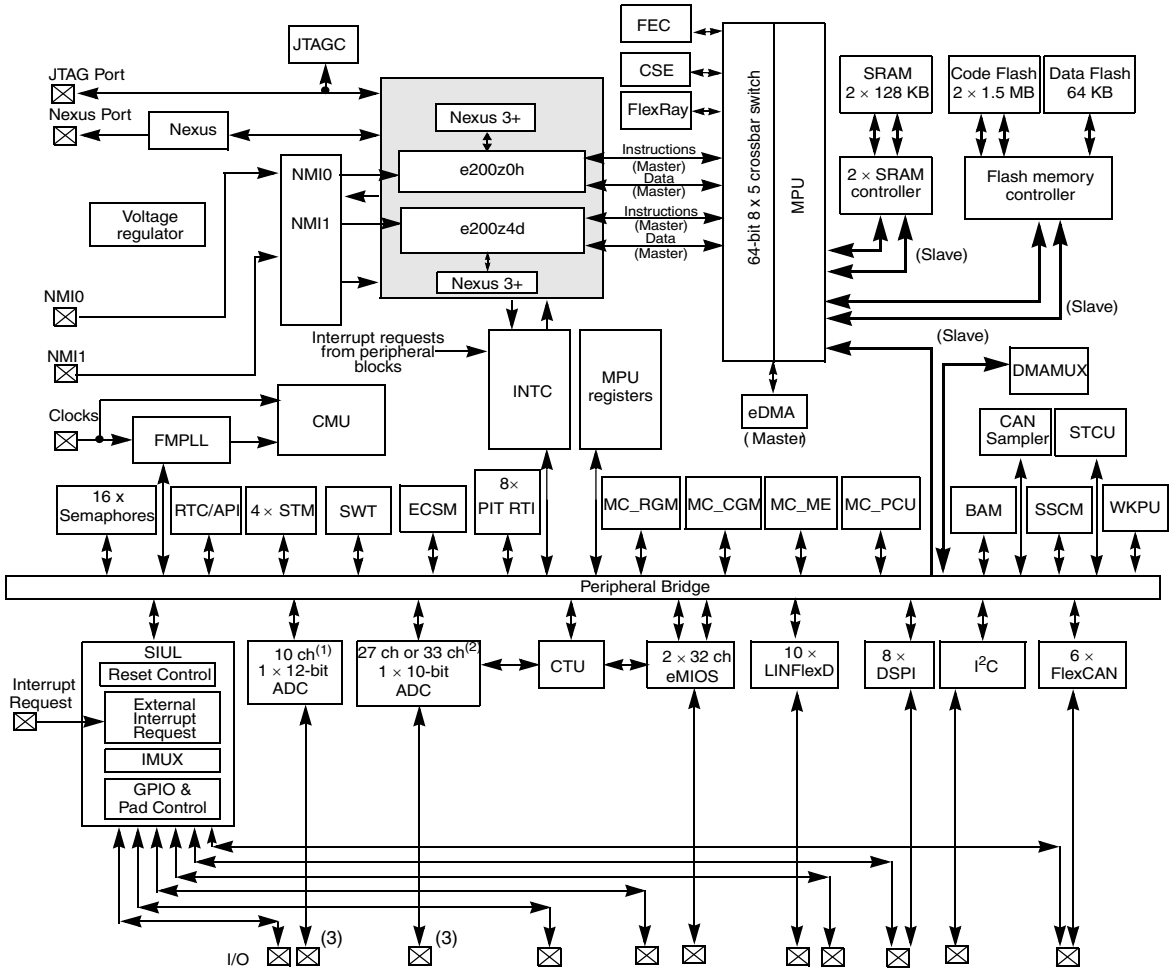
The SPC564Bxx and SPC56ECxx family is one of a series of next-generation automotive microcontrollers based on the Power Architecture® architecture and designed specifically for embedded automotive applications. This document describes the features of the SPC564Bxx and SPC56ECxx family and highlights important electrical and physical characteristics of the devices.

The advanced and cost-efficient host processor core of the SPC564Bxx and SPC56ECxx automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original Power Architecture user instruction set architecture (UISA). It operates at speeds of up to 120 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and will be supported with software drivers, operating systems and configuration code to assist with user implementations.

2 Block diagram

Figure 1 shows a top-level block diagram of the SPC564Bxx and SPC56ECxx family.

Figure 1. SPC564Bxx and SPC56ECxx block diagram



Legend:

ADC	Analog-to-Digital Converter	JTAGC	JTAG controller
BAM	Boot Assist Module	LINFlexD	Local Interconnect Network Flexible with DMA support
CSE	Cryptographic Services Engine	MC_ME	Mode Entry Module
CAN	Controller Area Network (FlexCAN)	MC_CGM	Clock Generation Module
CMU	Clock Monitor Unit	MC_PCU	Power Control Unit
CTU	Cross Triggering Unit	MC_RGM	Reset Generation Module
DMAMUX	DMA Channel Multiplexer	MPU	Memory Protection Unit
DSPI	Deserial Serial Peripheral Interface	Nexus	Nexus Development Interface
eDMA	enhanced Direct Memory Access	NMI	Non-Maskable Interrupt
FlexCAN	Controller Area Network controller modules	PIT_RTI	Periodic Interrupt Timer with Real-Time Interrupt
FEC	Fast Ethenet Controller	RTC/API	Real-Time Clock/ Autonomous Periodic Interrupt
eMIOS	Enhanced Modular Input Output System	SIUL	System Integration Unit Lite
ECSM	Error Correction Status Module	SRAM	Static Random-Access Memory
FMPLL	Frequency-Modulated Phase-Locked Loop	SSCM	System Status Configuration Module
FlexRay	FlexRay Communication Controller	STM	System Timer Module
I2C	Inter-integrated Circuit Bus	SWT	Software Watchdog Timer
IMUX	Internal Multiplexer	STCU	Self Test Control Unit
INTC	Interrupt Controller	WKPU	Wakeup Unit

Notes:
1) 10 dedicated channels plus up to 19 shared channels. See the device-comparison table.
2) Package dependent. 27 or 33 dedicated channels plus up to 19 shared channels. See the device-comparison table.
3) 16 x precision channels (ANP) are mapped on input only I/O cells.

3 Application examples

3.1 Introduction

The SPC564Bxx and SPC56ECxx is designed to address central body, smart junction box, front module and high end gateway or combined body controller and gateway applications within the vehicle. As shown in the following examples, the MCU is central to the application and provides the flexibility to add or remove peripheral components in a modular design.

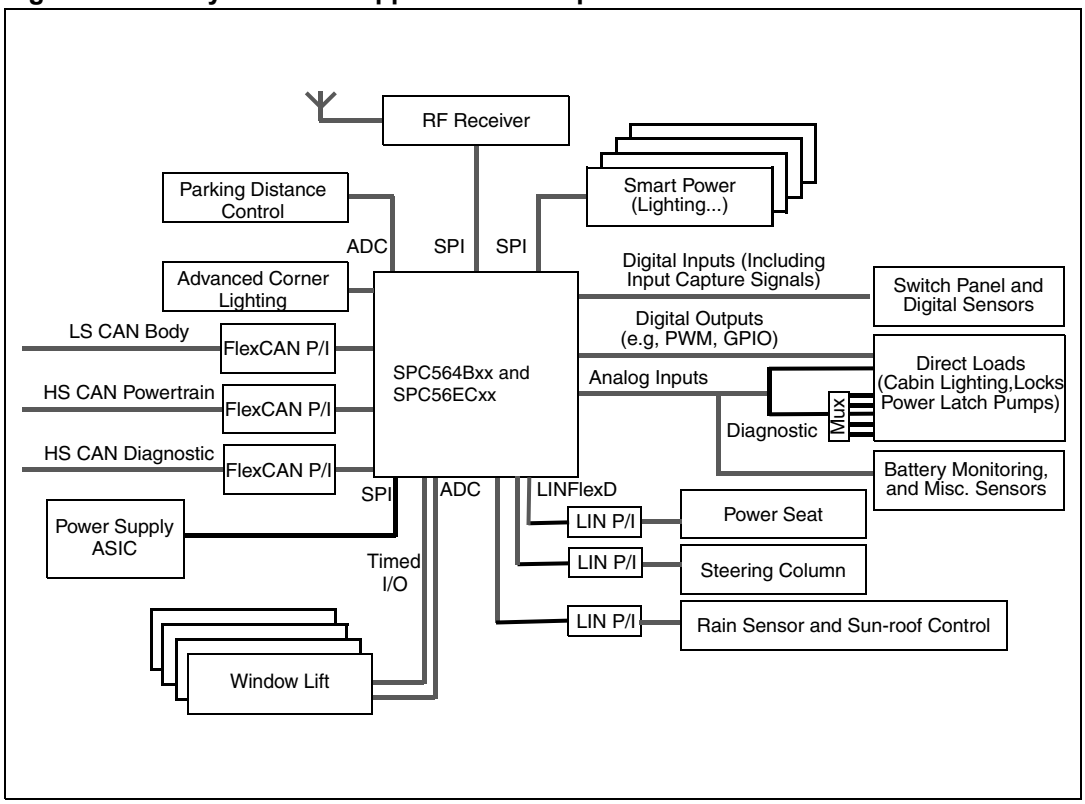
3.2 Body controller application example

Body controller modules primarily control the following:

- Comfort features—doors, seats, interior lighting
- Security/access features—passive entry, immobilizer, TPMS
- Lighting—headlights, brake lights, turn lights
- Centralized diagnostic and network management
- Vehicle communications network routing—CAN, FlexRay, Ethernet

Figure 2 shows the SPC564Bxx and SPC56ECxx used in a typical body controller application.

Figure 2. Body controller application example



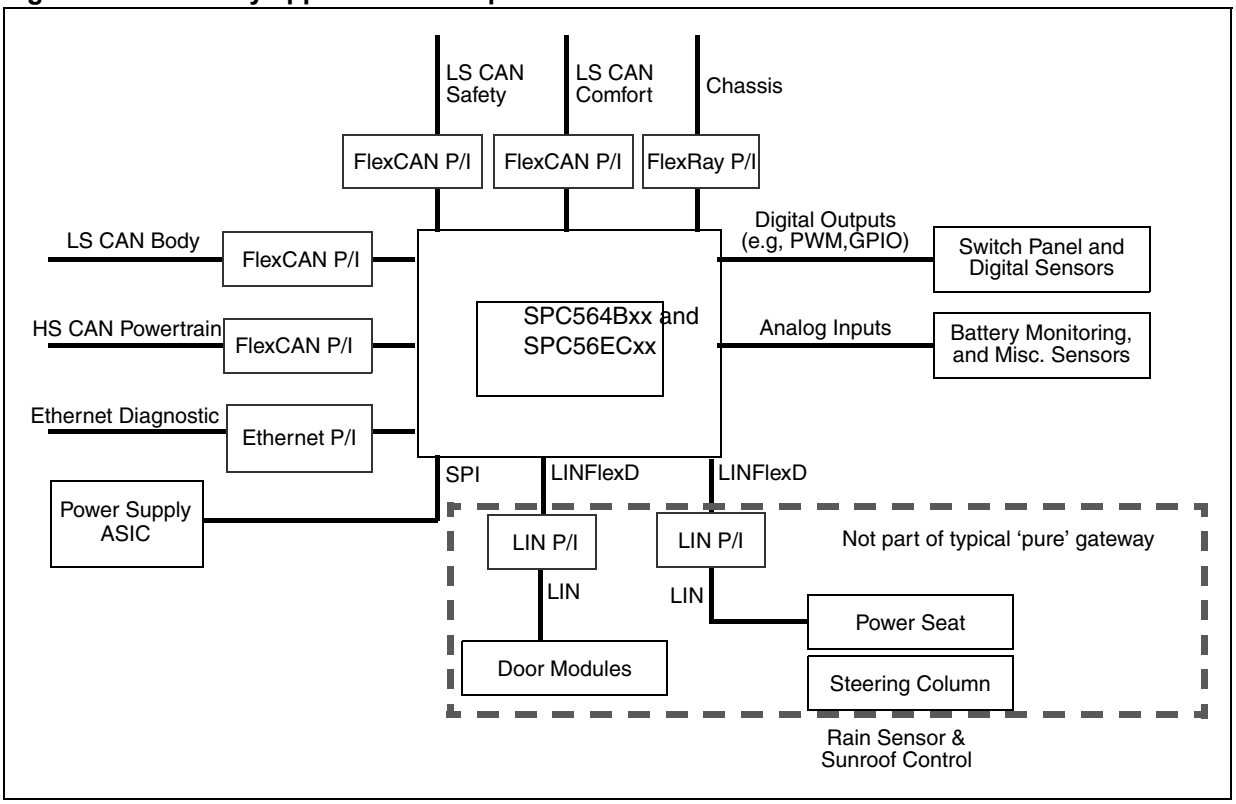
3.3 Gateway application example

Gateway controller modules primarily control the inter-bus communications necessary to pass information between the multiple communications busses with in the vehicle:

- CAN communications—Dominant vehicle bus within automotive comfort and body
- FlexRay— High bandwidth bus used to support time critical communications for safety related network communications with redundancy and high bandwidth data transfer
- Ethernet— High speed diagnostics, vehicle programing
- LIN— Low bandwidth sub-bus communications

Figure 3 shows the SPC564Bxx and SPC56ECxx used in a gateway application controller.

Figure 3. Gateway application example



4 Device family overview

4.1 Introduction

This section provides a comparison of the different SPC564Bxx and SPC56ECxx family members, presents the critical performance parameters, low power operation and lists the chip-level features and the flash memory module details.

Table 1 provides a summary of the different members of the SPC564Bxx and SPC56ECxx family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family.

Table 1. SPC564Bxx and SPC56ECxx family comparison[1]

Feature	SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256
CPU	e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h			e200z4d		e200z4d + e200z0h		
Execution speed[2]	Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]			Up to 120 MHz (e200z4d)		Up to 120 MHz (e200z4d) Up to 80 MHz (e200z0h)[3]		
Code flash memory	1.5 MB					2 MB					3 MB				
Data flash memory	4 x16 KB														
SRAM	128 KB		192 KB			160 KB		256 KB			192 KB		256 KB		
MPU	16-entry														
eDMA[4]	32 ch														
10-bit ADC															
dedicated[5], [6]	27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch		27 ch	33 ch	27 ch	33 ch	
shared with 12-bit ADC[7]	19 ch														
12-bit ADC															
dedicated[8]	10 ch														
shared with 10-bit ADC[7]	19 ch														
CTU	64 ch														
Total timer I/O[9] eMIOS	64 ch, 16-bit														
SCI (LINFlexD)	10														
SPI (DSPI)	8														
CAN (FlexCAN)[10]	6														
FlexRay	Yes														

Table 1. SPC564Bxx and SPC56ECxx family comparison(1) (continued)

Feature	SPC564B64		SPC56EC64			SPC564B70		SPC56EC70			SPC564B74		SPC56EC74		
Package	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256	LQFP 176	LQFP 208	LQFP 176	LQFP 208	BGA 256
STCU(11)	Yes														
Ethernet	No		Yes			No		Yes			No		Yes		
I^2C	1														
32 kHz oscillator (SXOSC)	Yes														
GPIO(12)	147	177	147	177	199	147	177	147	177	199	147	177	147	177	199
Debug	JTAG				Nexus3+	JTAG				Nexus3+	JTAG				Nexus3+
Cryptographic Services Engine (CSE)	Optional														

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature and subject to full device characterisation.
3. The e200z0h can run at speeds up to 80 MHz. However, if system frequency is >80 MHz (e.g., e200z4d running at 120 MHz) the e200z0h needs to run at 1/2 system frequency. There is a configurable e200z0 system clock divider for this purpose.
4. DMAMUX also included that allows for software selection of 32 out of a possible 57 sources.
5. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
6. There are 23 dedicated ANS plus 4 dedicated ANX channels on LQPF176. For higher pin count packages, there are 29 dedicated ANS plus 4 dedicated ANX channels.
7. 16x precision channels (ANP) and 3x standard (ANS).
8. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
9. As a minimum, all timer channels can function as PWM or Input Capture and Output Control. Refer to the eMIOS section of the device reference manual for information on the channel configuration and functions.
10. CAN Sampler also included that allows ID of CAN message to be captured when in low power mode.
11. STCU controls MBIST activation and reporting.
12. Estimated I/O count for proposed packages based on multiplexing with peripherals.

4.2 Critical performance parameters

The critical performance parameters of the SPC564Bxx and SPC56ECxx feature the following:

- Fully static design operation up to a maximum of 120 MHz + 2%, 150 °C junction. This is based on 125 °C ambient.
- Low power design
  - Designed for dynamic power management of core and peripherals
  - Software-controlled clock gating of peripherals
  - Multiple power domains to minimize leakage in low power modes
- Internal voltage regulator (V_{REG}) enables control with a single input voltage for device operation with the following features:
  - Regulates 3.3 V to 5 V(± 10%) input to generate all internal low power supplies.
  - Voltage regulator (V_{REG}) for regulation of input supply and all internal voltages. Requires external ballast transistor.
  - Manages power gating
  - Low power regulators support operation when in STOP and STANDBY modes to minimize power consumption
  - Startup on-chip regulators in <50 µs for rapid exit of STOP and STANDBY modes
  - Low voltage detection on main supply and 1.2 V regulated supplies.
- ADC analog supply 3.3–5 V ±10%
- Configurable I/O domains supporting Ethernet bank and general I/O bank
- Configurable pins
  - Selectable pull-up, pull-down, or no pull on all GPIO pins
  - Selectable open-drain pin
- Frequency modulated phase-locked loop
- –40 to 125 °C ambient operating temperature range

Table 2. Current consumption target(1), (2)

Mode	Condition(3)	Typical(4)	Max(5)
RUN	25 °C, 120 MHz	175 mA(6),(7)	240 mA7,(8)
	25 °C, 80 MHz	110 mA6	150 mA8
HALT	25 °C	25 mA	35 mA
STOP	25 °C	400 µA7	1200 µA7
STANDBY1 (8 KB RAM retained)	25 °C	25 µA	75 µA
STANDBY2 (64 KB RAM retained)	25 °C	45 µA	135 µA
STANDBY3 (96 KB RAM retained)	25 °C	60 µA	175 µA

1. Values are preliminary and subject to change during characterization.
2. All values are package dependant due to thermal constraints.
3. All temperatures are based on an ambient temperature.
4. Target typical current consumption for the following typical operating conditions and configuration. Process = Typical, Voltage = 1.2 V.
5. Target maximum current consumption for mode observed under typical operating conditions. Process = Fast, Voltage= 1.32 V.
6. Subject to change, Configuration: 1 ¥ e200z4d + 4 kbit/s Cache, 1 ¥ eDMA (32 ch), 4 ¥ FlexCAN (2 ¥ 500 kbit/s, 2 ¥ 125 kbit/s), 10 ¥ LINFlexD (20 kbit/s), 8 ¥ DSPI (4 ¥ 2 Mbit/s, 3 ¥ 4 Mbit/s, 1 ¥ 10 Mbit/s), 40 ¥ PWM (200 Hz), 40 ¥ ADC Input, 1 ¥ CTU (40 ch), 1 ¥ FlexRay (2 ch, 10 Mbit/s), 1 ¥ RTC, 4 ¥ PIT, 1 ¥ SWT, 1 ¥ STM. Ethernet and e200z0h disabled. Also reduced timed I/O channels for smaller packages. RUN current measured with typical application with accesses on both code flash memory and RAM.
7. This value is obtained from limited sample set.
8. Subject to change, Configuration: 1 ¥ e200z4d + 4 kbit/s Cache, 1 ¥ e200z0h (1/2 system frequency), CSE, 1 ¥ eDMA (10 ch), 6 ¥ FlexCAN (4 ¥ 500 kbit/s, 2 ¥ 125 kbit/s), 4 ¥ LINFlexD (20 kbit/s), 6 ¥ DSPI (2 ¥ 2 Mbit/s, 3 ¥ 4 Mbit/s, 1 ¥ 10 Mbit/s), 16 ¥ Timed I/O, 16 ¥ ADC Input, 1 ¥ FlexRay (2 ch, 10 Mbit/s), 1 ¥ FEC (100 Mbit/s), 1 ¥ RTC, 4 ¥ PIT, 1 ¥ SWT, 1 ¥ STM. For lower pin count packages reduce the amount of timed I/O's and ADC channels. RUN current measured with typical application with accesses on both code flash memory and RAM.

Table 3. Operating mode summary(1)

Operating modes	Device feature				Clock sources					RTC / APIr(2)	Wake-up inputs	V_{REG} modes		V_{REG} Start-up
	CPU Core(s)	Flash memory	RAM	Peripherals	PLL	16 MHz IRC	4-40 MHz OSC	128 kHz IRC	32 kHz XOSC			High-Power V_{REG}	Low-Power V_{REG}	V_{REG} start-up
RUN	On	OP	On	OP	OP	On	OP	On	OP	OP	—(3)	On	On	—
HALT	CG	OP	On	OP	OP	On	OP	On	OP	OP	OP	On	On	—
STOP	CG	CG	On	CG	Off	OP	OP	On	OP	OP	OP	OP	On	20 µs (4)
STANDBY1 (5)	Off	Off	8 KB (6)	Off	Off	OP	OP	OP	OP	OP	OP	Off	On	20 µs
STANDBY2[5]	Off	Off	64 KB (7)	Off	Off	OP	OP	OP	OP	OP	OP	Off	On	20 µs
STANDBY3[5]	Off	Off	96 KB (8)	Off	Off	OP	OP	OP	OP	OP	OP	Off	On	20 µs
POR	—	—	—	—	—	—	—	—	—	—	—	—	—	1.5 ms

1. Table Key:

   On—Powered and clocked

   OP—Optionally configurable to be enabled or disabled (clock gated)

CG—Clock gated, powered but clock stopped

   Off—Powered off and clock gated

FP—V_{REG} full performance mode

   LP—V_{REG} low power mode, reduced output capability of VREG but lower power consumption

Var—Variable duration, based on the required reconfiguration and execution clock speed

BAM—Boot Assist Module software and hardware used for device start-up and configuration

2. RTC runs through functional reset.
3. All wake-up pins are functional in RUN mode but wake-up has no meaning in this mode.
4. 20 µs startup time only when High-Power V_{REG} is OFF. If it is ON, V_{REG} startup time is <1us.
5. For any STANDBY mode, the device startup time is calculated based upon SRAM bootup after STANDBY exit.
6. 8 KB of the RAM contents is retained in STANDBY mode (but only accessible in RUN mode).
7. 64 KB of the RAM contents retained in STANDBY mode (but only accessible in RUN mode).
8. 96 KB of the RAM contents retained in STANDBY mode (but only accessible in RUN mode).

Table 4. Total device wakeup time

Mode	Total time
STOP mode with HPREG OFF and RAM wakeup	20 µs
STOP mode with HPREG OFF and flash memory Wakeup	55 µs
STOP mode with HPREG ON and RAM wakeup	<5 µs
STOP mode with HPREG ON and flash memory wakeup	35 µs
STANDBY with RAM wakeup	35 µs
STANDBY with flash memory wakeup	160 µs

4.3 Low power operation

The SPC564Bxx and SPC56ECxx has two dynamic power modes (RUN and HALT), and two static power modes. There is also the 'WAIT' instruction which allows either of the cores to be placed in WAIT:

- Low power modes use clock gating to halt the clock for all or part of the device.
- The lowest power mode also uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.
- Dynamic power modes RUNx:
  - Four dynamic RUN modes supported.
  - RUN modes are the main operating modes where the entire device can be powered and clocked and where most processing activity is done. The ability to configure and select different RUN modes allows different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions both simply and rapidly.
  - The necessary peripherals, clock sources, clock speed and systems clock prescalers can be independently configured for each of the four RUN modes of the device.
- WAIT command
  - WAIT allows the core to be frozen while most peripherals are allowed to continue to run. It can be entered directly by a core request (Wait For Interrupt, Wait For Event instructions) or indirectly by a core request (writing NVIC registers). As soon as an event or and interrupt is pending, the system returns to RUN mode within few system clock-cycles.
- Dynamic power mode HALT
  - HALT mode is a reduced activity low power mode intended for periods of moderate duration where less processing activity is needed. In this mode, the core clocks are stopped but user selected peripheral tasks can continue to run. It may be configured to provide more efficient power management features (switch-off PLL, flash, main regulator...) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.
- Static power mode STOP
  - STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than

the lowest STANDBY mode, with no need to reconfigure the device before starting to execute code. The clocks are halted to the cores and peripherals and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode, but not WAIT or HALT mode.

Wake-up from STOP mode is provided from an external event, or by the internal periodic wake-up, if enabled.

- Static power mode STANDBY
  - STANDBY mode halts the clock to the entire device and turns off the power to the majority of the chip in order to offer the lowest power consumption modes of the SPC564Bxx and SPC56ECxx. STANDBY mode means that the contents of the cores, on-chip peripheral registers and potentially some of the volatile memory are not held. The device can be awakened from up to 30 I/O pins, a reset, or from a periodic wake-up using a low power oscillator. If required by the user, it is possible to enable the internal 16 MHz or 128 kHz RC oscillator or external high frequency/low frequency oscillator.
  - STANDBY1 mode retains 8 KB of the on-chip RAM. Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM or flash memory on exit from low power modes.
  - STANBDY2 mode retains the 64 KB contents of the on-chip RAM.
  - STANBDY3 mode retains the 96 KB contents of the on-chip RAM.
- 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals through selection as the system clock.
- Supports operation of ADCs using internal 16 MHz RC oscillator.
- Internal 16 MHz RC oscillator can be used as the PLL input clock source to provide fast start-up without the external oscillator delay.
- Up to 30 external pins for wake-up from low power modes.
- Rapid exit from low power mode with fast startup internal voltage regulator.

4.4 Chip-level features

On-chip modules available within the family include the following features:

- e200z4d dual issue, 32-bit core Power Architecture® compliant CPU
  - Up to 120 MHz
  - 4 KB, 2/4-Way Set Associative Instruction Cache
  - Variable length encoding (VLE)
  - Embedded floating-point (FPU) unit
  - Supports Nexus3+
- e200z0h single issue, 32-bit core Power Architecture compliant CPU
  - Up to 80 MHz
  - Variable length encoding (VLE)
  - Supports Nexus3+
- Up to 3 MB on-chip flash memory: flash page buffers to improve access time
- Up to 256 KB on-chip SRAM
- 64 KB on-chip data flash memory to support EEPROM emulation
- Up to 16 semaphores across all slave ports
- User selectable MBIST
- Low-power modes supported: STOP, HALT, STANDBY
- 16 region Memory Protection Unit (MPU)
- Dual-core Interrupt Controller (INTC). Interrupt sources can be routed to e200z4d, e200z0h, or both
- Frequency-Modulated Phase-Locked Loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash memory, and SRAM from multiple bus masters
- 32 channel eDMA controller with DMAMUX
- Timer supports input/output channels providing 16-bit input capture, output compare, and PWM functions (eMIOS)
- 2 analog-to-digital converters (ADC): one 10-bit and one 12-bit
- Cross Trigger Unit (CTU) to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- Up to 8 serial peripheral interface (DSPI) modules
- Up to 10 serial communication interface (LINFlex) modules
- Up to 6 full CAN (FlexCAN) modules with 64 MBs each
- CAN Sampler to catch ID of CAN message
- 1 inter IC communication interface (I^2C) module
- Up to 177 (LQFP) or 199 (BGA) configurable general purpose I/O pins
- System clocks sources
  - 4–40 MHz external crystal oscillator
  - 16 MHz internal RC oscillator
  - FMPLL
    Additionally, there are two low power oscillators: 128 kHz internal RC oscillator, 32 kHz external crystal oscillator
- Real Time Counter (RTC) with clock source from internal 128 kHz or 16 MHz oscillators

or external 4–40 MHz crystal
  - Supports autonomous wake-up with 1 ms resolution with max timeout of 2 seconds
  - Optional support from external 32 kHz crystal oscillator, supporting wake-up with 1 second resolution and max timeout of 1 hour
- 1 System Timer Module (STM) with four 32-bit compare channels
- Up to 8 periodic interrupt timers (PIT) with 32-bit counter resolution
- 1 Real Time Interrupt (RTI) with 32-bit counter resolution
- 1 Safety Enhanced Software Watchdog Timer (SWT) that supports keyed functionality
- 1 dual-channel FlexRay Controller with 128 message buffers
- 1 Fast Ethernet Controller (FEC)
- On-chip voltage regulator (V_{REG})
- Cryptographic Services Engine (CSE)
- Offered in the following standard package types:
  - 176-pin LQFP, 24 × 24 mm, 0.5 mm Lead Pitch
  - 208-pin LQFP, 28 × 28 mm, 0.5 mm Lead Pitch
  - 256-ball LBGA, 17 × 17mm, 1.0 mm Lead Pitch

4.5 Flash memory details

The on-chip flash memory on the SPC564Bxx and SPC56ECxx features the following:

- 3 MB burst flash memory
- Single dual port flash memory controller and flash BIU shared with the data flash memory
- Flash memory partitioning:
  - 1.5 MB Code flash memory module 1:
    1 × 512 KB (2 × 16 KB, 3 × 32 KB, 3 × 128 KB, 2 × 16 KB (reserved))
    2 × 512 KB (4 × 128 KB)
  - 1.5 MB Code flash memory module 2:
    1 × 512 KB (2 × 16 KB, 3 × 32 KB, 3 × 128 KB, 2 × 16 KB (reserved))
    2 × 512 KB (4 × 128 KB)
  - 64 KB Data flash memory
    4 × 16 KB, 1 × 8 KB (reserved)
- RWW is supported between Code flash memory and Data flash memory modules, to facilitate the EEPROM emulation capability. RWW is not supported between the 512 KB arrays within the Code flash memory
- Typical Code flash memory access time is 40 ns: 0 wait-state for buffer hits, 5 wait-states for page buffer miss at 120+2% MHz
- Typical Data flash memory access time is 120 ns: up to 13 wait-states for page buffer miss at 120 + 2% MHz.
- Page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
- 64-bit ECC with single-bit correction, double-bit detection for data integrity in Code Flash, 32-bit ECC with single-bit correction, double-bit detection for data integrity in Data Flash.
- Censorship protection scheme to prevent flash memory content visibility
- Supports flash memory writes using internal 16 MHz RC oscillator
- Margin read for flash memory array supported for initial program verification

4.5.1 Flash memory partitioning

Table 5. SPC564Bxx and SPC56ECxx Flash memory partitioning

Array	Address	SPC564B64 / SPC56EC6	SPC564B70 / SPC56EC70	SPC564B74 / SPC56EC4
		1.5 MB	2 MB	3 MB
Array_A	Flash base + 0x0000_0000	32 KB	32 KB	32 KB
	Flash base + 0x0000_8000	16 KB	16 KB	16 KB
	Flash base + 0x0000_C000	16 KB	16 KB	16 KB
	Flash base + 0x0001_0000	32 KB	32 KB	32 KB
	Flash base + 0x0001_8000	32 KB	32 KB	32 KB
	Flash base + 0x0002_0000	128 KB	128 KB	128 KB
	Flash base + 0x0004_0000	128 KB	128 KB	128 KB
	Flash base + 0x0006_0000	128 KB	128 KB	128 KB
Array_B	Flash base + 0x0008_0000	128 KB	128 KB	128 KB
	Flash base + 0x000A_0000	128 KB	128 KB	128 KB
	Flash base + 0x000C_0000	128 KB	128 KB	128 KB
	Flash base + 0x000E_0000	128 KB	128 KB	128 KB
Array_C	Flash base + 0x0010_0000	128 KB	128 KB	128 KB
	Flash base + 0x0012_0000	128 KB	128 KB	128 KB
	Flash base + 0x0014_0000	128 KB	128 KB	128 KB
	Flash base + 0x0016_0000	128 KB	128 KB	128 KB

Table 5. SPC564Bxx and SPC56ECxx Flash memory partitioning (continued)

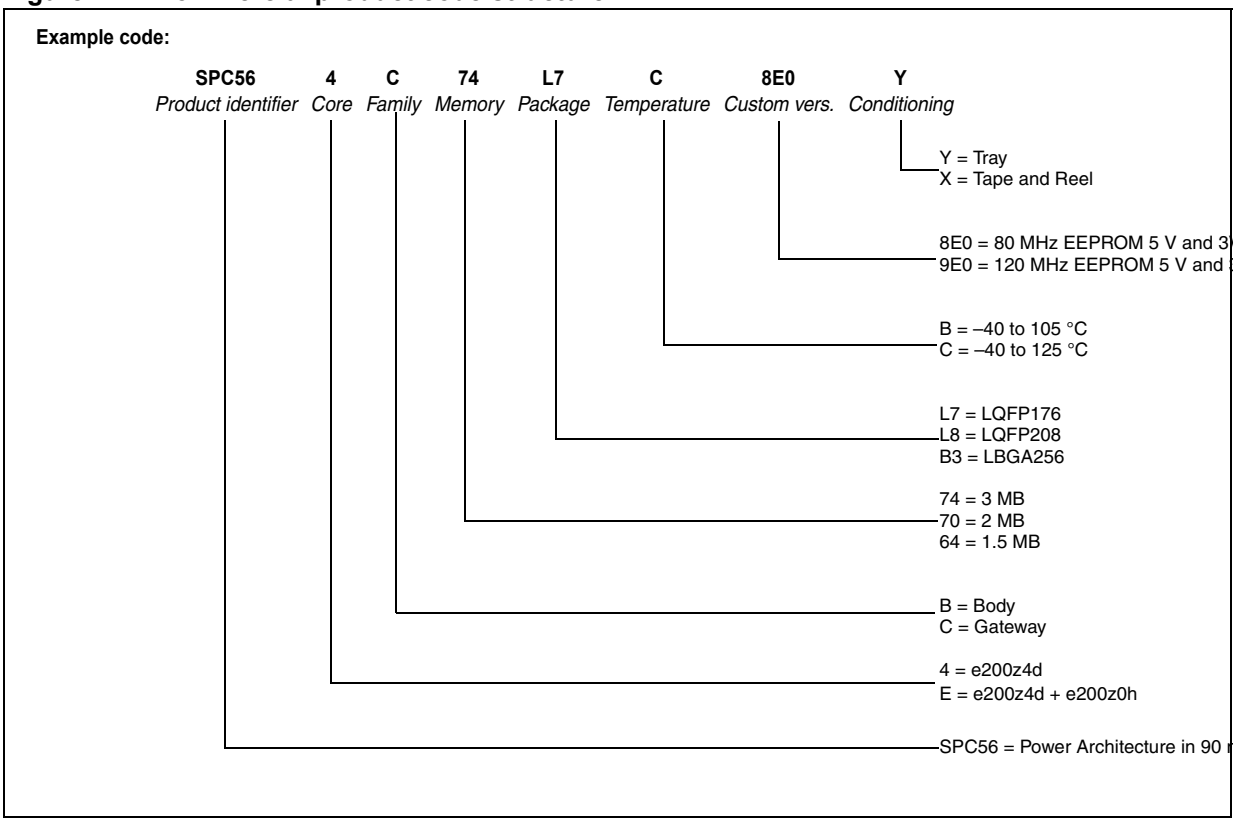
Array	Address	SPC564B64 / SPC56EC6	SPC564B70 / SPC56EC70	SPC564B74 / SPC56EC4
		1.5 MB	2 MB	3 MB
Array_D	Flash base + 0x0018_0000	—	128 KB	128 KB
	Flash base + 0x001A_0000	—	128 KB	128 KB
	Flash base + 0x001C_0000	—	128 KB	128 KB
	Flash base + 0x001E_0000	—	128 KB	128 KB
Array_E	Flash base + 0x0020_0000	—	—	128 KB
	Flash base + 0x0022_0000	—	—	128 KB
	Flash base + 0x0024_0000	—	—	128 KB
	Flash base + 0x0026_0000	—	—	128 KB
Array_F	Flash base + 0x0028_0000	—	—	32 KB
	Flash base + 0x0028_8000	—	—	16 KB
	Flash base + 0x0028_C000	—	—	16 KB
	Flash base + 0x0029_0000	—	—	32 KB
	Flash memory base + 0x0029_8000	—	—	32 KB
	Flash base + 0x002A_0000	—	—	128 KB
	Flash base + 0x002C_0000	—	—	128 KB
	Flash base + 0x002E_0000	—	—	128 KB

Table 5. SPC564Bxx and SPC56ECxx Flash memory partitioning (continued)

Array	Address	SPC564B64	SPC56EC6	SPC564B70	SPC56EC70	SPC564B74	SPC56EC4
		1.5 MB		2 MB		3 MB	
Array_G	Data flash base + 0x0000_0000	16 KB		16 KB		16 KB	
	Data flash base + 0x0000_4000	16 KB		16 KB		16 KB	
	Data flash base + 0x0000_8000	16 KB		16 KB		16 KB	
	Data flash base + 0x0000_C000	16 KB		16 KB		16 KB	

4.6 Ordering Information

Figure 4. Commercial product code structure



4.7 Developer environment

The SPC564Bxx and SPC56ECxx MCU family is supported by tools and third-party developers which offer a widespread, established network of tool and software vendors. It also features a high-performance Nexus debug interface.

The following development support are available:

- Automotive evaluation boards (EVB) featuring CAN, LIN interfaces, and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces

The following software support are available:

- OSEK solutions will be available from multiple third parties
- CAN and LIN drivers
- AUTOSAR package

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
01-Jul-2011	1	Initial release.
04-Jul-2011	2	– Made minor editing and formatting changes throughout the document to improve readability. – Figure 1: SPC564Bxx and SPC56ECxx block diagram: Replaced e200Z0h core nexus support from "nexus3" to "nexus3+". – Figure 2: Body controller application example: Added Power supply block, replaced LinFlex with LinFlexD. – Figure 3: Gateway Application Example: replaced LinFlex with LinFlexD. – Table 1: SPC564Bxx and SPC56ECxx Family Comparison: Replaced nexus 3 with nexus 3+ support for both the cores – Section 3.3: Critical performance parameters - Clarified feature 1 from "Fully static design operation up to a maximum of 120 MHz, based on 125 °C ambient" to "Fully static design operation up to a maximum of 120 MHz + 2%, 150 °C junction. This is based on 125 °C ambient" - Table 2: Current Consumption Target table: Editorial updates in footnote 6 and 7. – Section 3.5: Chip-level features: e200Z0h- Updated to show nexus 3+ debug support, listed low power modes. – Updated feature list. – SPC564Bxx and SPC56ECxx family comparison table: Updated ADC channels and added ADC footnotes. – Table 2. Current Consumption Target: Corrected RUN current max at 25 °C to 150 mA. Clarified footnote 6 and 7.
29-Jul-2011	3	– Updated block diagram – Updated family comparison table – Current Consumption Target table: Added HALT current values. – Operating Mode Summary table: Added footnote 4. Replaced OFF with OP for STOP mode at HPV_{REG}. – Flash memory detail section, simplified the module names. – Updated Commercial product code structure – Current consumption target table: Added footnote 7. – Flash memory details: Added 32-bit ECC with single-bit correction, double-bit detection for data integrity in Data Flash.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com