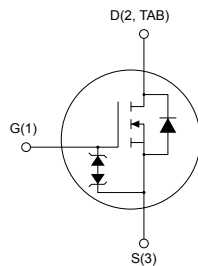


N-channel 600 V, 0.260 Ω typ., 12 A MDmesh M6 Power MOSFET in a DPAK package


DPAK


AM01479V1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD16N60M6	600 V	0.320 Ω	12 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



Product status

STD16N60M6

Product summary

Order code	STD16N60M6
Marking	16N60M6
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_c = 25\text{ }^\circ\text{C}$	12	A
I_D	Drain current (continuous) at $T_c = 100\text{ }^\circ\text{C}$	7.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
P_{TOT}	Total power dissipation at $T_c = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
3. $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	110	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$		0.260	0.320	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	575	-	pF
C_{oss}	Output capacitance		-	33	-	
C_{rss}	Reverse transfer capacitance		-	3	-	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0\text{ V}$	-	104	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 12\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	16.7	-	nC
Q_{gs}	Gate-source charge		-	3.5	-	
Q_{gd}	Gate-drain charge		-	9.4	-	

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 6\text{ A}, R_G = 4.7\text{ }\Omega,$ $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	13	-	ns
t_r	Rise time		-	7.6	-	
$t_{d(off)}$	Turn-off delay time		-	19.8	-	
t_f	Fall time		-	6.8	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 12\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	210		ns
Q_{rr}	Reverse recovery charge		-	1.7		μC
I_{RRM}	Reverse recovery current		-	13.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	310		ns
Q_{rr}	Reverse recovery charge		-	3.2		μC
I_{RRM}	Reverse recovery current		-	15.4		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

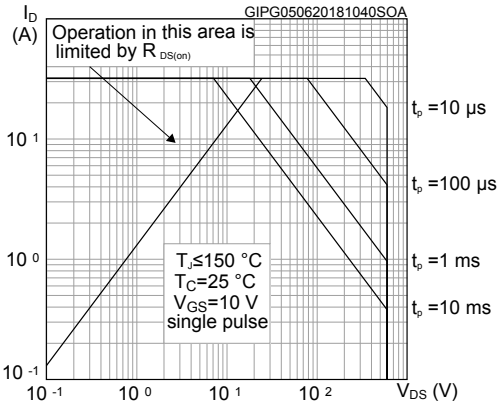


Figure 2. Thermal impedance

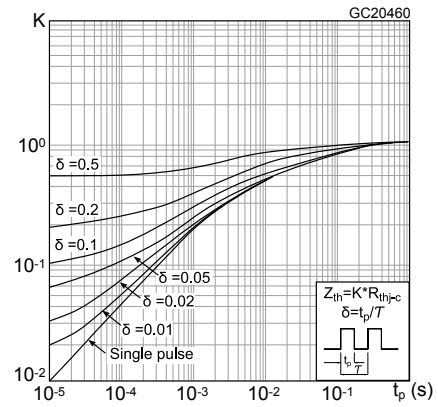


Figure 3. Output characteristics

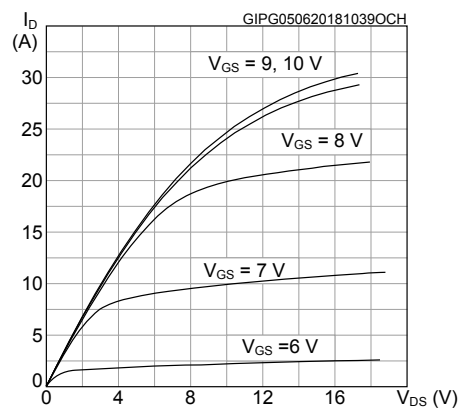


Figure 4. Transfer characteristics

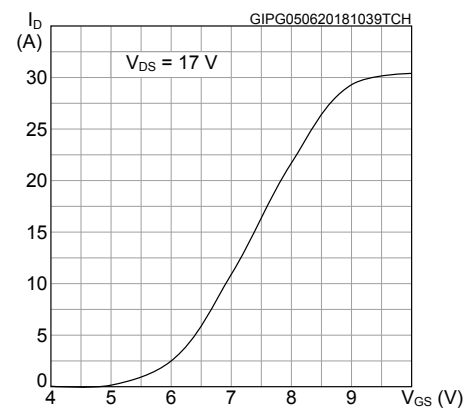


Figure 5. Gate charge vs gate-source voltage

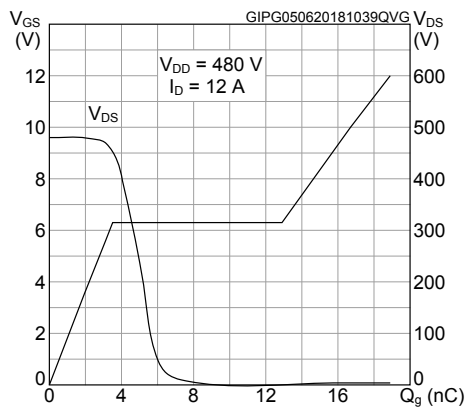


Figure 6. Static drain-source on-resistance

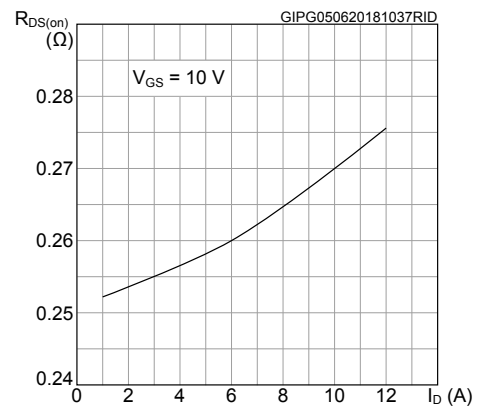


Figure 7. Capacitance variations

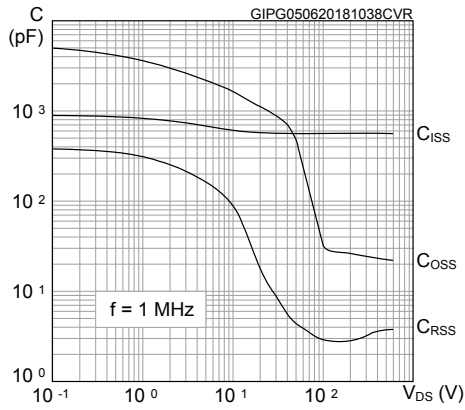


Figure 8. Normalized gate threshold voltage vs temperature

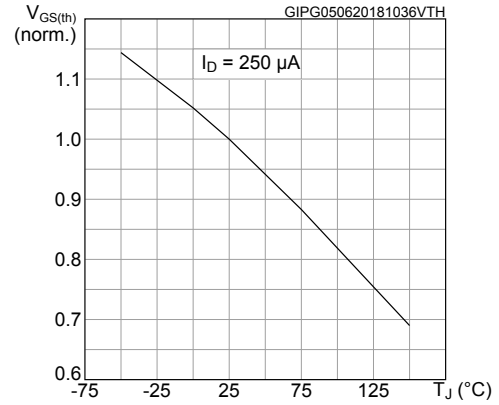


Figure 9. Normalized on-resistance vs temperature

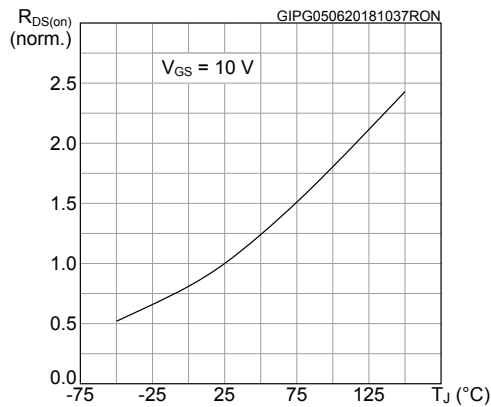


Figure 10. Normalized V_{(BR)DSS} vs temperature

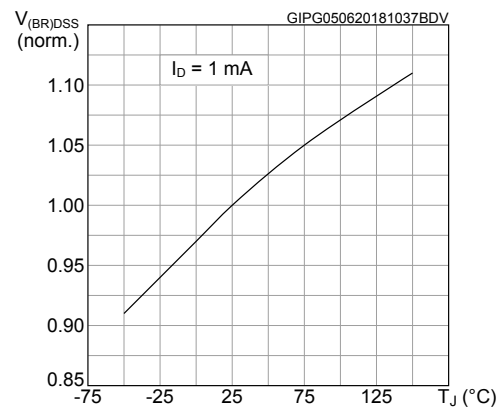


Figure 11. Output capacitance stored energy

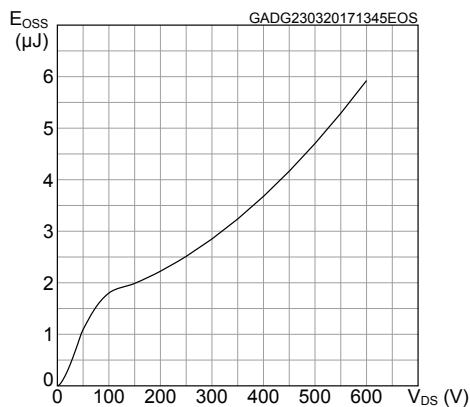
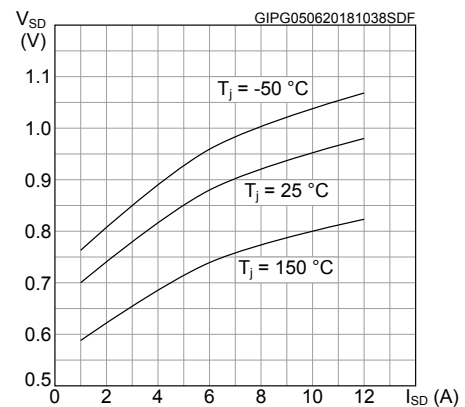
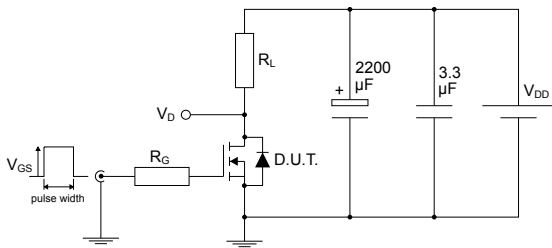


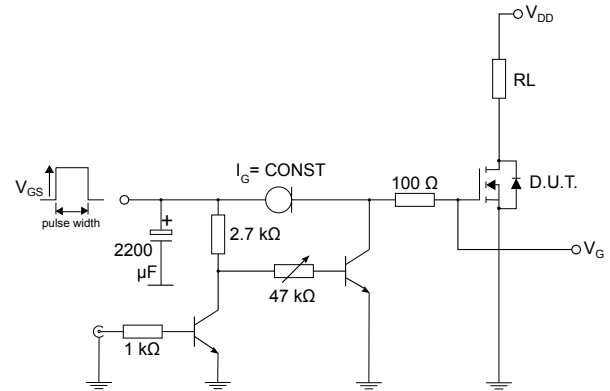
Figure 12. Source-drain diode forward characteristics



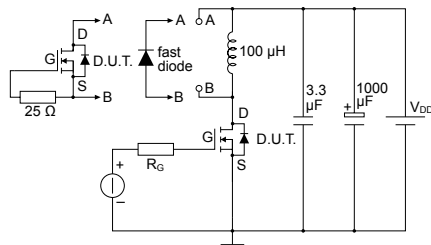
3 Test circuits

Figure 13. Test circuit for resistive load switching times


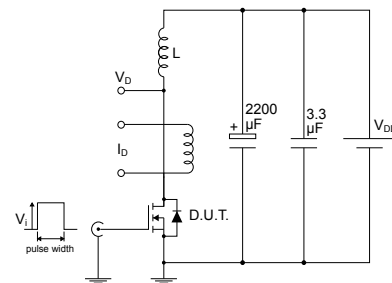
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Figure 14. Test circuit for gate charge behavior


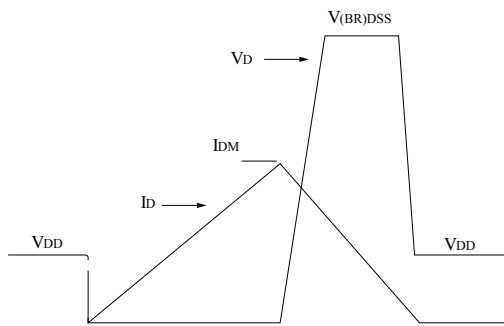
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Figure 15. Test circuit for inductive load switching and diode recovery times


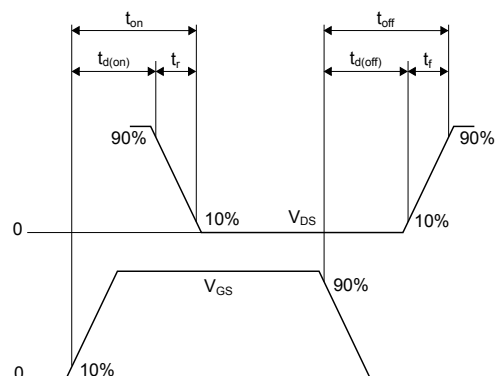
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


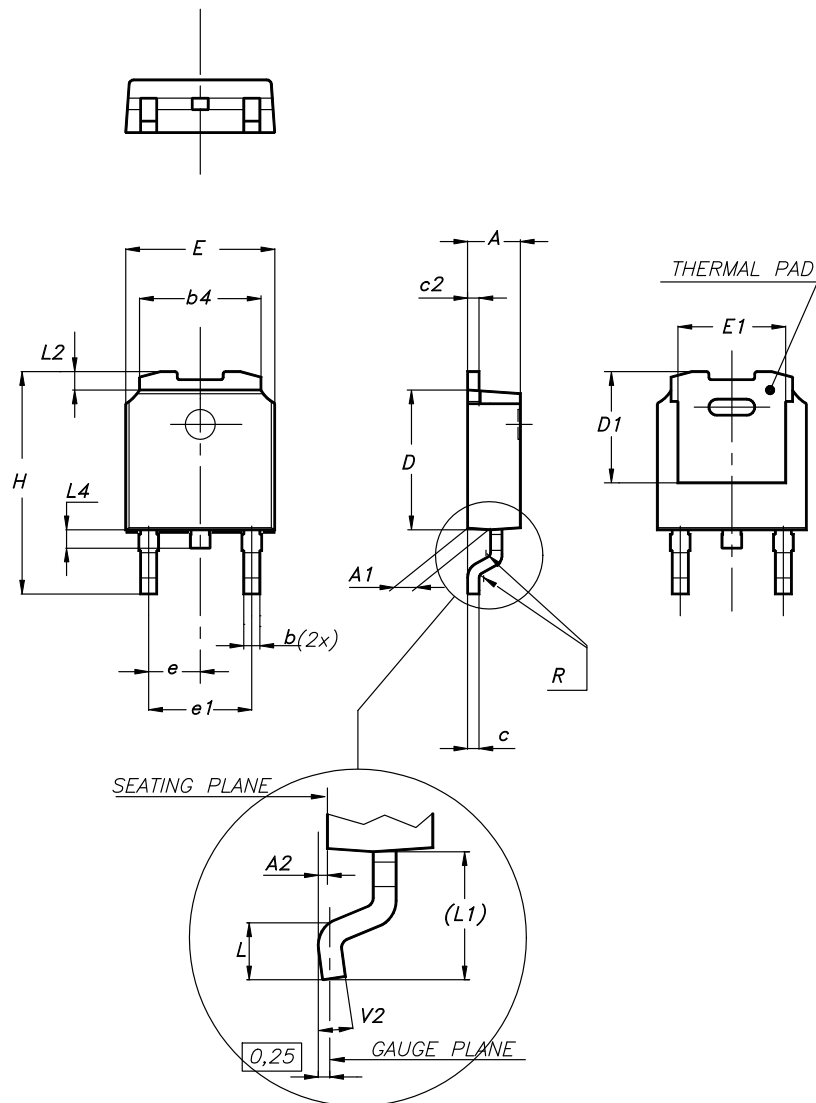
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline

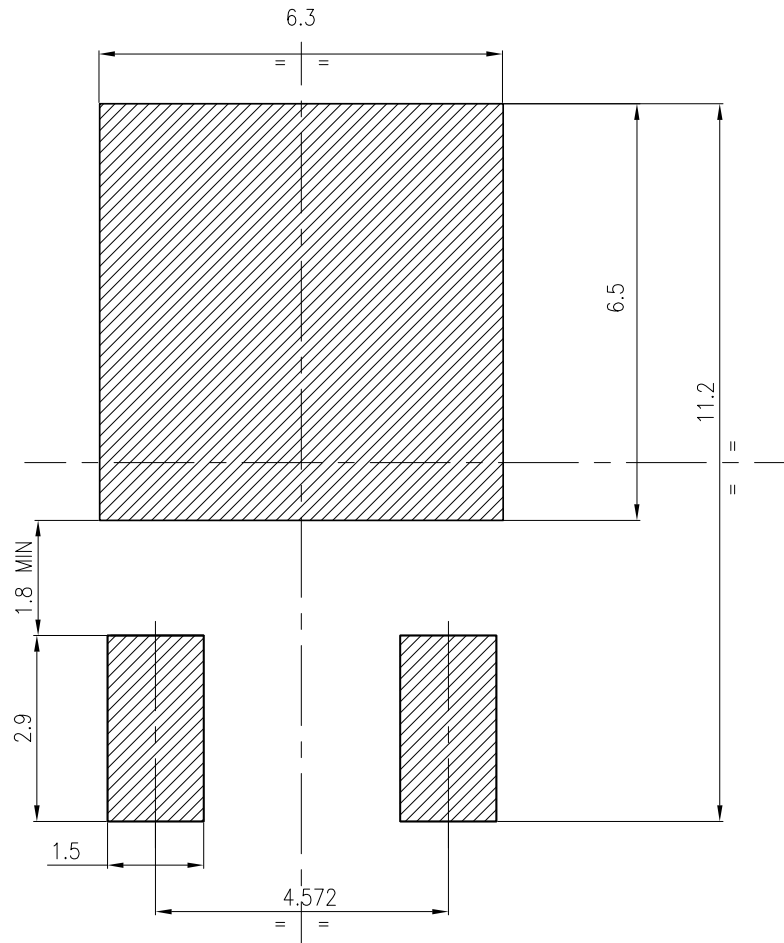


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Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

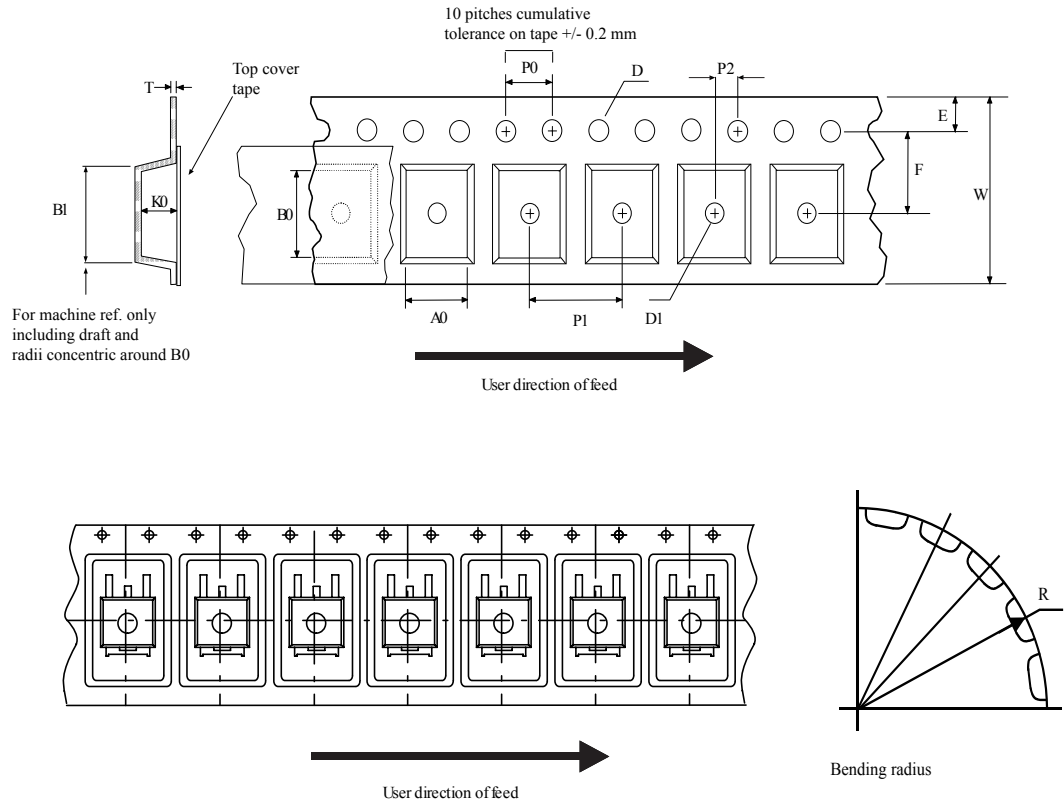
Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



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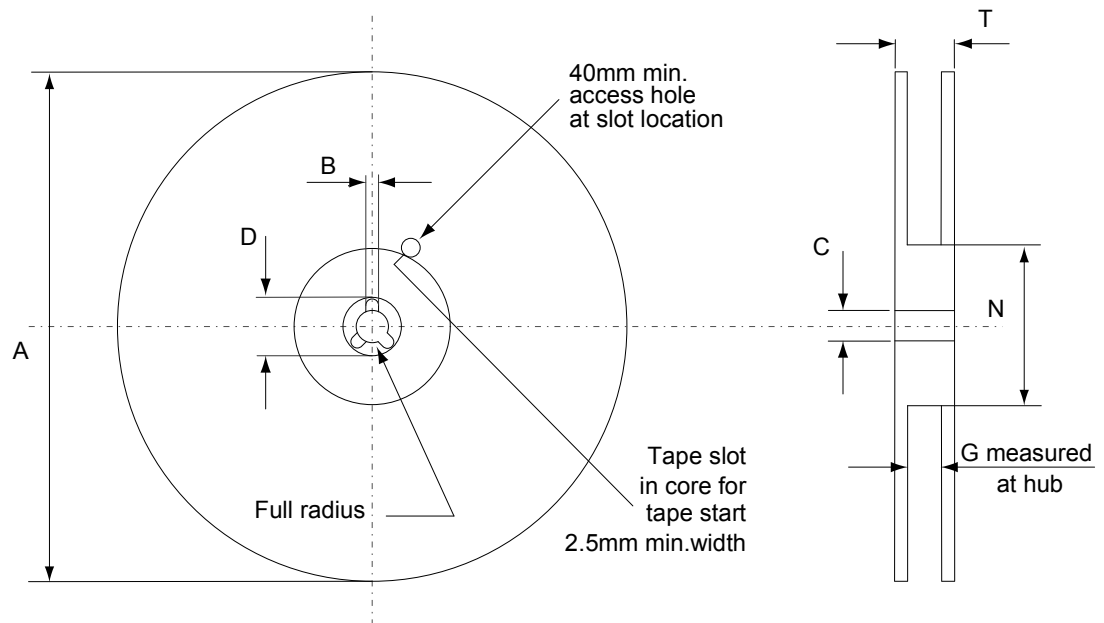
4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Jul-2018	1	First release.
05-Nov-2018	2	Updated Section 4 Package information.
08-May-2020	3	Updated Section 4 Package information.

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