Electronic fuse for 5 V line

DFN10 (3 x 3 mm)

Flip Chip 9

Maturity status link
STEF05L

Features

- Continuous current typ.: 3.6 A (DFN), 2.5 A (Flip Chip)
- N-channel on resistance (typ): 40 mΩ (DFN), 25 mΩ (Flip Chip)
- Enable/Fault functions
- Output clamp voltage (typ.): 6.1 V
- Undervoltage lockout
- Short-circuit limit
- Overload current limit
- Controlled output voltage ramp
- Thermal latch (typ): 160 °C
- Uses tiny capacitors
- Latching and auto-retry versions
- Operative junction temp. - 40 °C to 125 °C
- Available in DFN10 (3 x 3 mm) and Flip Chip 9 bumps

Applications

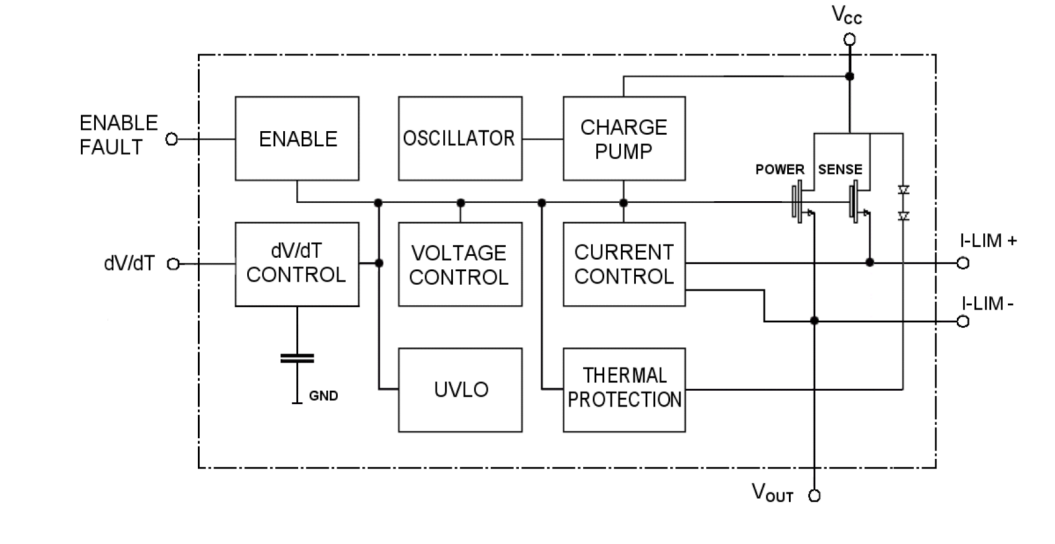
- Hard disk drives
- Solid state drives (SSD)
- Hard disk and SSD arrays
- Computer
- DVD and Blu-Ray disc drivers

Description

The STEF05L is an integrated electronic fuse optimized for monitoring output current and the input voltage. Connected in series to the 5 V rail, it is able to protect the electronic circuitry on its output from overcurrent and overvoltage. The STEF05L has controlled delay and turn-on time. When an overload condition occurs, the device limits the output current to a predefined safe value. If the anomalous overload condition persists, it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, when the power is re-applied the eFuse initially limits the output current to a safe value and then goes again into the open state. The voltage clamping circuit prevents the output voltage from exceeding a fixed value, if the input voltage goes beyond this threshold. The device is equipped with a thermal protection circuit. Intervention of thermal protection is signaled to the board-monitoring circuits through an appropriate signal on the Fault pin. Unlike mechanical fuses, which must be physically replaced after a single event, the eFuse does not degrade in its performances following short-circuit/thermal protection intervention and is reset either by re-cycling the supply voltage or using the appropriate Enable pin. The STEF05L is also available in an autoretry version; in case of thermal fault it automatically attempts to re-apply power to the load when the die temperature returns to a safe value.

1 Device block diagram

Figure 1. **Block diagram**



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2 Pin configuration

Figure 2. **Pin configuration**

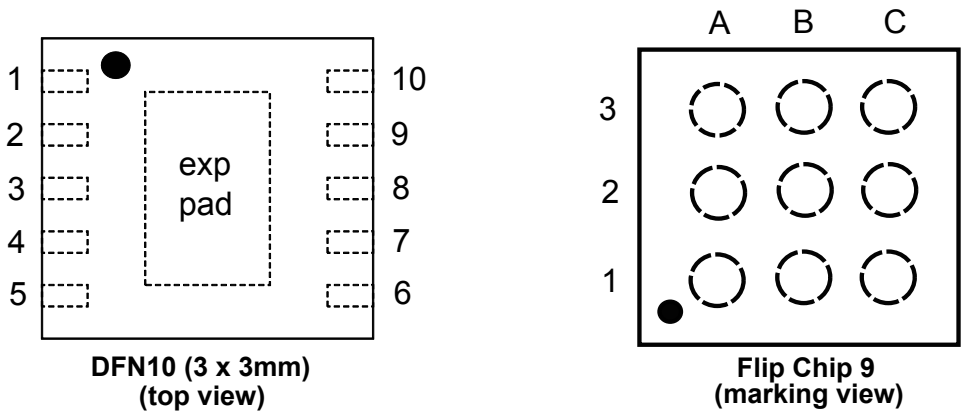

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Table 1. **Pin description**

Pin n° DFN10 (3 x 3 mm)	Pin n° Flip Chip 9	Symbol	Note
1, 2, 3, 4, 5	C1, C2, C3	V_{OUT}/source	Connected to the source of the internal power MOSFET and to the output terminal of the eFuse.
6	N.C.	I-lim -	A resistor between these two pins sets the overload and short-circuit current limit levels. On the Flip Chip the resistor must be connected between the I-Lim+ and Source pins.
7	A1	I-lim +	
8	A2	En/Fault	The Enable/Fault pin is a tri-state, bi-directional interface. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin goes into an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
9	N.C.	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 1.4 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open. This feature is not available on the Flip Chip version.
10	A3	GND	Ground pin.
Exposed pad	B1, B2, B3	V_{CC}	Exposed pad. Positive input voltage must be connected to V_{CC}.

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage	-0.3 to 10	V
V_{OUT}/Source	V_{OUT} pin voltage	-0.3 to 7	V
	V_{OUT} pin voltage (100 ms)	- 0.3 to V_{CC} + 0.3	
I-Lim+/I-Lim-	Current limit pin voltage	-0.3 to 7	V
	Current limit pin voltage (100 ms)	- 0.3 to V_{CC} + 0.3	
En/Fault	Enable/Fault pin voltage	-0.3 to 4.6	V
dv/dt	dv/dt pin voltage	-0.3 to 4.6	V
T_{OP}	Operating junction temperature range (1)	- 40 to 125	°C
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec	260	°C

1. *The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Recommended operating condition

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage	4.5 to 8	V
R_{Limit}	Current sense resistor range, STEF05L, STEF05LA	10 to 120	Ω
	Current limitation resistor range, STEF05LJ, STEF05LAJ	15 to 120	
$C_{dv/dt}$	Soft-start capacitor range	0 to 1	nF
V_{EN}	Enable/Fault pin voltage	0 to 3.6	V

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient, DFN10 (3 x 3 mm)	70	°C/W
	Thermal resistance junction-ambient, Flip Chip 9	90	
R_{thJC}	Thermal resistance junction-case, DFN10 (3 x 3 mm)	34	

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection	HBM	4	kV
		MM	400	V
		CDM DFN10 (3 x 3 mm)	500	V
		CDM (Flip Chip 9)	250	V

4 Electrical characteristics

V_{CC} = 5 V, C_I = 10 µF, C_O =10 µF, T_J = 25 °C (unless otherwise specified).

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Under/over voltage protection						
V_{Clamp}	Output clamping voltage	V_{CC} = 8 V	5.5	6.1	6.8	V
V_{UVLO}	Under voltage lockout	Turn-on, voltage increasing	3.1	3.4	4.0	V
V_{Hyst}	UVLO hysteresis			0.1		V
Power MOSFET						
t_{dly}	Delay time	Enabling of chip to V_{OUT} = 10 % of nominal value		500		µs
R_{DSon}	ON resistance (DFN package) (1)	I_{OUT} = 500 mA, T_J = 25 °C		40	60	mΩ
		I_{OUT}= 500 mA, -40 °C < T_J < 125 °C			70	
	ON resistance (Flip Chip package) (1)	I_{OUT} = 500 mA, T_J = 25 °C		30	50	mΩ
		I_{OUT} = 500 mA, -40 °C < T_J < 125 °C			70	
V_{OFF}	Off state output voltage	V_{EN} = GND, R_L = infinite			100	mV
I_D	Continuous current	DFN package		3.6		A
		Flip Chip package		2.5		
Current limit						
I_{Short}	Short-circuit current limit	R_{Limit} = 24 Ω, DFN package	0.8	1.2	1.6	A
		R_{Limit} = 24 Ω, Flip Chip package	1.1	1.5	1.9	
I_{Lim}	Overload current limit	R_{Limit} = 24 Ω (2)		2.5		A
dv/dt circuit						
dv/dt	Output voltage ramp time	V_{OUT} = 10 % to 90 % of nominal voltage, No $C_{dv/dt}$	0.8	1.4	2.5	ms
Enable/Fault						
V_{IL}	Low level input voltage	Output disabled (2)			0.5	V
$V_{I(INT)}$	Intermediate level input voltage	Thermal fault, output disabled (2)	0.8	1.4	2	V
V_{IH}	High level input voltage	Output enabled	2.5			V
$V_{I(MAX)}$	High state maximum voltage			3.25		V
I_{IL}	Low level input current (sink)	V_{Enable} = GND		-28	-50	µA
	Maximum fan-out for fault signal	Total number of chips that can be connected to this pin for simultaneous shutdown (2)			3	Units
Total device						
I_{Bias}	Bias current	Device operational		0.7	2	mA
		Thermal shutdown (only on latching versions) (2)		0.5		
		Device disabled (V_{EN} = GND)		0.35		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Thermal latch						
TSD	Shutdown temperature	(2)		160		°C
	Hysteresis	Only on auto-retry versions (2)		25		

1. *Pulse test.*
2. *Guaranteed by design, but not tested in production.*

5 Typical application

Figure 3. **Application circuit, STEF05L and STEF05LA (DFN10 (3 x3 mm) package)**

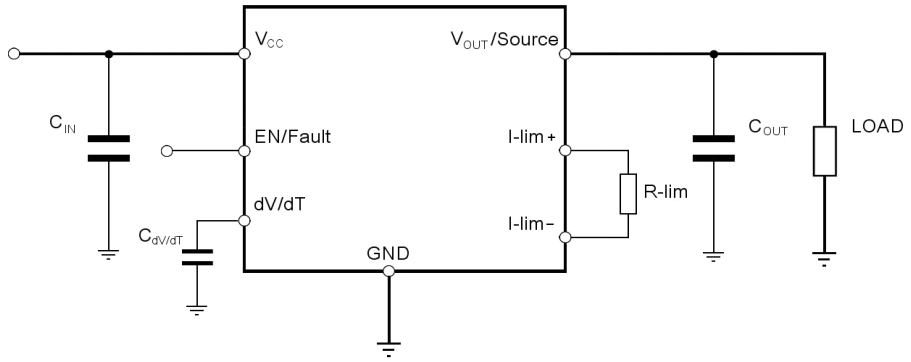

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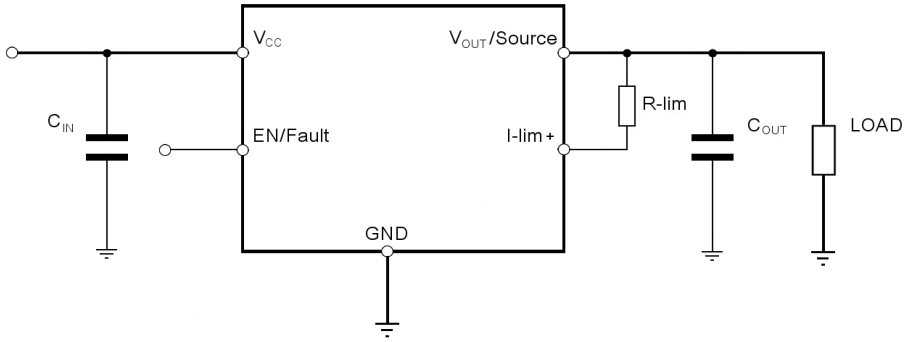
Figure 4. **Application circuit with Kelvin current sensing, STEF05LJ and STEF05LAJ (Flip-Chip 9 bump package)**



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5.1 Operating modes

5.1.1 Turn-on

When the input voltage is applied, the Enable/Fault pin goes up to the high state, enabling the internal control circuitry.

After an initial delay time of typically 500 ms, the output voltage is supplied with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to dv/dt pin, the total time from the Enable signal going high and the output voltage reaching the nominal value is around 1.6 ms (refer to Figure 5. Delay time and V_{OUT} rise time, and Figure 15. V_{OUT} turn-on vs enable).

5.1.2 Normal operating condition

The STEF05L eFuse behaves like a mechanical fuse, buffering the circuitry on its output with the same voltage shown at its input, with a small voltage fall due to the N-Channel MOSFET R_{DSOn}.

5.1.3 Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 6.1 V, if the input voltage exceeds this threshold.

5.1.4 Current limiting

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the value selected externally by means of the limiting resistor R_{Limit} (Figure 3. Application circuit, STEF05L and STEF05LA (DFN10 (3 x3 mm) package)).

5.1.5 Thermal shutdown and auto-retry function

If the device temperature exceeds the thermal latch threshold, typically 160 °C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The EN/Fault pin of the device is automatically set to an intermediate voltage, in order to signal the overtemperature event.

The STEF05L latch version can be reset from this condition either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold and then releasing it.

On the STEF05LA auto-retry version, the power MOSFET will remain in an OFF state until the die temperature drops below the hysteresis value. Once this happens, the internal autoretry circuit attempts to reset the device, pulling up the EN/Fault pin to the operative value.

5.2 R_{Limit} calculation

As shown in Figure 1. Block diagram the device uses an internal N-Channel Sense FET with a fixed ratio, to monitor the output current and limit it at the level set by the user.

The R_{Limit} value for achieving the requested current limitation can be estimated by using the “current limit vs R_{Limit}”, graph in Figure 12. Current limit vs R_{Limit} (I_{OUT} ramp).

The device has two levels of current limitation, depending on the load condition.

The short-circuit current limit (I_{Short}) is the current level that is imposed when the output voltage decreases sharply, as in the case of a short-circuit on the output.

The overload current limit (I_{Lim}), also described as “current limit trip-point”, represents the current level that is recognized by the device as an overload condition. Following this, the current limit trip point is reached the device enters into current limitation, and the current to the load is limited to the I_{Short} value, which is generally lower than the trip-point value.

The overload current limit (I_{Lim}) is dependent on the device reaction time, so it is influenced by the load current slew-rate. The faster the current increase, the higher the current limit trip point.

5.3 $C_{dv/dt}$ calculation

The device includes a rise-time control circuit, allowing the soft-start during turn-on and Hotplug of the equipment. The pre-programmed rise time, defined as the time interval during which the output voltage goes from 10 % to 90 % of the nominal voltage, is typically 1.4 ms.

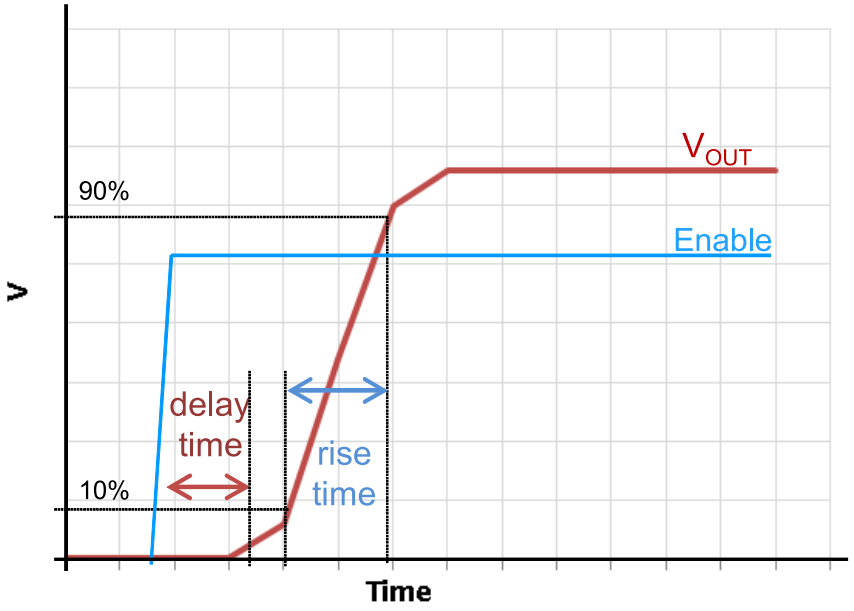
The STEF05L and STEF05LA in DFN10 package feature a user-programmable output voltage ramp-up time; by connecting a capacitor between the $C_{dv/dt}$ pin and GND, modification of the output voltage ramp-up time is possible. The capacitance to be added on the $C_{dv/dt}$ pin can be selected using the following table.

Table 7. Typical rise time values vs dv/dt capacitor

$C_{dv/dt}$	None	100 pF	470 pF	1 nF
Rise time [ms] (1)	1.4	2.8	8	16

1. *V_{CC} = 5 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, R_{LIMIT} = 24 Ω, I_{OUT} = 1 A.*

Figure 5. **Delay time and V_{OUT} rise time**



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5.4 Enable-Fault pin

The Enable/Fault pin has the dual function of controlling the output of the device and, at the same time, of providing information about the device status to the application.

It can be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it will turn the output of the eFuse off.

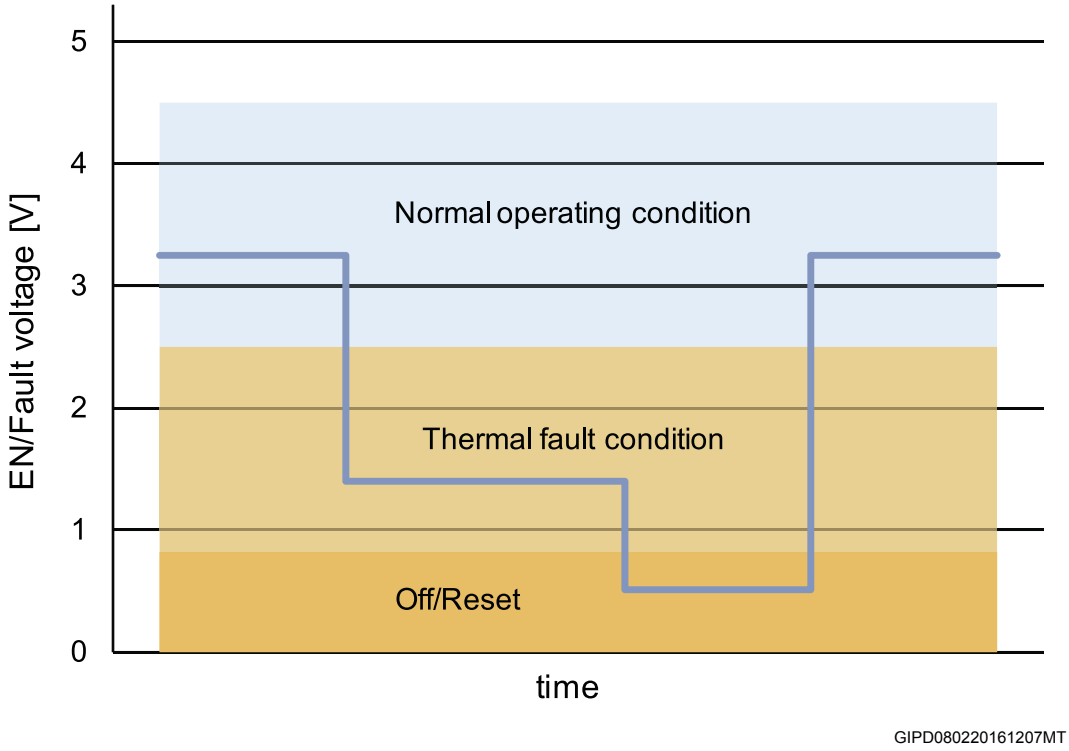
If this pin is left floating, since it has internal pull-up circuitry, the output of the eFuse is kept ON in normal operating conditions.

This pin should never be biased to a voltage higher than 3.6 V.

In case of thermal fault, the pin is pulled to an intermediate state (Figure 6. Enable/Fault pin status). This signal can be provided to a monitor circuit, signaling that a thermal shutdown has occurred, or it can be directly connected to the Enable/Fault pins of other STEFxx devices on the same application, in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

Figure 6. **Enable/Fault pin status**



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6 Typical performance characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25 °C.

Figure 7. Clamping voltage vs temperature

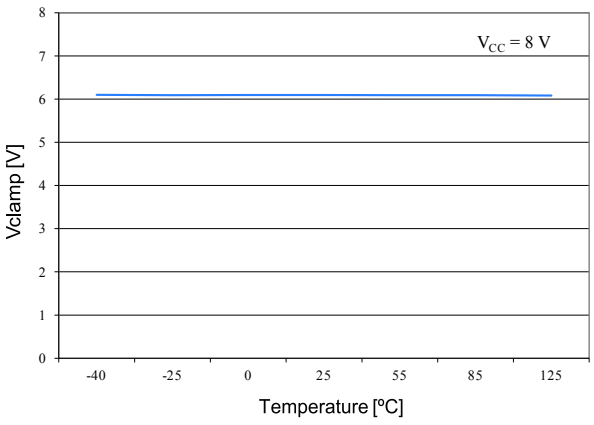

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Figure 8. Short-circuit current vs temperature

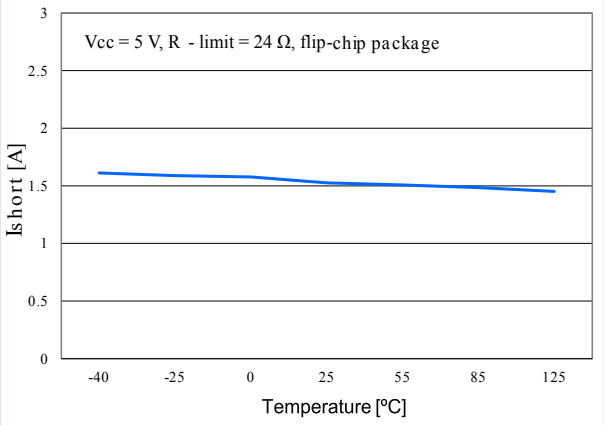

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Figure 9. Bias current vs temperature (device operational)

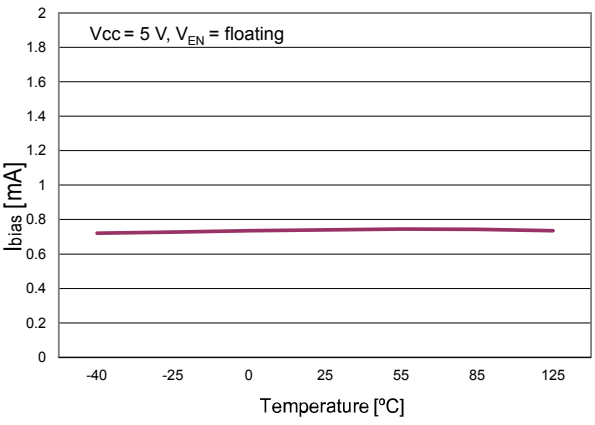

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Figure 10. Bias current vs temperature (device disabled)

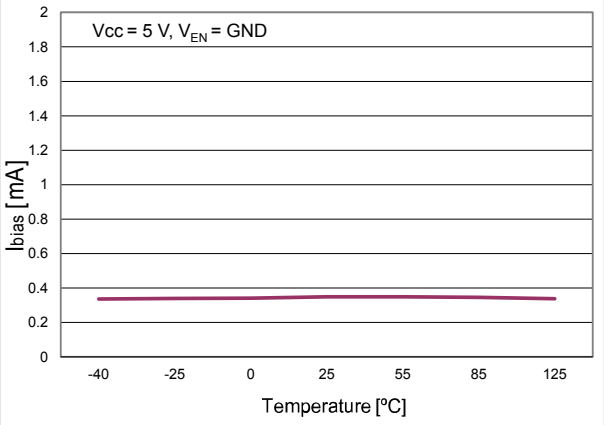

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Figure 11. ON resistance vs temperature

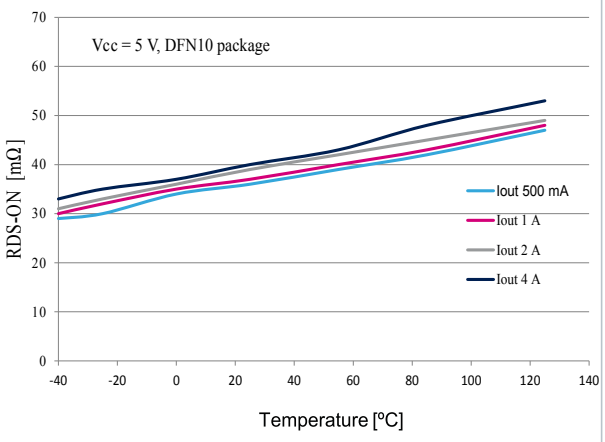

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Figure 12. Current limit vs R_{Limit} (I_{OUT} ramp)

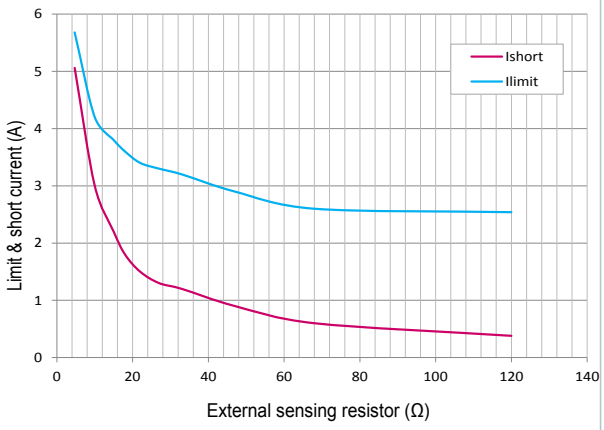

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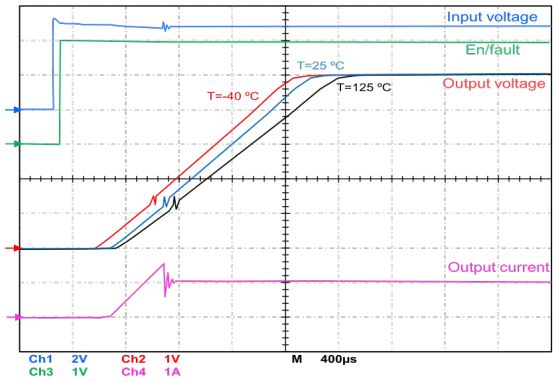
Figure 13. V_{OUT} ramp-up vs enable (NO C_{dvdt})



V_{CC} = 5 V, Enable from GND to Floating, C_{IN} = C_{OUT} = 10 µF, R_{Limit} = 24 Ω, NO Cdv/dt, I_{OUT} = 1 A

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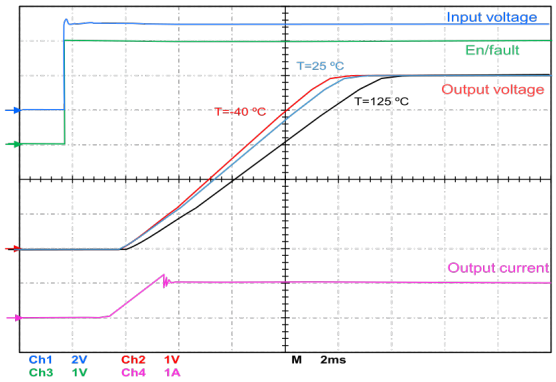
Figure 14. V_{OUT} ramp-up vs enable (C_{dvdt} = 470 pF)



V_{CC} = 5 V, Enable from GND to Floating, C_{IN} = C_{OUT}= 10 µF, R_{Limit} = 24 Ω, Cdv/dt= 470 pF, I_{OUT} = 1 A

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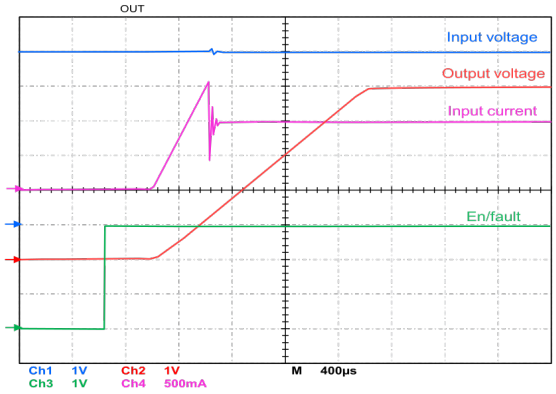
Figure 15. V_{OUT} turn-on vs enable



V_{CC} = 5 V, Enable from GND to Floating, C_{IN} = C_{OUT}= 10 µF, R_{Limit} = 24 Ω, NO Cdv/dt, I = 1 A

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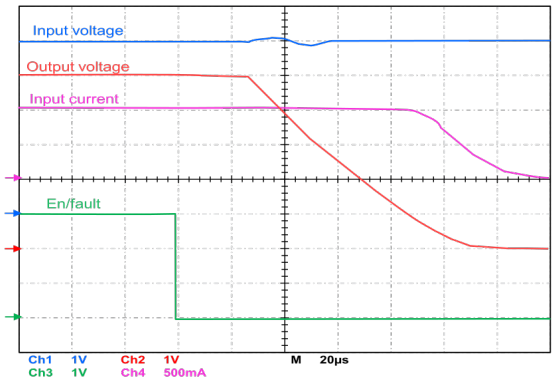
Figure 16. V_{OUT} turn-off vs enable



V_{CC} = 5 V, Enable from Floating to GND, C_{IN} = C_{OUT} = 10 µF, R_{Limit} = 24 Ω, NO Cdv/dt, I_{OUT} = 1 A

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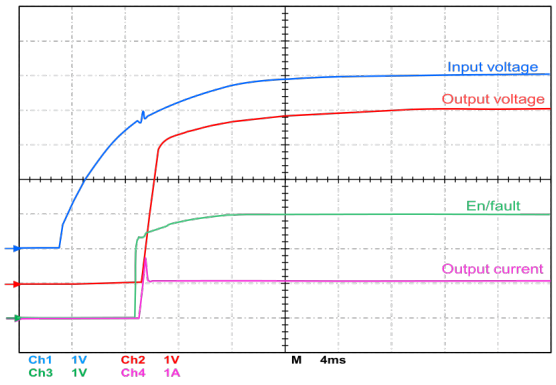
Figure 17. Startup (slow rising)



V_{CC} = from 0 to 5 V, C_{IN} = C_{OUT} = 10 µF, R_{Limit}= 24 Ω, NO Cdv/dt, I_{OUT} = 1 A

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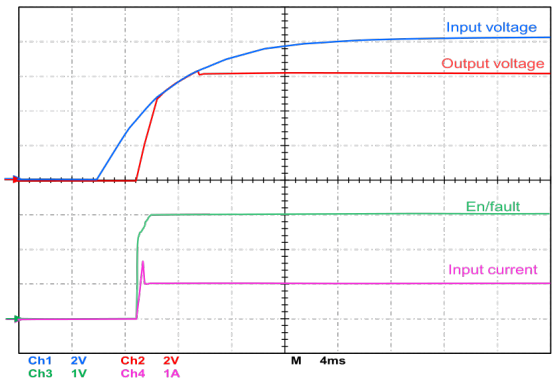
Figure 18. Startup and voltage clamp



V_{CC} = from 0 to 8 V, C_{IN} = C_{OUT} = 10 µF, R_{Limit} = 24 Ω, NO Cdv/dt, I_{OUT} = 1 A

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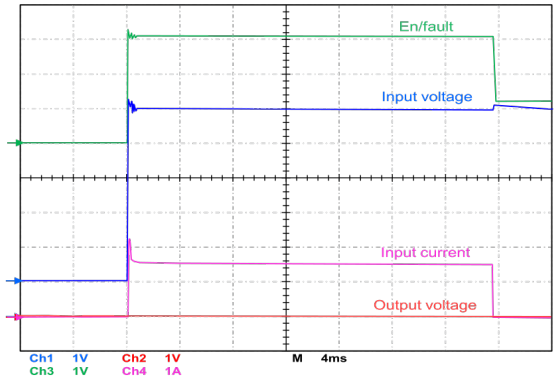
Figure 19. Startup into output short-circuit



V_{CC} = from 0 to 5 V, C_{IN}= C_{OUT} = 10 µF, R_{Limit} = 24 Ω, V_{OUT} short to GND

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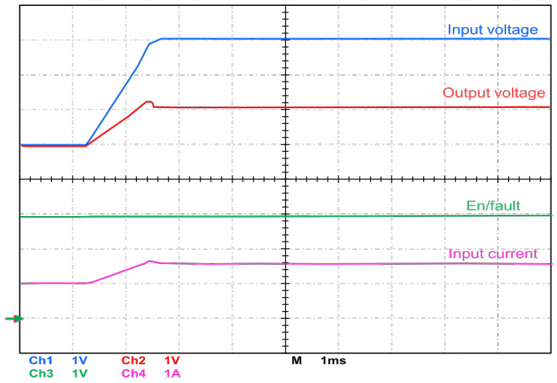
Figure 20. Voltage clamp



V_{CC} = from 5 to 8 V, C_{IN} = C_{OUT} = 10 µF, R_{Limit} = 24 Ω, I_{OUT} = 1 A

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN10 (3x3 mm) package information

Figure 21. **DFN10 (3x3 mm) package outline**

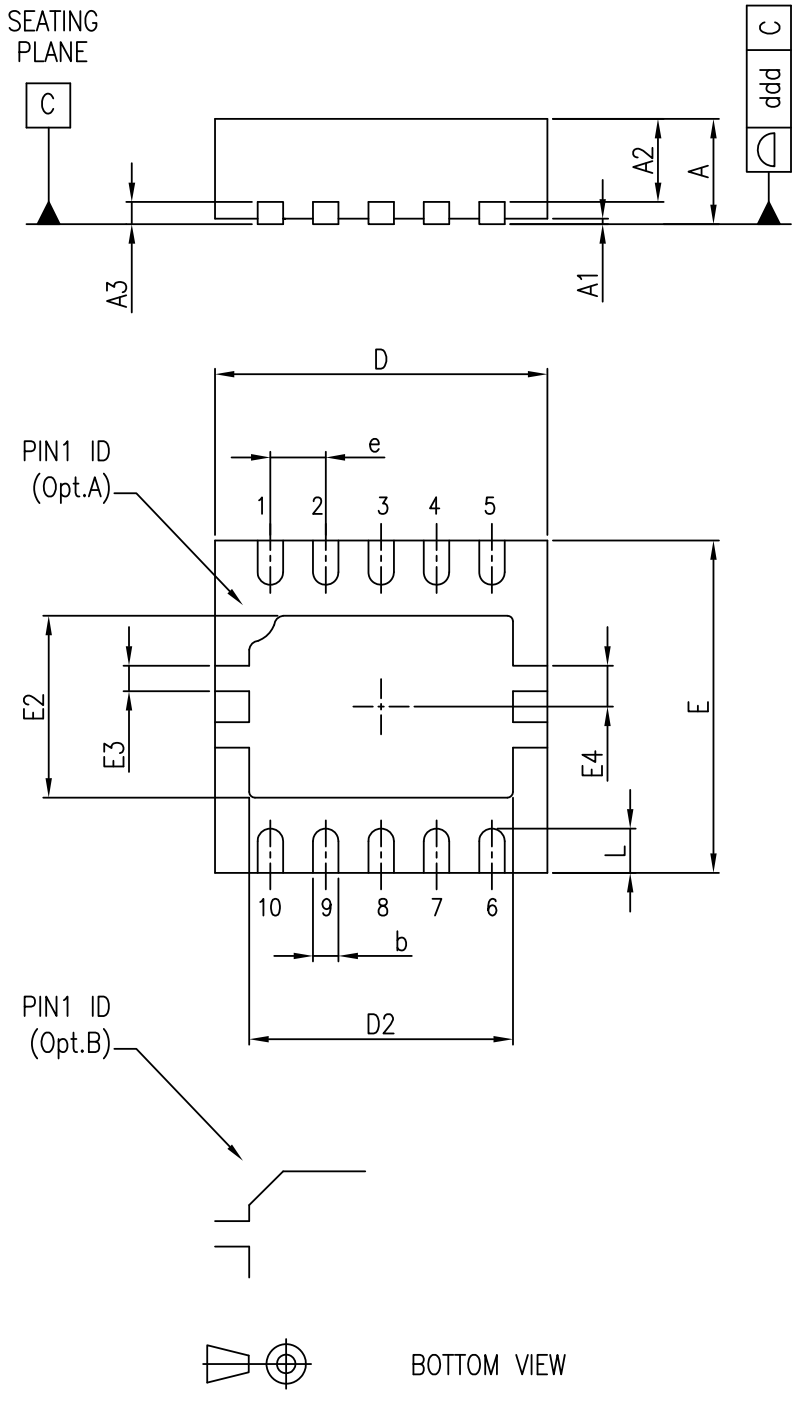

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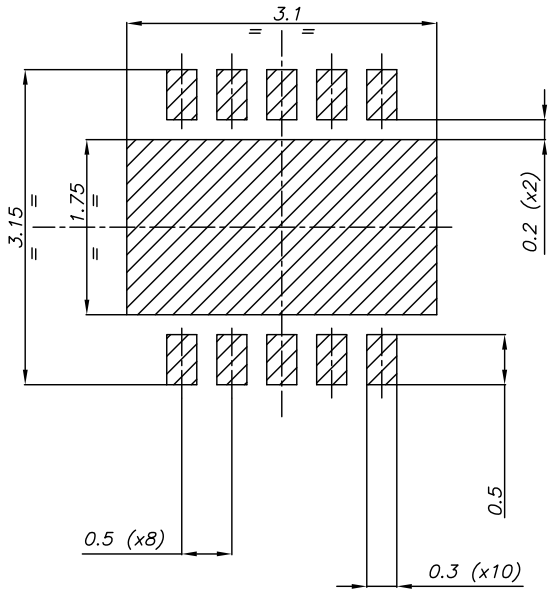
Table 8. **DFN10 (3x3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	00.5
A2		0.70	
A3		0.20	
b	0.18	0.23	0.30
D	2.85	3.00	3.15
D2	2.23	2.38	2.50
E	2.85	3.00	3.15
E2	1.49	1.64	1.75
E3	0.230		
E4	0.365		
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 22. **DFN10 (3x3 mm) recommended footprint**



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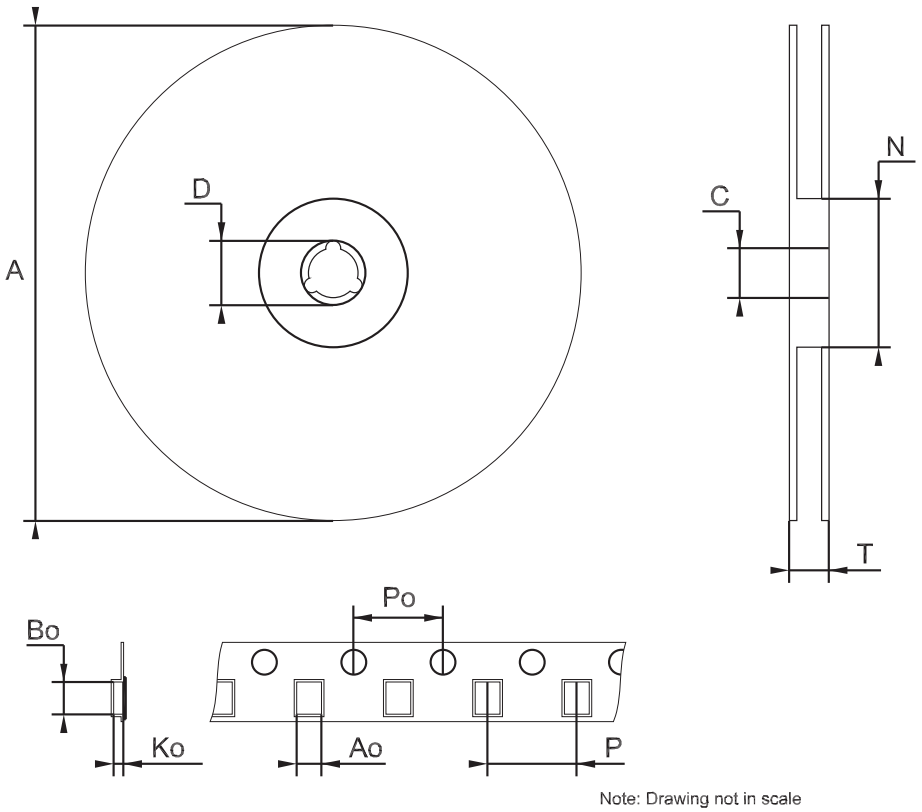
7.2 QFNxx/DFNxx (3 x 3 mm) package information

Figure 23. **DFN10 (3x3 mm) tape and reel outline**



Note: Drawing not in scale

Table 9. **DFN10 (3x3 mm) tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			18.4
Ao		3.3	
Bo		3.3	
Ko		1.1	
Po		4	
P		8	

7.3 Flip Chip 9 package information

Figure 24. **Flip Chip 9 package outline**

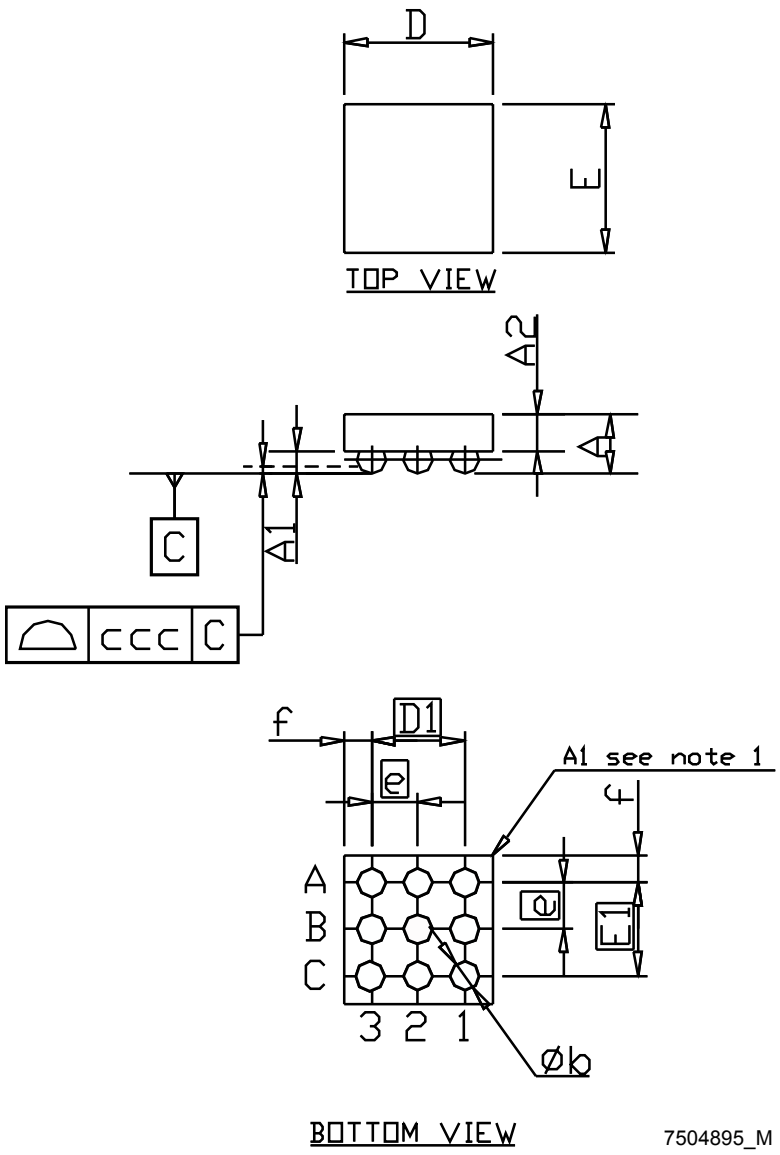
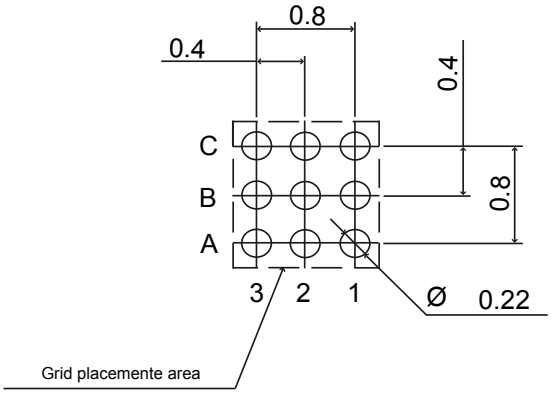


Table 10. **Flip Chip 9 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.17	0.20	0.23
A2	0.33	0.35	0.37
b	0.23	0.25	0.29
D	1.16	1.19	1.22

Dim.	mm		
	Min.	Typ.	Max.
D1		0.8	
E	1.16	1.19	1.22
E1		0.8	
e		0.40	
f		0.195	
ccc		0.075	

Figure 25. Flip Chip 9 recommended footprint



8 Ordering information

Table 11. **Order code**

Tape and reel	Package	Version	Marking
STEF05LPUR	DFN10 (3 x 3 mm)	Latch	EF05L
STEF05LJR	Flip Chip 9	Latch	5L
STEF05LAPUR	DFN10 (3 x 3 mm)	Auto-retry	EF05LA
STEF05LAJR	Flip Chip 9	Auto-retry	5A

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
04-Nov-2016	1	Initial release
15-Dec-2020	2	Updated Figure 9 and Figure 10

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