Design Note:

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Choosing an Optimal Filter Capacitor for the MAX3872 Multi-Rate CDR

maxim integrated™

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1 Introduction

The MAX3872 is a clock and data recovery (CDR) with limiting amplifier IC, designed to operate at multiple data rates. It is intended for regenerator and receiver applications and contains a fully-integrated phase lock loop (PLL). The PLL is a second-order feedback system that requires an external capacitor for the loop filter. This capacitor is a significant factor in multi-rate designs because it determines the acquisition time and jitter peaking at a particular data rate.

This design note is intended as a guide for choosing the optimal filter capacitor to minimize acquisition time, while meeting the jitter peaking specifications at all the data rates required for the application.

2 Role of the Filter Capacitor

2.1 PLL Overview

A fully integrated PLL is used in the MAX3872 to recover a synchronous clock signal from serial NRZ data. The PLL consists of a phase/frequency detector, loop filter, voltage-controlled oscillator (VCO), and programmable frequency divider. Refer to Figure 1 for a simplified model of the PLL.

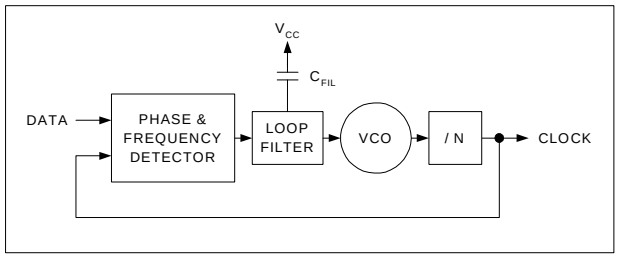

Figure 1. Simplified PLL Model

The phase/frequency detector converts phase and frequency error into current. The loop filter operates on the phase/frequency output current to generate a voltage that is forced on the filter capacitor. Control for the VCO is derived from the voltage on the filter capacitor. The VCO translates the control voltage to frequency, and the VCO output is fed through programmable dividers then back to the phase/frequency detector. Because of its feedback nature, the PLL drives the VCO until the error at the phase/frequency detector is zero.

2.2 PLL Characteristics

The loop filter and programmable dividers establish the key characteristics of the PLL, including jitter transfer bandwidth, jitter peaking, loop stability, and acquisition time. When designing with the MAX3872 the only adjustable parameter is the value of the filter capacitor, which will not affect jitter transfer bandwidth, but it will affect jitter peaking, loop stability, and acquisition time.

2.3 Jitter Peaking and Loop Stability

The PLL transfer function has a zero frequency (f_Z) that depends on the filter capacitor (C_{FIL}), and can be approximated according to:

$$f_Z = \frac{1}{2\pi\,(650\Omega)\,C_{FIL}}$$

The position of this zero relative to the jitter transfer bandwidth (J_{BW}) for a given data rate determines the loop-damping coefficient. The typical and maximum values for J_{BW} are given in the MAX3872 datasheet for the standard SONET/SDH data rates.

In SONET/SDH applications the damping coefficient must be sufficiently large to ensure the jitter peaking is less than 0.1dB in the jitter transfer bandpass region. This can be achieved by setting f_z lower than J_{BW} by a factor of approximately 100, which produces a large damping coefficient.

The MAX3872 PLL is a second order system and is considered overdamped when f_Z is at least four times smaller than J_{BW}. Under this condition, the jitter peaking (J_P), in dB, can be approximated by:

$$J_P = 20 \log\left(1 + \frac{f_Z}{J_{BW}}\right)$$

Figure 2 provides approximations of J_P using typical values of J_{BW}. To avoid excessive peaking and loop instability, use a filter capacitor that puts the loop in an overdamped condition with a sufficiently large damping coefficient at the lowest data rate required for the application.

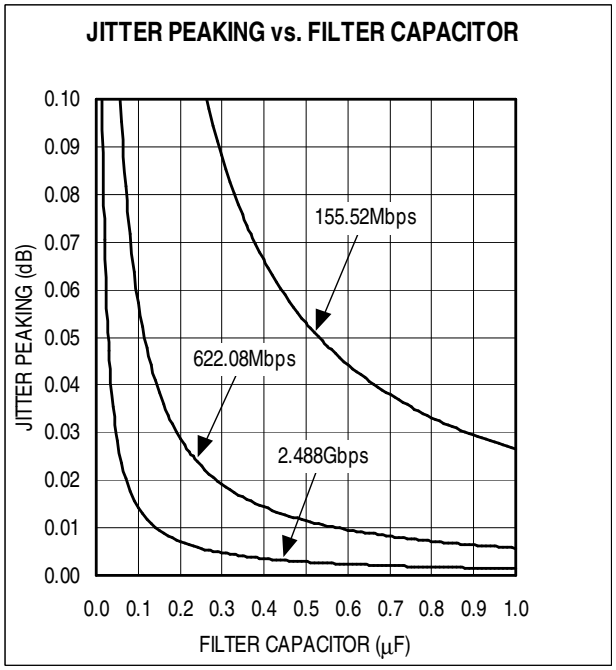

Figure 2. Jitter Peaking vs. Filter Capacitor

2.4 Acquisition Time

Acquisition time is defined in the MAX3872 datasheet as the time the PLL needs to reacquire phase/frequency lock to data and have the loss-of-lock ($\overline{LOL}$) indicator transition high (See Figure 3).

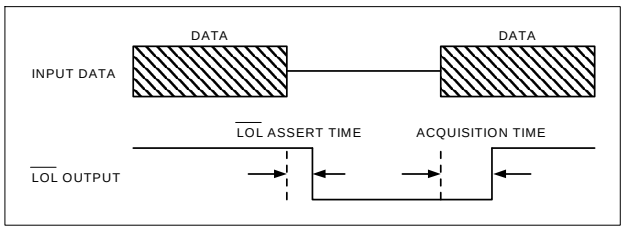

Figure 3. Definition of Acquisition Time

While there is valid data at the inputs, the $\overline{LOL}$ indicator remains high and the PLL remains locked to the data. When the data becomes invalid the $\overline{LOL}$ indicator transitions low and the PLL charges the filter capacitor, which forces the VCO to the edge of its frequency range. When valid data returns, the loop filter works with the phase/frequency detector error current to discharge the filter capacitor. The capacitor continues to discharge, with a time constant proportional to the capacitor value, until the PLL is phase/frequency locked to the data. Therefore, the greater the capacitor value, the longer it will take the PLL to reacquire lock to the data.

3 Tradeoff Between Jitter Peaking and Acquisition Time

If acquisition time isn't important, the best solution is a capacitor value that sets the zero frequency far below the jitter transfer bandwidth at the lowest data rate. This keeps the jitter peaking below 0.1dB at all the data rates, but also makes the acquisition time longer than is necessary and/or acceptable.

To decrease acquisition time the zero needs to be moved closer to the jitter transfer bandwidth, but if the zero is moved too much, the jitter peaking will increase to an unacceptable level. This is the tradeoff between jitter peaking and acquisition time that must be considered when optimizing the filter capacitor.

4 Optimizing for the Application

The MAX3872 can operate at multiple data rates ranging from 155Mbps to 2.67Gbps, but not all of the intended applications require this wide of a range. Furthermore, each application may have different limits for jitter peaking and acquisition time.

Typically jitter peaking is the first variable considered when choosing the filter capacitor. Most applications require the jitter peaking to be less than 0.1dB at all the data rates used in the design. The lowest data rate will always require the largest capacitor to meet this requirement. Optimization is accomplished by starting with the largest recommended capacitor (0.82µF), then decreasing its value until the desired acquisition time is achieved or until the jitter peaking does not have sufficient margin from the 0.1dB limit at the lowest data rate.

If acquisition time is more important than jitter peaking, the capacitor value can be decreased until the timing requirement is achieved at all the data rates. Acquisition time does not necessarily scale with data rate and thus the lowest data rate may not be the worst case. Once the capacitor has been chosen, it is important to also determine the jitter peaking at the lowest data rate. If the peaking is excessive it can lead to significant jitter accumulation along the data path. Optimizing for acquisition time should be done with caution because extremely small capacitor values may cause PLL instability.

5 Measurement Results

Figures 4 to 7 are measurements of jitter transfer and acquisition time at the standard SONET/SDH data rates. All measurements were done under typical conditions (V_{CC} = 3.3V, T_A = 25°C, PRBS = 2^{23}-1) and show trends with different filter capacitors.

Jitter peaking and acquisition time change with supply voltage and temperature, therefore the typical curves should not be used for design verification. For guaranteed performance, a full evaluation under worst case conditions is required.

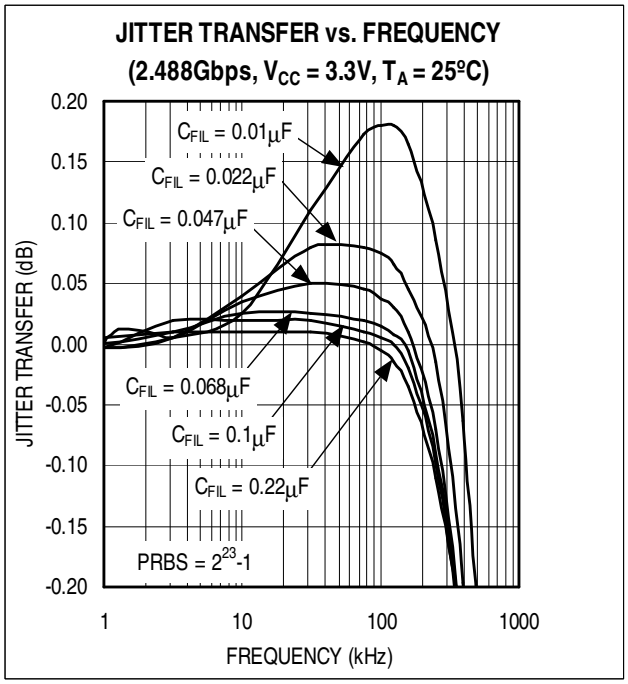

Figure 4. Jitter Transfer (2.488Gbps)

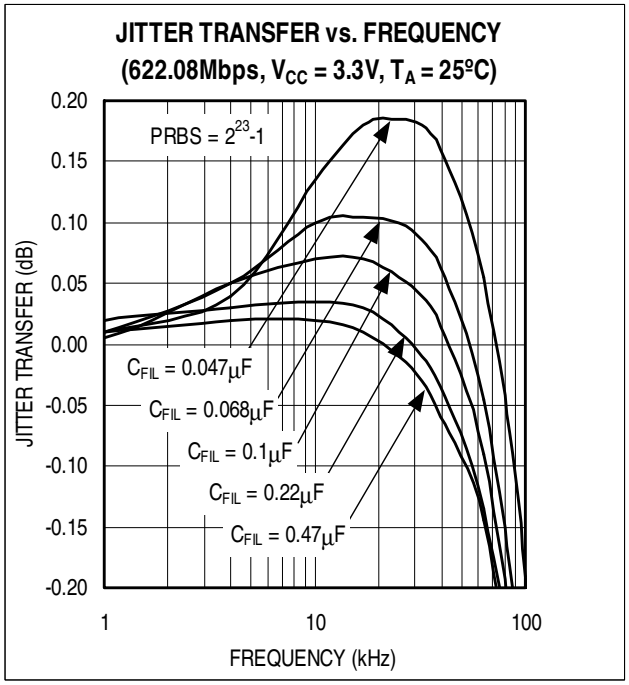

Figure 5. Jitter Transfer (622.08Mbps)

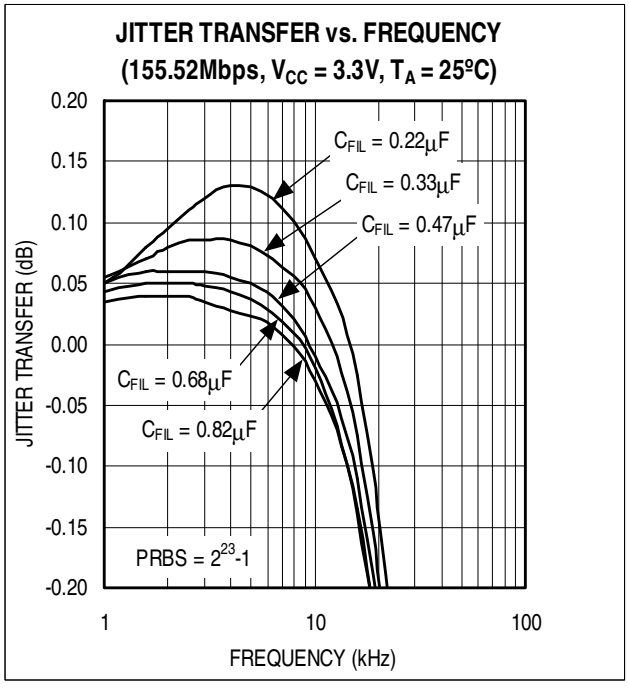

Figure 6. Jitter Transfer (155.52Mbps)

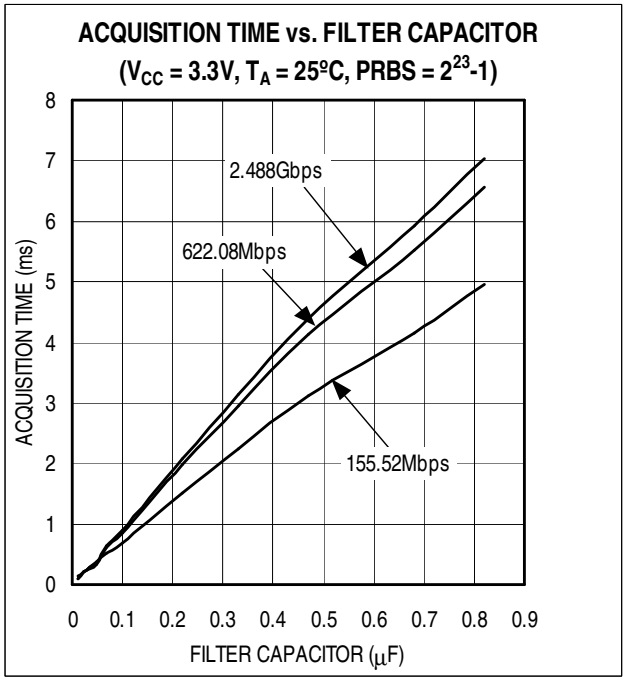

Figure 7. Acquisition Time vs. Filter Capacitor

6 Conclusion

The MAX3872 is designed to operate at multiple data rates ranging from 155Mbps to 2.67Gbps, but many applications do not require this full range. This allows the filter capacitor to be optimized for the specific application. By optimizing the filter capacitor, the acquisition time can be minimized while keeping the jitter peaking below the maximum limit. The equations and measured data provide general guidelines to follow when selecting the optimal filter capacitor.