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APPLICATION NOTE 4935

How to Enable the ITU-T G.703 2048kHz Synchronization Interface (T12) on the DS26303 LIU

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Abstract: Maintaining clock synchronization among multiple pieces of telecommunications equipment is an essential feature in any large installation. One common method of clock distribution is specified by the ITU-T G.703 2048kHz synchronization interface (T12). While the DS26303 E1/T1/J1 octal line interface unit (LIU) fully supports this specification, it needs some additional configuration settings for proper operation. This application note describes how to enable the 2048kHz synchronization interface mode and configure the DS26303 for use in clock-distribution applications.

Introduction

One of the lesser known features of the DS26303 E1/T1/J1 octal line interface unit (LIU) is its ability to transmit and receive a signal that complies with the 2048kHz synchronization interface (T12) of the International Telecommunication Union's ITU-T recommendation G.703 (November 2001) section 13. This application note describes how to properly program the DS26303 to enable the 2048kHz synchronization interface mode so the device can be used in clock-distribution applications such as a building integrated timing supply (BITS) or synchronization supply unit (SSU). It should be noted that there are two variants of the DS26303 available: the DS26303-120 and the DS26303-75. The only the difference between the two is the default E1 line impedance setting. One needs to be aware of this fact and ensure that the specific device used during the design phase is the same one used for manufacture.

DS26303 Programming for the 2048kHz Synchronization Interface Mode

Programming the DS26303 to support the 2048kHz synchronization interface is a multistep process and requires use of some registers that are not documented in the DS26303 data sheet. A complete description of all undocumented registers can be found below in the **Appendix**.

Before 2048kHz synchronization interface mode is enabled, a few configuration steps are necessary to ensure that the DS26303 will operate as expected.

Step 1. Change the internal clock map to use the transmit clock associated with the LIU channel (normally the TCLK input) instead of the master clock (the MCLK input). By default, the DS26303 uses the common MCLK input as the clock source when the 2048kHz synchronization interface mode is

enabled. This will cause the output signal on the TTIP/TRING pins to be frequency locked to the MCLK input rather than to the TCLK input. To program the DS26303 for the more common method with the TCLK input as the clock source, use the following software configuration.

- Set the ADDP register at address 0x1F to a value of 0x03 which will select the Global Test register bank.
- Set the TXDIG register at address 0x07 to a value of 0x10. By setting bit 4 of the TXDIG register to a 1, the 2048kHz synchronization interface mode will use the TCLK input instead of the MCLK input. It is important to note that changing bit 4 of the TXDIG register also affects two other features that normally use the MCLK input as the clock, specifically, the transmit all 1s (TAOE) and automatic transmit all 1s (ATAOS) features. Consequently, the bit needs to be set back to 0 when the 2048kHz synchronization interface mode is disabled. However, bit 4 of the TXDIG register could be set to a 1 if the engineer wants to use the TCLK input as the clock source when either TAOE or ATAOS is enabled.

Step 2. Change the current-limit value of the short-circuit detection circuit (SCDC) to prevent the TTIP/TRING transmitter outputs from being disabled. By default, the DS26303 current-limit values are incorrect when the 2048kHz synchronization interface mode is enabled. To program the DS26303 with the proper short-circuit current values, use the following software configuration.

- Set the ADDP register at address 0x1F to a value from 0x04 to 0x0B which selects the LIU1 Test through LIU8 Test register bank, respectively.
- Set the TXCMDA register at address 0x05 to one of the values listed below (**Table 1**). These values should be synchronous with the values selected in the Template Select (TS) register. For example, set the TXCMDA register to a value of 0x33 when the TS register is configured for E1 75Ω mode. Also, the Transmit Impedance Termination setting in the TS register should never be turned off when the G.703 2048kHz synchronization interface mode is enabled. Note that the TXCMDA register bits 7:6 should always remain at 0; bit 5 controls the SCDC override enable; and bits 4:0 contain the new short-circuit current-limit value. While adjustments can be made to the limit value, it is not advised as these values were chosen to prevent damage to the device.

Table 1. TXCMDA Register Settings

TS Mode Setting	TXCMDA Value
E1 75Ω	0x33
E1 120Ω	0x2F

Once these two configuration steps are completed, the DS26303 is properly configured to support the 2048kHz synchronization interface mode.

To program one or more channels of the DS26303 for 2048kHz synchronization interface mode, use the following software configuration.

- Set the ADDP register at address 0x1F to a value of 0x01 which will select the Individual LIU register bank.
- Set the G703EN register at address 0x08 to the value required to enable 2048kHz synchronization interface mode for the appropriate LIU channel.

Assuming now that the TTIP/TRING transmitter outputs are disabled as recommended earlier, enable the transmitter outputs using the following software configuration.

- Set the ADDP register at address 0x1F to a value of 0x00 which will select the Primary register bank.
- Set the OEB register at address 0x12 to the value required to enable the TTIP/TRING transmitter outputs for the same LIU channels enabled in the G703EN register.

Conclusion

With some minor changes to the default behavior of the DS26303, the device can fully support the ITU-T G.703 2048kHz synchronization interface (T12) specification. This application note describes what changes are necessary, provides background information on these changes, and presents detailed configuration procedures. This information and the DS26303 data sheet allow any designer to integrate the 2048kHz synchronization interface feature into a BITS or SSU design.

Appendix: DS26303 Required Register Information

The register space of the DS26303 spans address 0x00 to 0x1F. It uses a memory bank model, and contains configuration and status information for all LIU channels. The ADDP register at address 0x1F is a special register used as a pointer to access the different banks of registers. The function and value of this register remains the same for each register bank. However, changes to the ADDP register will change the current register bank, thereby altering the function and values of the registers that span address 0x00 to 0x1E.

Below is detailed information on the registers and a description of each bit that is needed to enable the ITU-T G.703 2048kHz synchronization interface (T12) mode.

Register Name: **ADDP**
Register Bank: **Exists In All Register Banks**
Register Description: **Address Pointer**
Register Address: **1Fh**

Bit #	7	6	5	4	3	2	1	0
Name	ADDP7	ADDP6	ADDP5	ADDP4	ADDP3	ADDP2	ADDP1	ADDP0
Default	0	0	0	0	0	0	0	0

Bit 7 to 0: Address Pointer (ADDP). This value is used as a pointer to select and switch among the Primary register bank, the Secondary register bank, Individual LIU register bank, BERT register bank, and any of the Test register banks. For example, the software must set the ADDP register to 0x00 for access to the Primary bank of registers; to 0xAA for access of the Secondary bank of registers; to 0x01 for access to the Individual LIU bank of registers; or to 0x02 for access of the BERT bank of registers. See **Table 2** for proper register bank selection.

Table 2. Address Pointer Register Bank Selection

ADDP Register Value	Register Bank Name
0x00	Primary
0xAA	Secondary
0x01	Individual LIU
0x02	BERT
0x03	Global Test
0x04	LIU1 Test
0x05	LIU2 Test
0x06	LIU3 Test
0x07	LIU4 Test
0x08	LIU5 Test
0x09	LIU6 Test
0x0A	LIU7 Test
0x0B	LIU8 Test

Register Name: **G703EN**
Register Bank: **Individual LIU Register Bank**
Register Description: **ITU-T G.703 2048kHz Synchronization Interface Enable**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	G703EN7	G703EN6	G703EN5	G703EN4	G703EN3	G703EN2	G703EN1	G703EN0
Default	0	0	0	0	0	0	0	0

Bit 7 to 0: G703 Enable (G703EN). When cleared to 0, the transmitter and receiver for the associated LIU channel are in normal T1/E1/J1 mode. When set to 1, the transmitter and receiver for the associated LIU channel are placed into ITU-T G.703 2048kHz synchronization interface (T12) mode.

Note: This feature is only available in device revision A2 and later.

Register Name: **TXCMDA**
Register Name: **LIU Test Register Banks 1 to 8**
Register Description: **Transmit Line Driver Custom Mode A**
Register Address: **05h**

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	SCDCOR	SCC4	SCC3	SCC2	SCC1	SCC0
Default	0	0	0	0	0	0	0	0

Bit 7 to 6: Reserved. This bit should remain cleared to 0.

Bit 5: Short-Circuit Detection Circuit Override (SCDCOR). When cleared to 0, the default line-driver current limits are enabled. When set to 1, the default line-driver current limits are overridden with the value set by SCC[4:0].

Bit 4 to 0: Short-Circuit Current (SCC[4:0]). When the short-circuit detection circuit override (SCDCOR) bit is set to 1, the binary weighted value of these 4 bits set the short-circuit detection circuit current limit. When the line driver current exceeds this value, the transmitter is disabled and the driver fault monitor status is set to a 1.

Note: This feature is only available in device revision A2 and later.

Register Name: **TXDIG**
Register Name: **Global Test Register Bank**
Register Description: **Transmit Digital Test Modes**
Register Address: **07h**

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	CLKS	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit 7 to 5: Reserved. This bit should remain reset to 0.

Bit 5: Clock Selection Mode (CLKS). When cleared to 0, the transmit clock source for each LIU channel is the master clock when the LIU channel is in the following modes: transmit all 1s, automatic transmit all 1s, ITU-T G.703 2048kHz synchronization interface (T12), and factory test. When set to 1, the transmit clock source for each LIU channel is the associated TCLK pin (or recovered clock if remote loopback is enabled) when the LIU channel is in any of these modes.

Bit 3 to 0: Reserved. These bits should remain cleared to 0.

Note: This feature is only available in device revision A2 and later.

Related Parts		
DS26303	3.3V, E1/T1/J1, Short-Haul, Octal Line Interface Unit	Free Samples