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REFERENCE SCHEMATIC 5740

HOW TO SELECT THE EXTERNAL COMPONENTS FOR AN AUTOMOTIVE SEPIC DC-DC REGULATOR

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Abstract: In this application note, we review the parameters and calculations needed in selecting the external components for optimal performance of the MAX16990/MAX16992 used in single-ended primary-inductor converter (SEPIC) configurations. A calculator is provided to help the user in the selection of external components, compensation design, and the evaluation of power-supply performance. A reference design, showing how the devices can be used in an automotive SEPIC application, is discussed as well as the optimal layout for this SEPIC regulator.

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Introduction

A high-voltage SEPIC controller, such as the MAX16990/MAX16992, has many applications in an automobile. It is commonly used as a front-end regulator to control the main system voltage during a cold or warm crank when the battery voltage falls or during a load dump when the battery voltage rises.

In this article, we examine how to implement an automotive high-voltage SEPIC DC-DC power supply using a 36V, automotive boost SEPIC controller. We explain how to select the external components for the MAX16990/MAX16992 to achieve the best system performance. Finally, we present a reference design for an automotive SEPIC DC-DC regulator.

Select the External Components

Basic Parameters

We begin with **Figure 1**, a typical SEPIC regulator circuit for an automobile. Our initial focus is on the basic parameters to define before you can select external components.

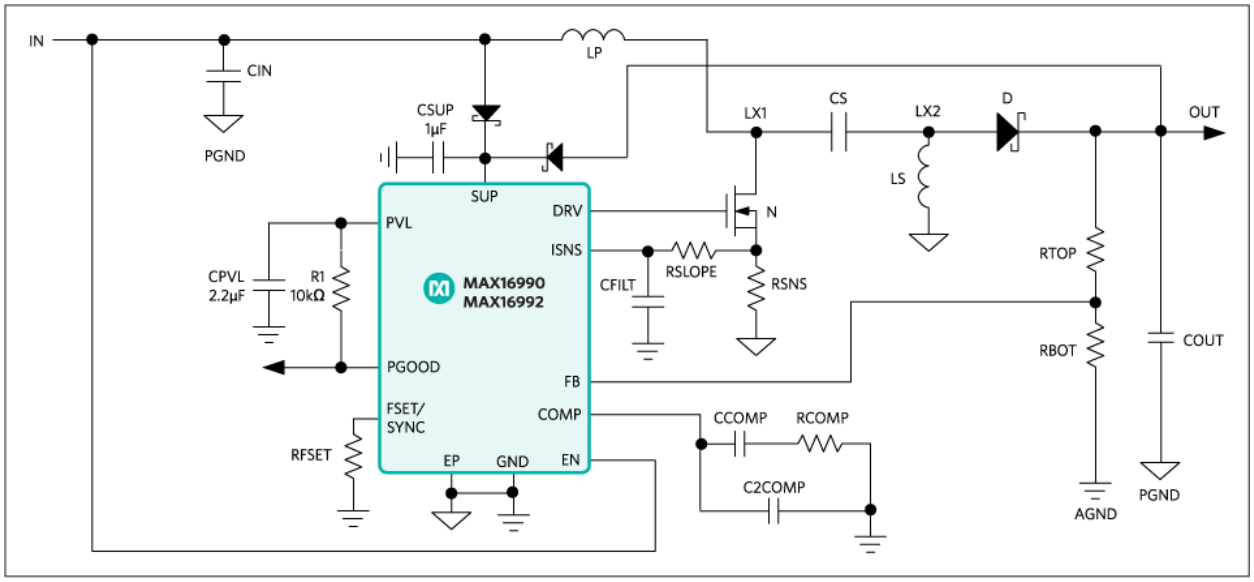

Figure 1. Typical application circuit for a SEPIC regulator. Here the example device is the MAX16990/MAX16992.

There are four principal design input parameters that influence the choice of external components:

1. Switching frequency (f_{SW})
2. Output voltage (V_{OUT})
3. Output current range (I_{OUTMIN} and I_{OUTMAX})
4. Input voltage range (V_{INMIN} and V_{INMAX})

The switching frequency is determined by the operating range of the controller used in your design. For this article and reference design we use the MAX16990, which has a 100kHz to 1MHz switching frequency range, and the MAX16992 with a 1MHz to 2.5MHz switching frequency range. Choose the controller and switching frequency best suited to your application.

Using the principal design input parameters, we estimate the average input current range with the following two equations:

$$V_{IN(AVG,MIN)} = (V_{OUT} \times I_{OUTMIN})/(V_{INMAX} \times Eff) \quad \text{(Eq. 1)}$$

$$I_{IN(AVG,MAX)} = (V_{OUT} \times I_{OUTMAX})/(V_{INMIN} \times Eff) \quad \text{(Eq. 2)}$$

where Eff is the estimated efficiency of the SEPIC regulator.

We assume an initial efficiency of 85% for 400kHz operation and an efficiency of 80% for 2.2MHz operation. Now specify all the external power components (nMOS, inductors, series capacitance, sense resistor, and rectifier diode), and then review and refine your design with a new useful calculator specifically created for the MAX16990/MAX16992.

Next, we evaluate the duty-cycle range (D_{MIN} and D_{MAX}) in which the regulator operates. This can be determined with the following two equations:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{INMAX} + V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times (I_{IN(AVGMIN)} + I_{OUTMIN})]} \quad \text{(Eq. 3)}$$

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{INMIN} + V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times (I_{IN(AVGMAX)} + I_{OUTMAX})]} \quad \text{(Eq. 4)}$$

where:
V_D is the forward voltage of the rectifier diode
$R_{DS(ON)}$ is the drain-source resistance of the nMOS when turned on
R_{SENSE} is the sense resistor.

You can ignore R_{SENSE} in the equations for now. We will make a more accurate estimate of the duty-cycle range later. Nonetheless, ensure that the estimated duty-cycle range is within the specification of the selected device, in this case 4% to 93% for the MAX16990 and 24% to 85% for the MAX16992.

Inductors
Calculate the critical inductance for Lp and Ls with Equations 5 and 6. Choose a commercial value that is always higher than the critical inductance. In this way you guarantee continuous-conduction mode (CCM) operation throughout the application.

$$Lp \geq Lp_C = \frac{(V_{OUT} + V_D) \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{IN(AVGMIN)}} \quad \text{(Eq. 5)}$$

$$Ls \geq Ls_C = \frac{(V_{OUT} + V_D) \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{OUTMIN}} \quad \text{(Eq. 6)}$$

Note that Lp_C and Ls_C halve their values if coupled inductors are used.

There is another parameter to remember when choosing proper inductors: the inductor current ripple ratio, or LIR. This parameter is defined as the ratio of the peak-to-peak inductor current and the average input current:

$$LIR = IL_{P-P}/IL_{(AVG)} \quad \text{(Eq. 7)}$$

The relationship between the inductors (Lp and Ls) and the LIR is shown in Equations 8 and 9:

$$Lp_{LIR} = \frac{(V_{OUT} + V_D) \times (1 - D)}{f_{SW} \times L \times I_{IN(AVG)}} \quad \text{(Eq. 8)}$$

$$Lp_{LIR} = \frac{(V_{OUT} + V_D) \times (1 - D)}{f_{SW} \times L \times I_{IN(AVG)}} \quad \text{(Eq. 9)}$$

Lp_{LIR} and Ls_{LIR} halve their values if coupled inductors are used.

To reduce losses choose an inductor that guarantees an LIR between 0.3 and 0.5. With L equal to L_C, the LIR is 2. By increasing L further, you reduce the LIR. The selected inductors need to have a saturation current higher than their respective peak current, which is:

$$ILp_{PEAK} = I_{IN(AVG)}(1 + Lp_{LIR}/2) \quad \text{(Eq. 10)}$$

$$ILsPEAK = IOUT(1 + LsLIR/2) \quad \text{(Eq. 11)}$$

Figures 2 and **3** illustrate the inductor's current shape during the switching period.

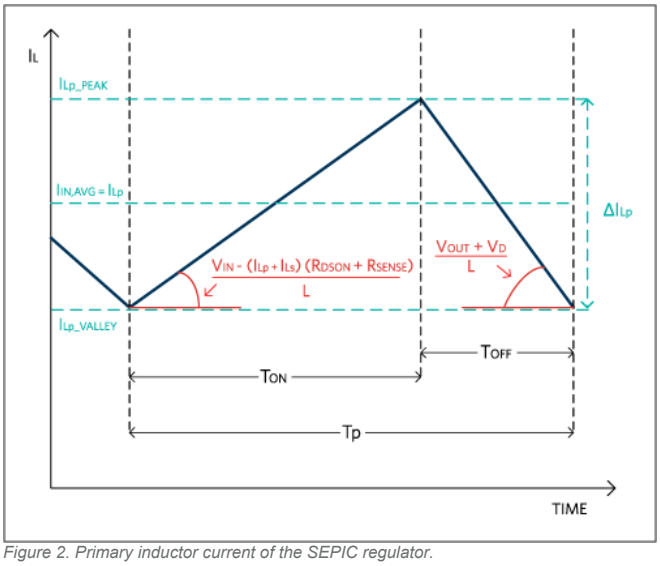

Figure 2. Primary inductor current of the SEPIC regulator.

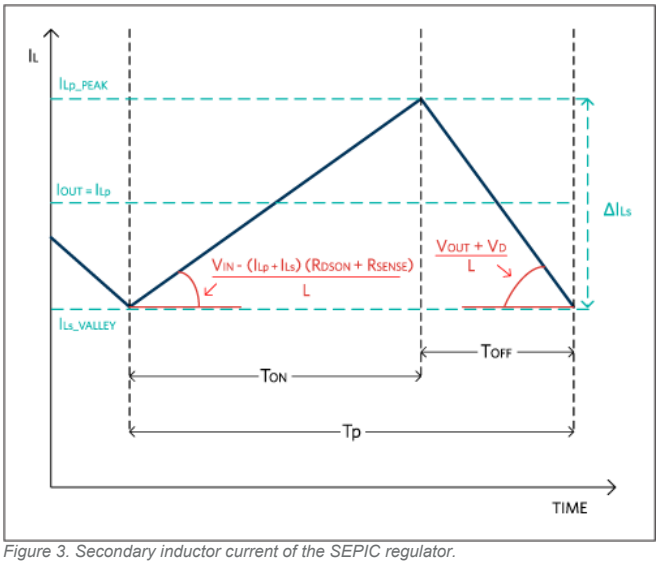

Figure 3. Secondary inductor current of the SEPIC regulator.

nMOS and Rectifier Diode

The peak nMOS drain current is the sum of the peak current of the two inductors:

$$InMOS_{PEAK} = ILp_{PEAK} + ILs_{PEAK} \quad \text{(Eq. 12)}$$

While the maximum drain-source voltage is equal to:

$$VnMOS_{DSMAX} = V_{INMAX} + V_D + V_{OUT} \quad \text{(Eq. 13)}$$

The average current that flows through the rectifier diode coincides with the output current, while the maximum reverse voltage is equal to:

$$V_{DREVMAX} = V_{INMAX} + V_{OUT} \quad \text{(Eq. 14)}$$

Choose the rating of the two power components according to the above formulas.

Sense Resistor

Now that the peak nMOS current has been calculated, it is possible to select the sense resistor (R_{SENSE}). The MAX16990/MAX16992 trigger the current limit when the voltage on the ISNS pin reaches 212mV (min). This voltage is due both to the drop on the sense resistor and to the drop on the slope resistor (R_{SLOPE}), the latter of which is used for slope compensation. To leave 100mV of room for slope compensation it is initially recommended that R_{SENSE} generates a voltage drop of 112mV at the current-limit threshold. In Equation 15, R_{SENSE} is calculated with a current-limit threshold 20% higher than the peak inductor current.

$$R_{SENSE} = 0.112/(1.2 \times InMOS_{PEAK}) \quad \text{(Eq. 15)}$$

Series Capacitor

The series capacitor is charged at a DC voltage equal to the input voltage. It must carry the primary inductor current during the off-time and the secondary inductor current during the on-time. This makes this capacitor selection challenging, even somewhat tricky.

As the first requirement the voltage rating of the series capacitor has to be higher than the maximum input voltage(V_{INMAX}).

The RMS current flowing through the capacitor is given by equation 16:

$$ICs_{RMS} = I_{OUTMAX} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad \text{(Eq. 16)}$$

The ripple across the series capacitor is determined by the capacitor value and its equivalent series resistance (ESR). Assuming a 1% voltage ripple across the series capacitor due to the ESR, the series capacitor ESR has to be lower than:

$$ESR_{CS} < MIN\left(\frac{0.01 \times V_{INMIN}}{IL_{PPEAK}}, \frac{0.01 \times V_{INMIN}}{IL_{SPEAK}}\right) \quad \text{(Eq. 17)}$$

Finally, the series capacitor value has to be high enough to guarantee a voltage ripple lower than 5%:

$$CS > \frac{I_{OUTMAX} \times D_{MAX}}{0.05 \times V_{INMIN} \times f_{SW}} \quad \text{(Eq. 18)}$$

Output Capacitor

Selecting the correct output capacitor (C_{OUT}) and its related ESR is very important for minimizing output voltage ripple. Assume that the output voltage ripple (V_{OUT_RIPPLE}) is equally distributed between the voltage drop, which is due to the capacitor discharging during off-time, and the ESR voltage drop. Use the following formulas to find the minimum capacitance and the maximum ESR for the output capacitor:

$$C_{OUT} > \frac{I_{OUTMAX} \times D_{MAX}}{0.5 \times V_{OUT\_RIPPLE} \times f_{SW}} \quad \text{(Eq. 19)}$$

$$ESR < \frac{0.5 \times V_{OUT\_RIPPLE}}{IL_{PPEAK} + IL_{SPEAK} - I_{OUT}} \quad \text{(Eq. 20)}$$

Compensation

After reviewing these external components, we need to consider the external compensation components needed for the SEPIC regulator. Unfortunately, the equations describing the closed-loop response of the SEPIC regulator are not easy to manage. For this reason we urge you to use the electronic calculator with the link above for selecting the compensation components R_{SLOPE}, R_{COMP}, C_{COMP}, and $C2_{COMP}$.

Once you have entered all your application conditions and power components, select a slope resistor (R_{SLOPE}) higher than the one estimated by the calculator.

Now complete the compensation section by inserting the input voltage, the output current, the selected output capacitor (both capacitance and ESR), the selected series resistor and, finally, the desired crossover frequency. The calculator will estimate the R_{COMP} and C_{COMP} values. Refine those values until a reasonable phase margin has been obtained. Once the selected C_{COMP} and R_{COMP} component values are entered in the calculator, it will plot the bode diagram.

SEPIC Regulator Reference Design

We can now examine a reference design for an automotive SEPIC regulator.

A possible usage for the SEPIC regulator would be as a main 5V/2A rail regulated directly from the battery voltage. Thanks to SEPIC architecture, the 5V rail will also be regulated during cold-crank and load-dump conditions.

For higher efficiency, in this reference design the MAX16990 is used at a 440kHz switching frequency. **Table 1** shows the summary of the design input parameters for this SEPIC regulator.

Table 1. Basic Input Parameters for the SEPIC Regulator in this Reference Design

f_{SW}	440kHz
V_{IN}	3V to 42V (minimum startup voltage is 5V)
V_{OUT}	5V
I_{OUT}	2A ±10%
V_{OUT_RIPPLE}	50mV

Suppose efficiency (Eff) of 85% and calculate the input current range that is equivalent to the primary inductor current range:

$$I_{IN(AVGMIN)} = I_{LP(AVGMIN)} = \frac{V_{OUT} \times I_{OUTMIN}}{V_{INMAX} \times Eff} = \frac{5 \times 1.8}{42 \times 0.85} = 0.252A \quad \text{(Eq. 21)}$$

$$I_{IN(AVGMAX)} = I_{LP(AVGMAX)} = \frac{V_{OUT} \times I_{OUTMAX}}{V_{INMIN} \times Eff} = \frac{5 \times 2.2}{3 \times 0.85} = 4.314A \quad \text{(Eq. 22)}$$

The secondary inductor average current range coincides with the output current range:

$$I_{Ls(AVGMIN)} = I_{OUTMIN} = 1.8A \quad \text{(Eq. 23)}$$

$$I_{Ls(AVGMAX)} = I_{OUTMAX} = 2.2A \quad \text{(Eq. 24)}$$

Now calculate the duty-cycle range. To do this, choose the external nMOS. To determine the nMOS ratings requirement, calculate the peak drain current that corresponds to the peak inductor current.

Assuming a maximum LIR of 0.5 when the input and output currents are at their maximum, then:

$$InMOS_{(PEAK(MAX,ESTIMATED)} = I_{IN(AVGMAX)}(1 + LIR/2) + I_{OUTMAX}(1 + LIR/2) = 8.143A \quad \text{(Eq. 25)}$$

Based on this information, a Fairchild™ FDS5670 nMOS rated for a drain current of 10A was chosen for Q. The typical $R_{DS(ON)}$ of this transistor is 15mΩ with a VGS = 5V (i.e., the gate-source voltage provided by the MAX16990). The rated drain-source voltage for this component is 60V, higher than the maximum drain-source voltage calculated by the following formula:

$$VnMOS_{DSMAX} = V_{INMAX} + V_D + V_{OUT} = 47.5V \quad \text{(Eq. 26)}$$

Assume that the forward voltage of the rectifier diode (a Diodes Incorporated B350-13-F) is equal to 0.5V. The maximum reverse voltage for this component is 50V, higher than the maximum reverse voltage required in this application:

$$V_{DREVMAX} = V_{INMAX} + V_{OUT} = 47V \quad \text{(Eq. 27)}$$

Once we have this information, we can calculate the duty-cycle range and ignore R_{SENSE} for now:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{INMAX} + V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times (I_{IN(AVGMIN)} + I_{OUTMIN})]} = 0.116 \quad \text{(Eq. 28)}$$

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{INMIN} + V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times (I_{IN(AVGMAX)} + I_{OUTMAX})]} = 0.655 \quad \text{(Eq. 29)}$$

This duty-cycle range is compatible with the MAX16990. To guarantee continuous-conduction mode:

$$Lp \geq Lp_C = \frac{(V_{OUT} + V_D) \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{IN(AVGMIN)}} = 21.9\mu H \quad \text{(Eq. 30)}$$

$$Ls \geq Ls_C = \frac{(V_{OUT} + V_D) \times (1 - D_{MIN})}{2 \times f_{SW} \times I_{OUTMIN}} = 3.07\mu H \quad \text{(Eq. 31)}$$

Based on this information, a Würth Elektronik 22µH inductor 7443551221 was selected for Lp (I_R = 6A, I_{SAT} = 6.5A) and a Würth Elektronik 4.7µH inductor 744311470 was selected for Ls (I_R = 15A, I_{SAT} = 19A). Using these inductors, when the input voltage is at its minimum and the output current at its maximum, therefore:

$$Lp_{LIR} = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{f_{SW} \times Lp \times I_{IN(AVGMAX)}} = 0.045 \quad \text{(Eq. 32)}$$

$$Ls_{LIR} = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{f_{SW} \times Ls \times I_{OUTMAX}} = 0.418 \quad \text{(Eq. 33)}$$

This results in inductors and nMOS peak current of:

$$ILp_{PEAK} = I_{IN(AVGMAX)}(1 + Lp_{LIR}/2) = 4.411A \quad \text{(Eq. 34)}$$

$ILs_{PEAK} = I_{OUTMAX}(1 + Ls_{LIR}/2) = 2.660A$ (Eq. 35)

$InMOS_{PEAK} = ILp_{PEAK} + ILs_{PEAK} = 7.071A$ (Eq. 36)

The nMOS drain-current rating and the inductors' current rating are compliant with the values given by Equations 34, 35, and 36.

Now calculate the series capacitor with the following formula, and then choose a commercial value higher than that:

$$CS > \frac{I_{OUTMAX} \times D_{MAX}}{0.05 \times V_{INMIN} \times f_{SW}} = 21.8\mu F$$ (Eq. 37)

The ESR of the series capacitor must be lower than the one calculated with the following formula:

$$ESR_{CS} < MIN\left(\frac{0.01 \times V_{INMIN}}{ILp_{PEAK}}, \frac{0.01 \times V_{INMIN}}{ILs_{PEAK}}\right) = \frac{0.01 \times V_{INMIN}}{ILp_{PEAK}} = 6.8m\Omega$$ (Eq. 38)

The voltage rate has to be higher than 42V and the capacitor current rate has to be higher than:

$$ICs_{RMS} = I_{OUTMAX} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 3.031A$$ (Eq. 39)

For these reasons a TDK® C5750Y5V1H226ZT 22µF ceramic capacitor was selected.

Now it is possible to calculate the sense resistor:

$$R_{SENSE} = \frac{0.112}{1.2 \times InMOS_{PEAK(MAX)}} = 13.1m\Omega$$ (Eq. 40)

A 15mΩ resistor was chosen for R_{SENSE}.

In accordance with the design specification on the output voltage ripple, the constraints on C_{OUT} are:

$$C_{OUT} > \frac{I_{OUTMAX} \times D_{MAX}}{0.5 \times V_{OUT\_RIPPLE} \times f} = 65.5\mu F$$ (Eq. 41)

$$ESR < \frac{0.5 \times V_{OUT\_RIPPLE}}{ILp_{PEAK} + ILs_{PEAK} - I_{OUTMAX}} = 10.2m\Omega$$ (Eq. 42)

Consequently, two Murata® 47µF GRM32ER61C476K ceramic capacitors with an ESR of 5mΩ at the 440kHz switching frequency were chosen.

Using the electronic calculator it is now possible to extrapolate the following component values for compensation so we can obtain a crossover frequency of 3kHz with a phase margin of 60 degrees:

$R_{SLOPE} = 2k\Omega$
$C_{COMP} = 33nF$
$R_{COMP} = 3k\Omega$

Figure 4 shows a schematic of this reference design and the selected external components, and **Figure 5** shows the design in a three-dimensional view.

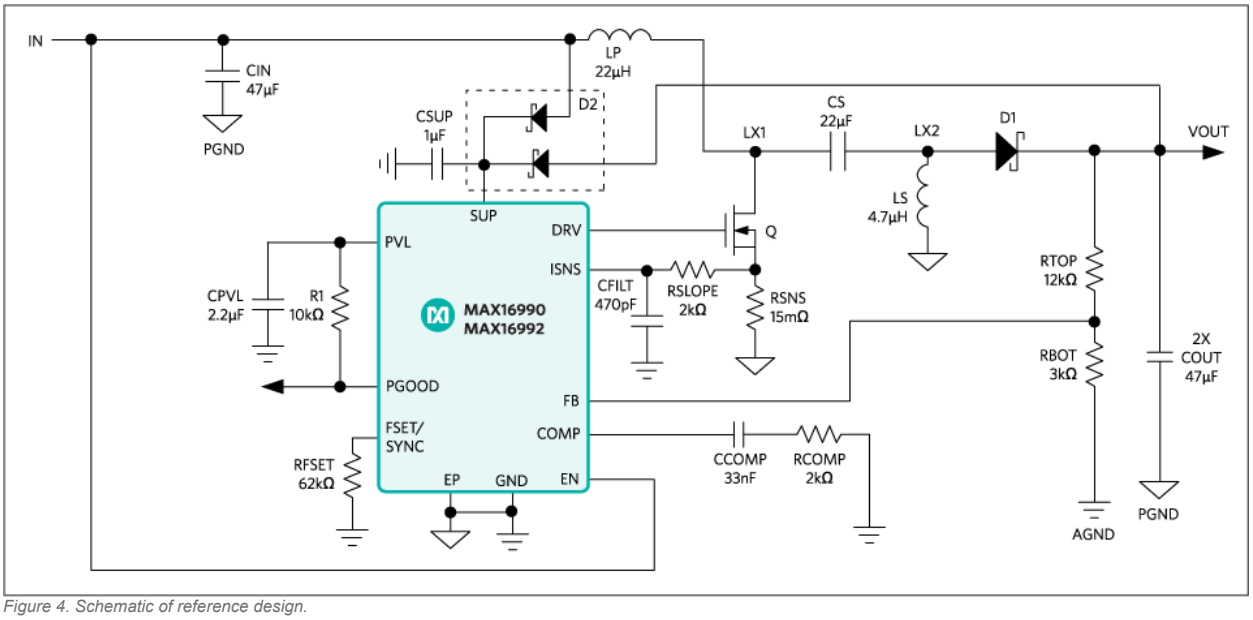

Figure 4. Schematic of reference design.

Layout Recommendation

A good layout is very important to maximize EMI and jitter-free performance of the boost regulator. To achieve that, follow these general recommendations:

1. Place all power components on the same side of the board.
2. Keep the AC paths as short as possible. During on-time, the first AC path is composed of C_{IN}, L1 inductor, nMOS, R_{SENSE}, and GND; the second AC path is composed of L2 inductor, CS capacitor, nMOS, R_{SENSE}, and GND. During off-time, the first AC path is composed of C_{IN}, L1 inductor, CS capacitor, D1 diode, C_{OUT}, and GND; the second AC path is composed of L2 inductor, D1 diode, C_{OUT}, and GND.
3. Keep the switching nodes (LX1 and LX2) as compact as possible.
4. Do not route the path between the DRV pin and the gate of the nMOS with the minimum width. This net commutes at the switching frequency and has to carry the current necessary to drive the nMOS. If vias are necessary, route the net to an internal layer.
5. Connect the C_{SUP} and C_{PVL} capacitors directly to the IC, as close as possible without using vias.
6. Use a Kelvin connection between R_{SENSE} and R_{SLOPE}, and between R_{SLOPE} and the ISNS pin.
7. Use a Kelvin connection between VOUT and R_{TOP}. Keep the FB node as close as possible to the FB pin of the IC.
8. Use two separate GNDs as indicated on the schematic: PGND for power components and AGND for the signal circuitry and the EP of the MAX16992. Use a single-point connection between PGND and AGND, as close as possible to the EP.

A reference layout is shown in **Figures 5** through **Figure 9**.

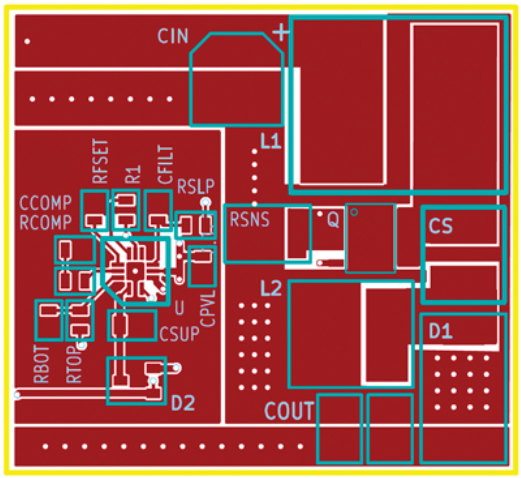

Figure 5. Reference design layout, top layer.

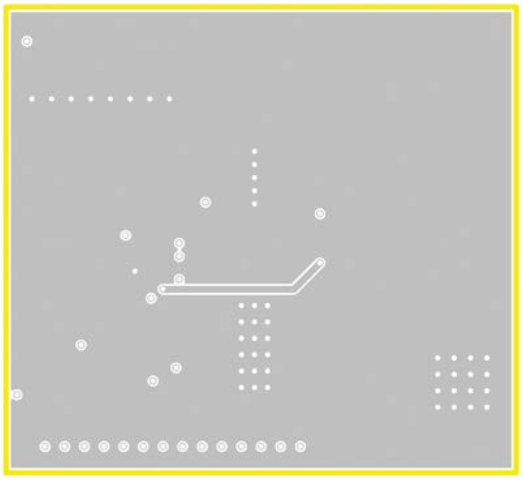

Figure 6. Reference design layout, inner layer 1.

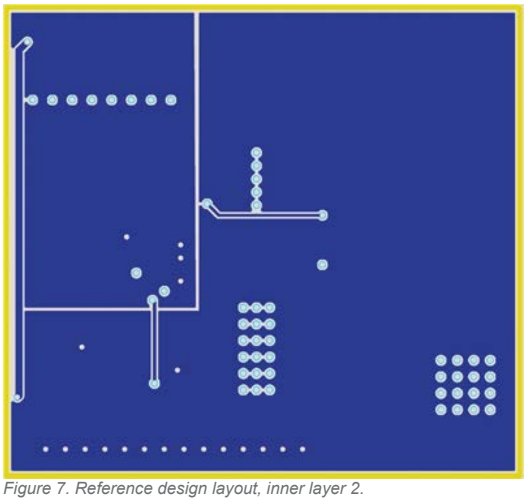

Figure 7. Reference design layout, inner layer 2.

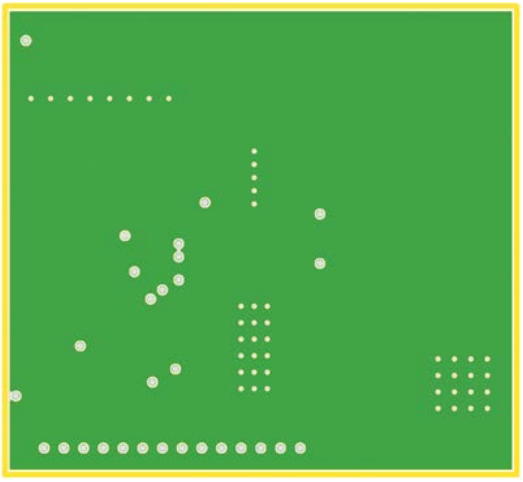

Figure 8. Reference design layout, back layer.

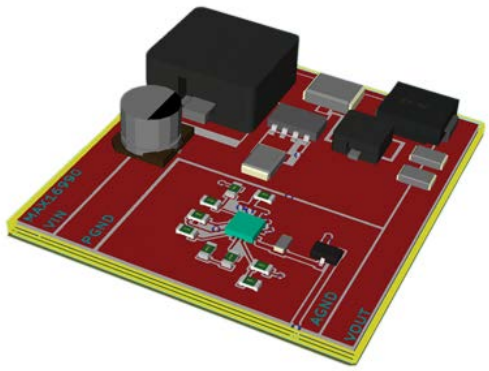

Figure 9. Reference design, three-dimensional view.

Lab Test Results

Regulator Efficiency

The efficiency of the SEPIC regulator at full load versus input voltage (V_{IN}) is shown in **Figure 10**.

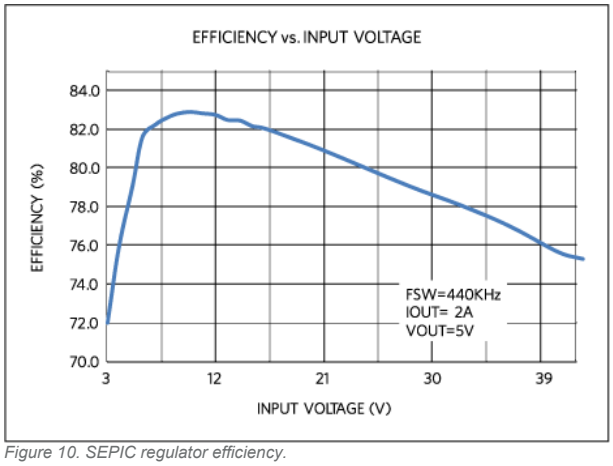

Figure 10. SEPIC regulator efficiency.

Cold Crank

Figures 11 and **12** show the SEPIC regulator's behavior during an automotive cold-crank event, where the battery voltage goes down to 3V. In this reference design the dual-diode D2 is used to supply the input voltage to the MAX16990 from the converter's output when the battery voltage falls below the minimum input voltage of the controller IC.

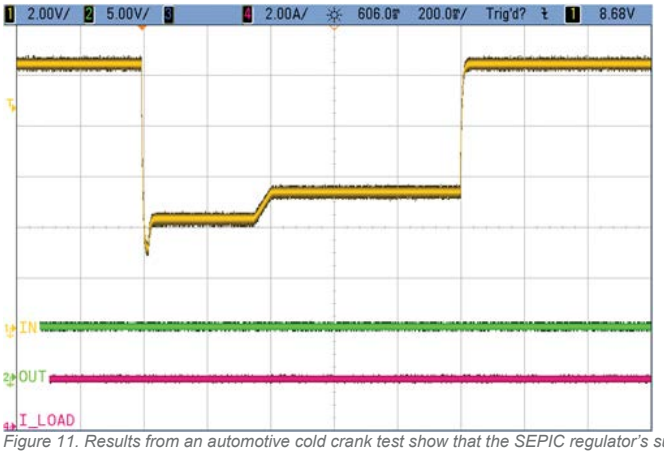

Figure 11. Results from an automotive cold crank test show that the SEPIC regulator's supply is a very stable 5V/2A rail during the automotive cold crank event.

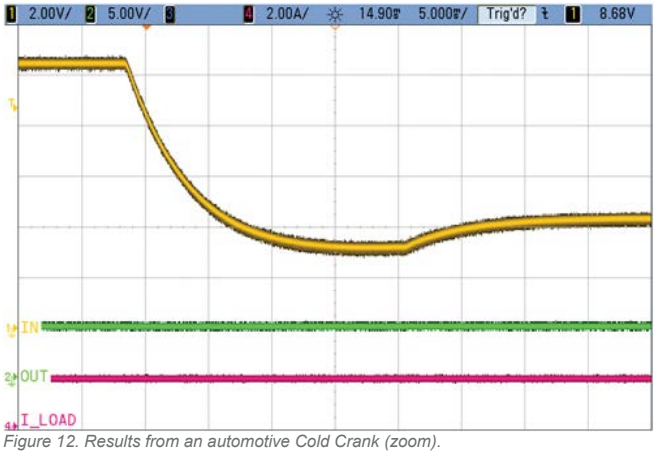

Figure 12. Results from an automotive Cold Crank (zoom).

Conclusion

We learned how best to select the external components and compensation to optimize the performance of an automotive SEPIC DC-DC regulator. Using the MAX16990/MAX16922 as example SEPIC converters, we demonstrated a SEPIC DC-DC regulator reference design for automotive applications. Test data illustrate the excellent performance of the reference design.

Related Parts		
MAX16990	36V, 2.5MHz Automotive Boost/SEPIC Controllers	Free Samples
MAX16992	36V, 2.5MHz Automotive Boost/SEPIC Controllers	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/en/support For Samples: http://www.maximintegrated.com/en/samples
Other Questions and Comments: http://www.maximintegrated.com/en/contact

Application Note 5740: http://www.maximintegrated.com/en/an5740