

Automotive IPD Series

# Built-in Output Diagnosis 1ch High Side Switch

## BV1HLC45EFJ-C

### General Description

BV1HLC45EFJ-C is a 1ch high side switch for automotive application. It has a built-in overcurrent limit function, thermal shutdown protection function, open load detection function, low power output-OFF function and short-to-VCC detection function. It is equipped with diagnostic output function for abnormality detection.

### Features

- Built-in Dual TSD<sup>(Note 1)</sup>
- AEC-Q100 Qualified<sup>(Note2)</sup>
- Built-in Overcurrent Protection Function (OCP)
- Built-in Thermal Shutdown Protection Function (TSD)
- Built-in Open Load Detection Function
- Built-in Short-to-VBB Detection Function
- Built-in Low Voltage Output OFF Function (UVLO)
- Built-in Reverse Battery Connection Protection
- Built-in Diagnostic Output
- Low On-Resistance Single Nch MOSFET Switch
- Monolithic power management IC with control unit (CMOS) and power MOSFET mounted on a single chip

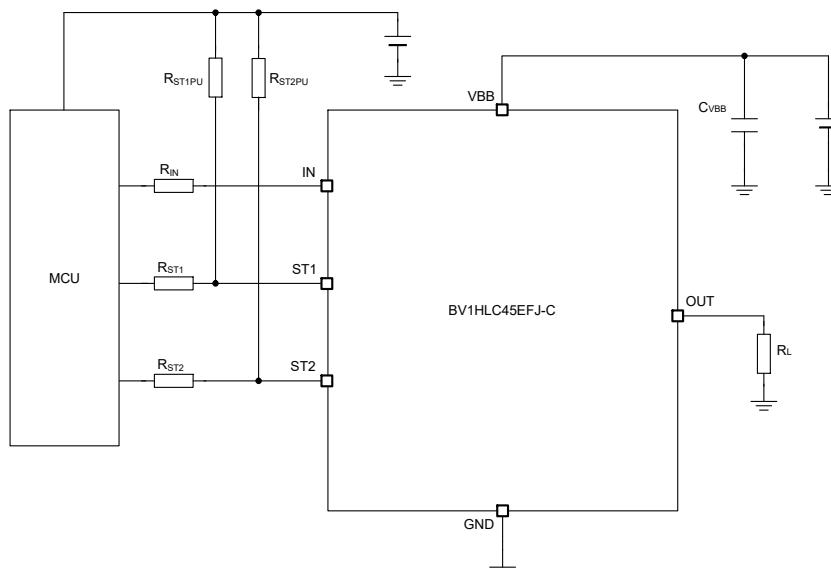
(Note 1) Two type of built-in temperature protection: Junction temperature, and  $\Delta T_J$  protection that detects sudden temperature rise of the Power-MOS

(Note 2) Grade 1

### Application

- Resistance load, inductance load and capacitance load for automotive application

### Typical Application Circuit



### Key Specifications

■ Power Supply Operating Range	6 V to 28 V
■ ON-Resistance (T <sub>J</sub> = 25 °C)	45 mΩ (Typ)
■ Overcurrent Limit	2.5 A (Min)
■ Standby Current (T <sub>J</sub> = 25 °C)	0.5 μA (Max)
■ Active Clamp Tolerance (T <sub>J</sub> = 25 °C)	120 mJ

Package  
HTSOP-J8

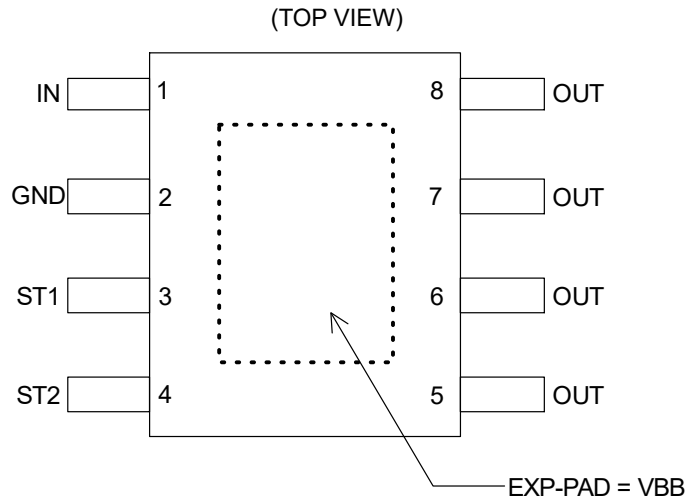
W (Typ) x D (Typ) x H (Max)  
4.9 mm x 6.0 mm x 1.0 mm



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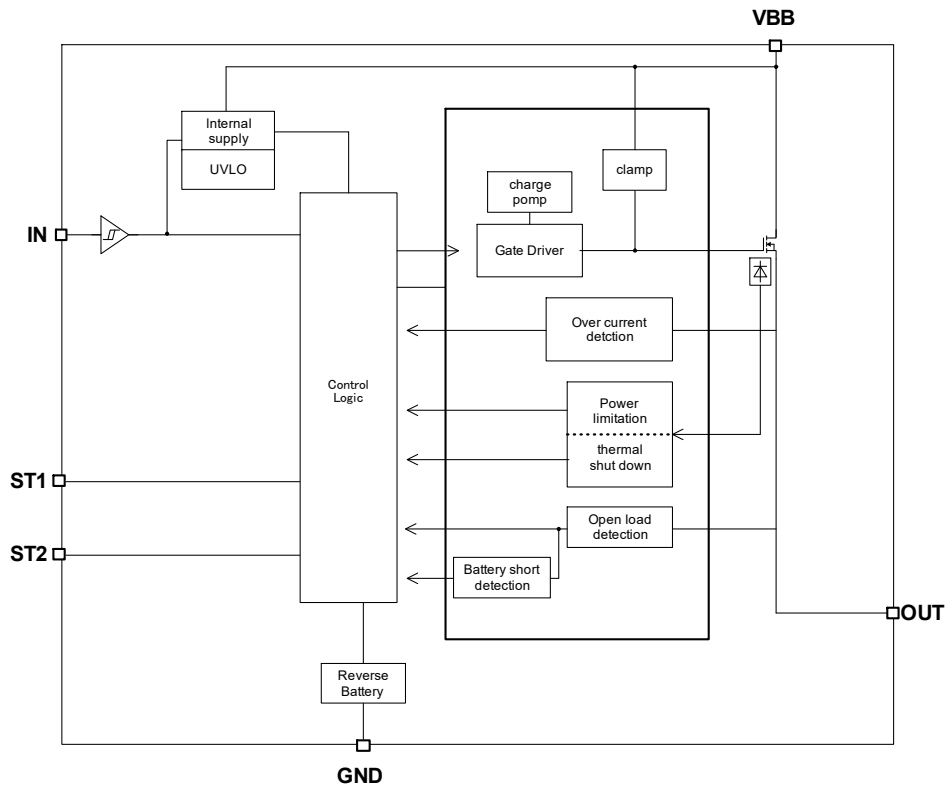
Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	IN	Input pin. Pull-down resistor is connected internally. Active High to turn on the switch.
2	GND	Ground pin
3	ST1	Self-diagnostic output pin 1
4	ST2	Self-diagnostic output pin 2
5	OUT	Switch output pin
6	OUT	Switch output pin
7	OUT	Switch output pin
8	OUT	Switch output pin
EXP-PAD	VBB	Power input pin, switch input pin

Block Diagram



Definition

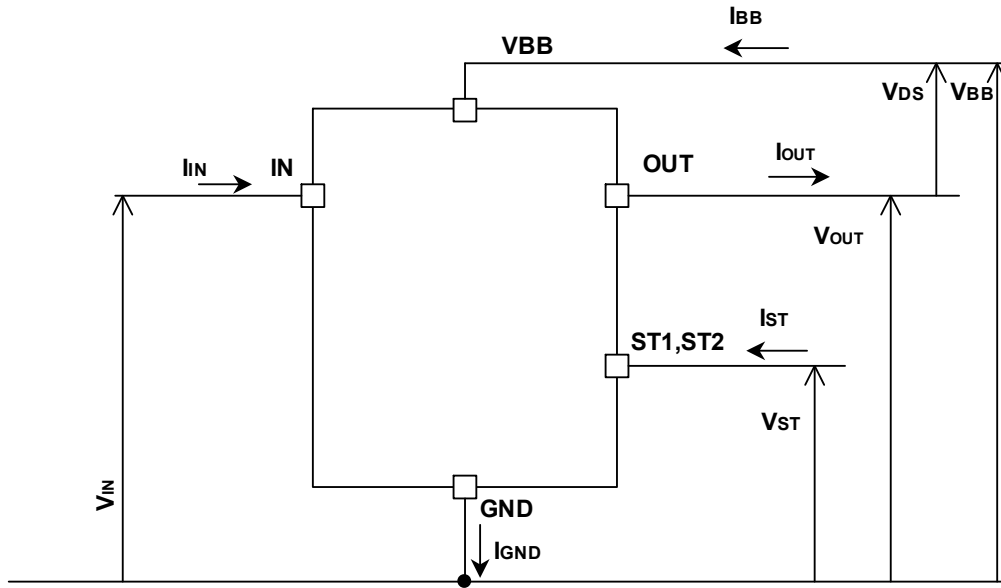


Figure 1. Voltage and Current Definition

## Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VBB - OUT Voltage	V <sub>DS</sub>	-0.3 to Internal clamp <sup>(Note 1)</sup>	V
Power Supply Voltage	V <sub>BB</sub>	-0.3 to +40	V
Input Voltage	V <sub>IN</sub>	-0.3 to +7.0	V
Diagnostic Output Voltage	V <sub>ST</sub>	- 0.3 to +7.0	V
Output Current	I <sub>OUT</sub>	Internal limit <sup>(Note 2)</sup>	A
Diagnostic Output Current	I <sub>ST</sub>	10	mA
Junction Temperature Width	T <sub>J</sub>	-40 to +150	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Maximum Junction Temperature	T <sub>jmax</sub>	+150	°C
Active Clamp Energy (Single Pulse) T <sub>J(START)</sub> = 25 °C, I <sub>OUT</sub> = 4 A <sup>(Note 3) (Note 4)</sup>	E <sub>AS</sub> (25 °C)	120	mJ
Active Clamp Energy (Single Pulse) T <sub>J(START)</sub> = 150 °C, I <sub>OUT</sub> = 4 A <sup>(Note 3) (Note 4)</sup>	E <sub>AS</sub> (150 °C)	60	mJ
Supply Voltage for Short Circuit Protection <sup>(Note 5)</sup>	V <sub>BBLIM</sub>	28	V
Supply Voltage for Reverse-Battery Connection Protection	V <sub>RBPLIM</sub>	18	V

(Note 1) Internally limited by output clamp voltage.

(Note 2) Internally limited by fixed over current limit.

(Note 3) Maximum active clamp energy using single pulse of I<sub>OUT(START)</sub> = 2 A and V<sub>BB</sub> = 14 V.

(Note 4) Not 100% tested.

(Note 5) Maximum power supply voltage that can detect short circuit protection.

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

**Caution 3:** When IC turns off with an inductive load, reverse energy is generated. This energy can be calculated by the following equation:

$$E_L = \frac{1}{2} \times L \times I_{OUT(START)}^2 \times \left( 1 - \frac{V_{BB}}{V_{BB} - V_{DS}} \right)$$

Where:

L is the inductance of the inductive load.

I<sub>OUT(START)</sub> is the output current at the time of turning off.

The BV1HLC45EFJ-C integrates the active clamp function to internally absorb the reverse energy E<sub>L</sub> which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E<sub>L</sub> is active clamp tolerance E<sub>AS</sub> (refer to Figure 24. Active Clamp Energy vs Output Current) or under when inductive load is used.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Operating Range	V <sub>BB</sub>	6	14	28	V
Operating Temperature	T <sub>opr</sub>	-40	-	+150	°C
Input Frequency	f <sub>IN</sub>	-	-	1	kHz

**Thermal Resistance** (Note 1)

Parameter	Symbol	Typ	Unit	Condition
HTSOP-J8				
Between Junction and Surroundings Temperature Thermal Resistance	$\theta_{JA}$	130.3	°C/W	1s (Note 2)
		36.8	°C/W	2s (Note 3)
		25.9	°C/W	2s2p (Note 4)
Between Junction and the top center of the outside surface of the component package Thermal Characterization Parameter (Note 5)	$\Psi_{JT}$	20	°C/W	1s (Note 2)
		8	°C/W	2s (Note 3)
		6	°C/W	2s2p (Note 4)

(Note 1) The thermal impedance is based on JESD51-2A (Still-Air) standard. It is used the chip of BV1HLC45EFJ-C.

(Note 2) JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)  
 (Top copper foil: ROHM recommended Footprint + wiring to measure, 2 oz. copper.)

(Note 3) JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layers (2s)  
 (Top copper foil: ROHM recommended Footprint + wiring to measure/  
 Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,  
 copper (top & reverse side) 2 oz)

(Note 4) JESD51-5/-7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p)  
 (Top copper foil: ROHM recommended Footprint + wiring to measure/  
 2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,  
 copper (top & reverse side/inner layers) 2 oz/1 oz)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

■ PCB Layout 1 layer (1s)

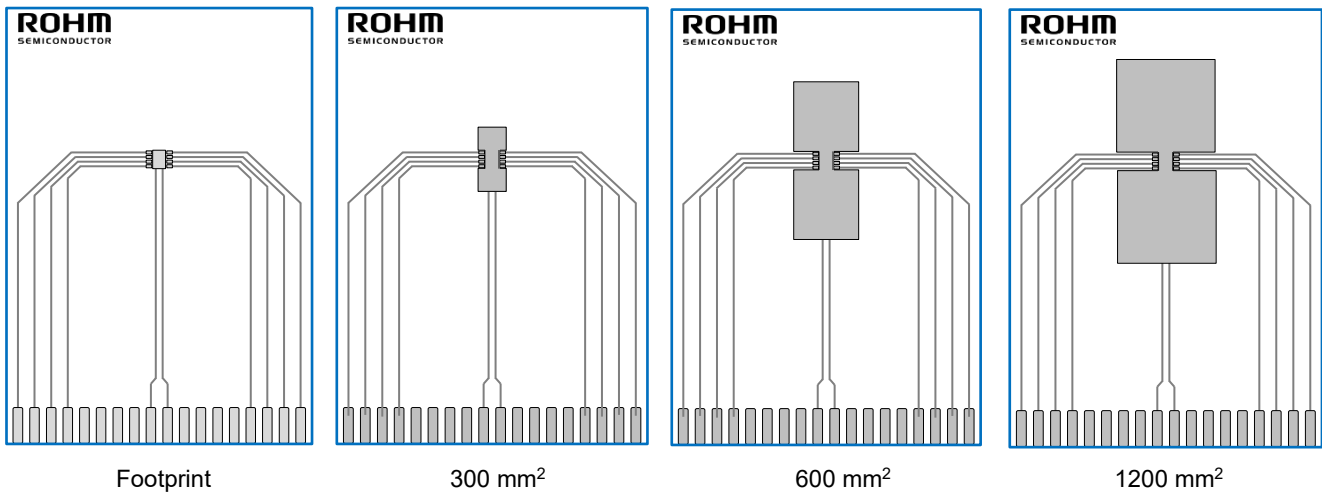


Figure 2. PCB Layout 1 Layer (1s)

Dimension	Value
Board Finish Thickness	1.57 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top Layer)	0.070 mm (Cu: 2 oz)
Copper Foil Area Dimension	Footprint/100 mm²/600 mm²/1200 mm²

Thermal Resistance – continued

- PCB Layout 2 layers (2s)

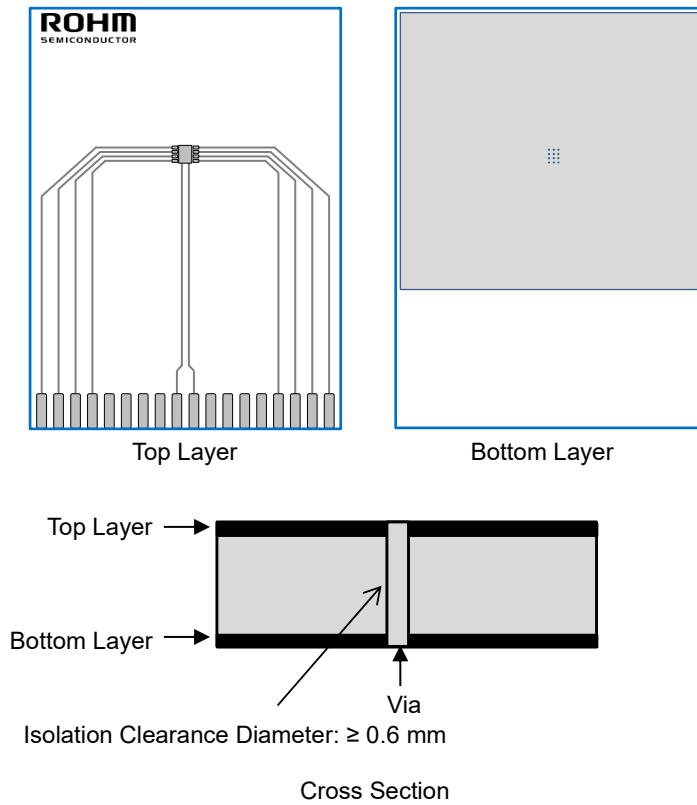
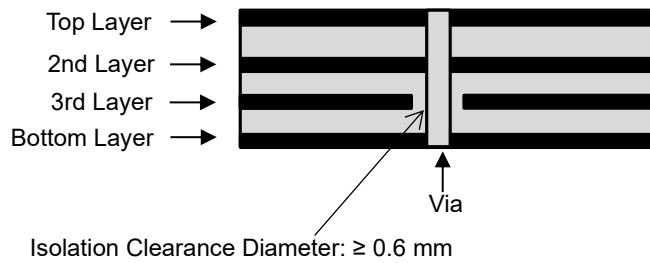
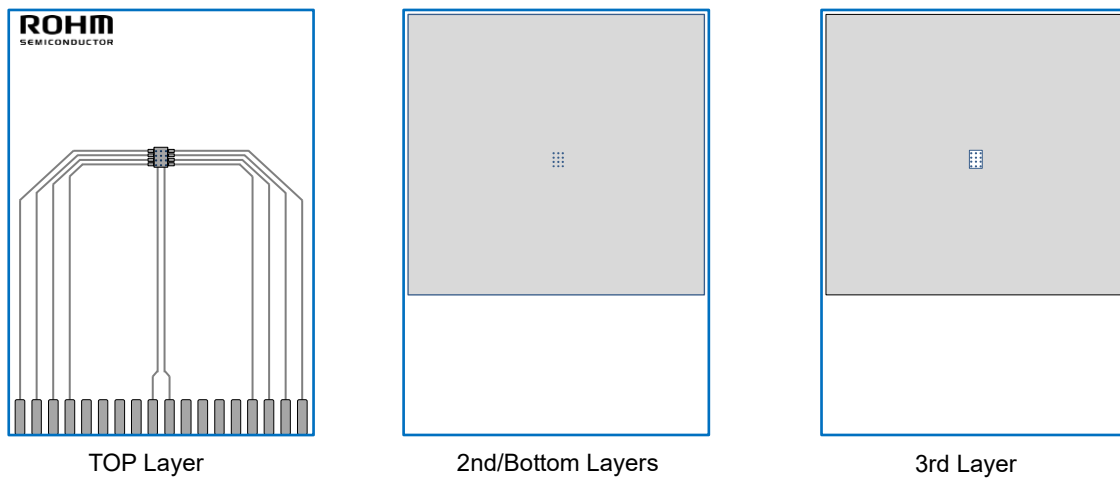


Figure 3. PCB Layout 2 Layers (2s)

Dimension	Value
Board Finish Thickness	1.60 mm $\pm$ 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu + Plating)
Thermal Via Separation/Diameter	1.2 mm/0.3 mm

Thermal Resistance – continued

- PCB Layout 4 layers (2s2p)



Cross Section

Figure 4. PCB Layout 4 Layers (2s2p)

Dimension	Value
Board Finish Thickness	1.60 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu + Plating)
Copper Thickness (Inner Layers)	0.035 mm
Thermal Vias Separation/Diameter	1.2 mm/0.3 mm



Thermal Resistance – continued

- Transient Thermal Resistance (Single Pulse)

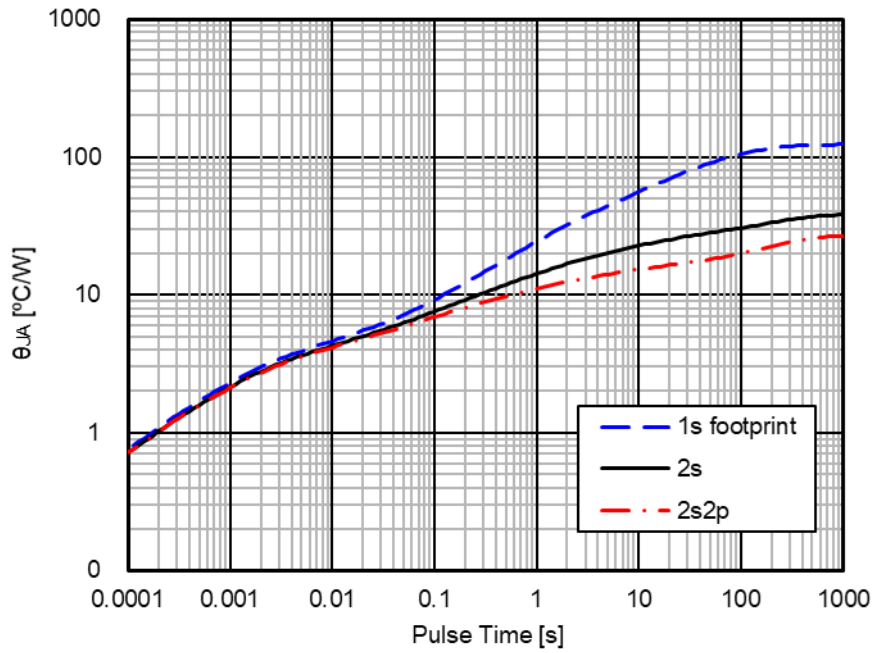


Figure 5. Transient Thermal Resistance

- Thermal Resistance ( $\theta_{JA}$  vs Copper foil area- 1s)

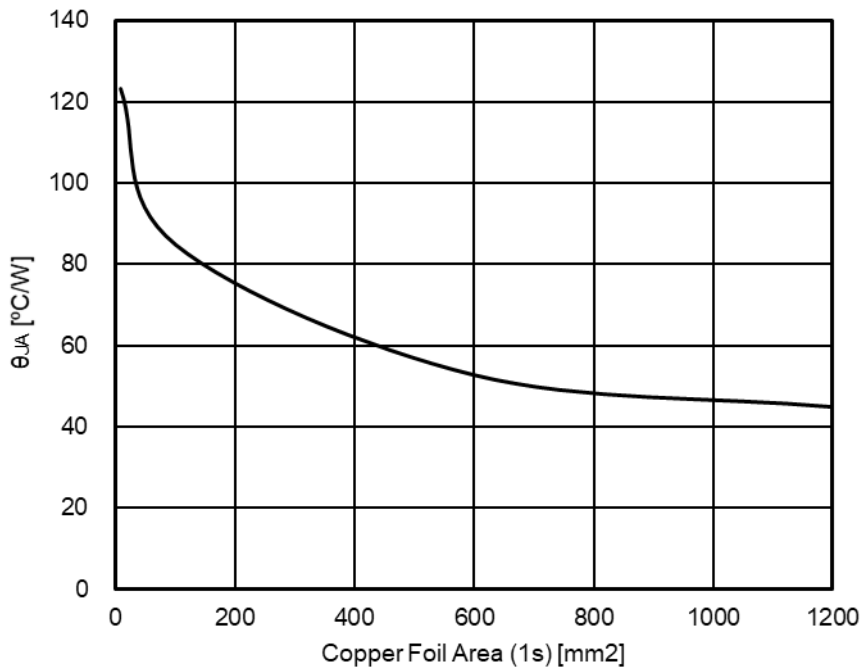


Figure 6. Thermal Resistance

Electrical Characteristics (unless otherwise specified  $V_{BB} = 6\text{ V to }28\text{ V}$ ,  $T_j = -40\text{ °C to }150\text{ °C}$ )

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
<b>Power Supply</b>						
Standby current	$I_{BBL1}$	-	-	0.5	$\mu\text{A}$	$V_{BB} = 14\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 25\text{ °C}$
	$I_{BBL2}$	-	-	20	$\mu\text{A}$	$V_{BB} = 14\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 150\text{ °C}$
Operating Current	$I_{BBH}$	-	2.0	3.5	$\text{mA}$	$V_{BB} = 14\text{ V}$ , $V_{IN} = 5\text{ V}$ , $V_{OUT} = \text{open}$
UVLO Detection Voltage	$V_{UVLO}$	-	-	5.0	$\text{V}$	
UVLO Hysteresis Voltage	$V_{UVHYS}$	-	-	1.0	$\text{V}$	
<b>Input</b>						
High Level Input Voltage	$V_{INH}$	2.1	-	-	$\text{V}$	
Low Level Input Voltage	$V_{INL}$	-	-	0.9	$\text{V}$	
Input Hysteresis Voltage	$V_{HYS}$	-	0.3	-	$\text{V}$	
High Level Input Current	$I_{INH}$	-	50	150	$\mu\text{A}$	$V_{IN} = 5\text{ V}$
Low Level Input Current	$I_{INL}$	-10	-	+10	$\mu\text{A}$	$V_{IN} = 0\text{ V}$
<b>Power MOS Output</b>						
Output ON Resistance	$R_{ON1}$	-	45	60	$\text{m}\Omega$	$V_{BB} = 8\text{ V to }28\text{ V}$ , $T_j = 25\text{ °C}$
	$R_{ON2}$	-	-	90	$\text{m}\Omega$	$V_{BB} = 8\text{ V to }28\text{ V}$ , $T_j = 150\text{ °C}$
	$R_{ON3}$	-	-	75	$\text{m}\Omega$	$V_{BB} = 6\text{ V}$ , $T_j = 25\text{ °C}$
Output Leak Current	$I_{OUTL1}$	-	-	0.5	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 25\text{ °C}$
	$I_{OUTL2}$	-	-	10	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 150\text{ °C}$
Output Slew Rate when ON	$SR_{ON}$	-	0.3	1.0	$\text{V}/\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\ \Omega$
Output Slew Rate when OFF	$SR_{OFF}$	-	0.3	1.0	$\text{V}/\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\ \Omega$
Propagation Delay when ON	$t_{OUTON}$	-	60	120	$\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\ \Omega$
Propagation Delay when OFF	$t_{OUTOFF}$	-	60	120	$\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\ \Omega$
Output Clamp Voltage	$V_{DS}$	45	50	55	$\text{V}$	$V_{IN} = 0\text{ V}$ , $I_{OUT} = 10\text{ mA}$
<b>Diagnostics</b>						
Diagnostic Output L Voltage	$V_{STL}$	-	-	0.5	$\text{V}$	$I_{ST} = 1\text{ mA}$
Diagnostic Output Leak Current	$I_{STL}$	-	-	10	$\mu\text{A}$	$V_{ST} = 5\text{ V}$
Propagation Delay Time when Diagnostic Output is ON	$t_{STON}$	-	120	240	$\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\ \Omega$
Propagation Delay Time when Diagnostic Output is OFF	$t_{STOFF}$	-	50	100	$\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\ \Omega$
<b>Protection Circuit</b>						
Overcurrent Limit Value	$I_{LIM}$	2.5	4.0	5.5	$\text{A}$	$V_{DS} = 5\text{ V}$
Overcurrent Detect Value 1 (Note 1)	$I_{OCD1}$	2.5	-	10.0	$\text{A}$	$T_j = -40\text{ °C}$
Overcurrent Detect Value 2 (Note 1)	$I_{OCD2}$	2.5	-	5.8	$\text{A}$	$T_j = 150\text{ °C}$
Short-to-VCC Detection Voltage	$V_{SHV}$	$V_{BB}-1.8$	$V_{BB}-1.2$	$V_{BB}-0.5$	$\text{V}$	$V_{IN} = 0\text{ V}$
Load Open Detection Voltage	$V_{OLD}$	2.0	3.0	4.0	$\text{V}$	$V_{IN} = 0\text{ V}$
Load Open Detection Sink Current	$I_{OLD}$	-	10	30	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{OUT} = 5\text{ V}$
Thermal Shutdown (Note 2)	$T_{TSD}$	150	175	200	$\text{°C}$	
Thermal Shutdown Hysteresis (Note 2)	$T_{TSDHYS}$	-	15	-	$\text{°C}$	
$\Delta T_j$ Protection Temperature (Note 2)	$T_{DTJ}$	-	120	-	$\text{°C}$	

(Note 1) Max value is not 100% tested.

(Note 2) Not 100% tested.

Typical Performance Curves

(Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $I_N = 5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

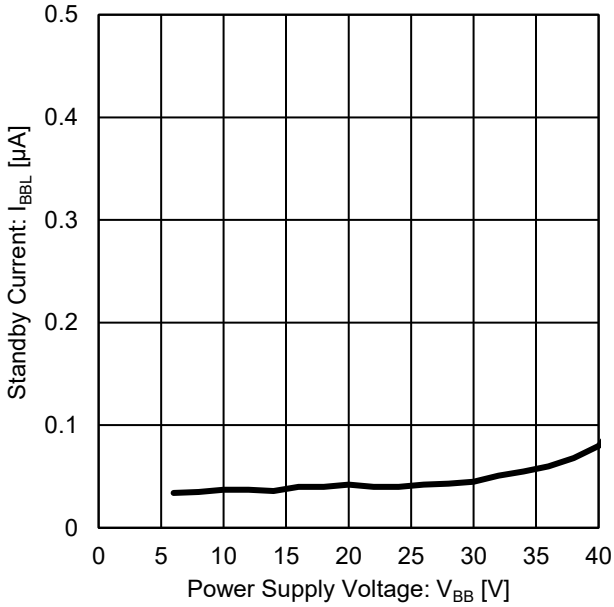


Figure 7. Standby Current vs Power Supply Voltage

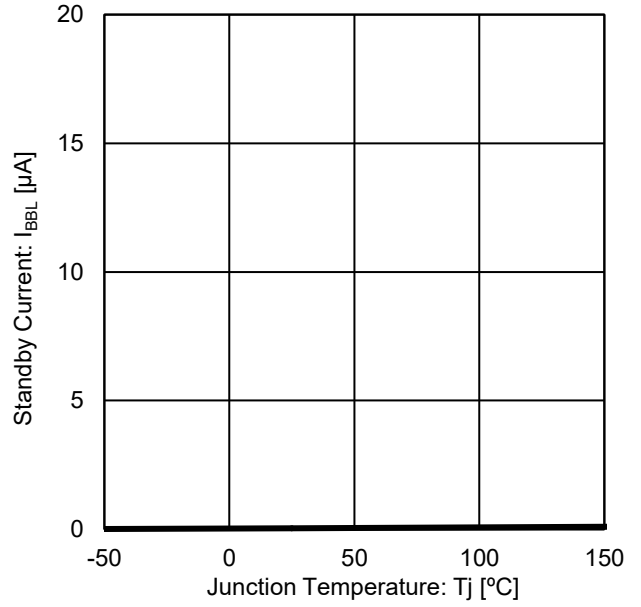


Figure 8. Standby Current vs Junction Temperature

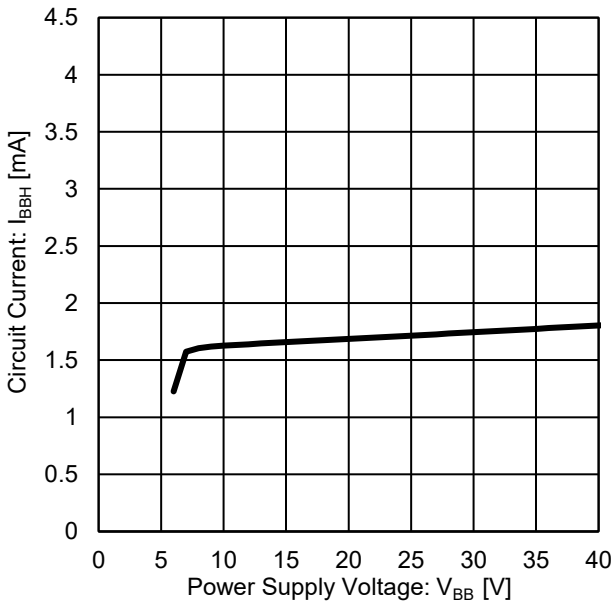


Figure 9. Circuit Current vs Power Supply Voltage

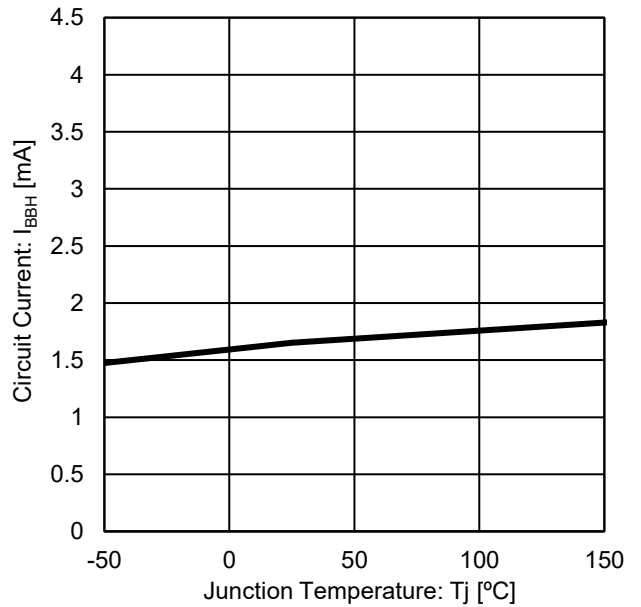


Figure 10. Circuit Current vs Junction Temperature

Typical Performance Curves - continued

(Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $I_N = 5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

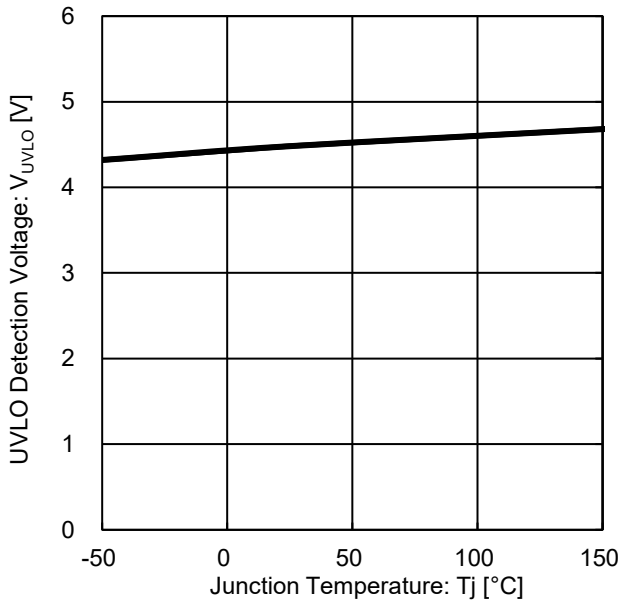


Figure 11. UVLO Detection Voltage vs Junction Temperature

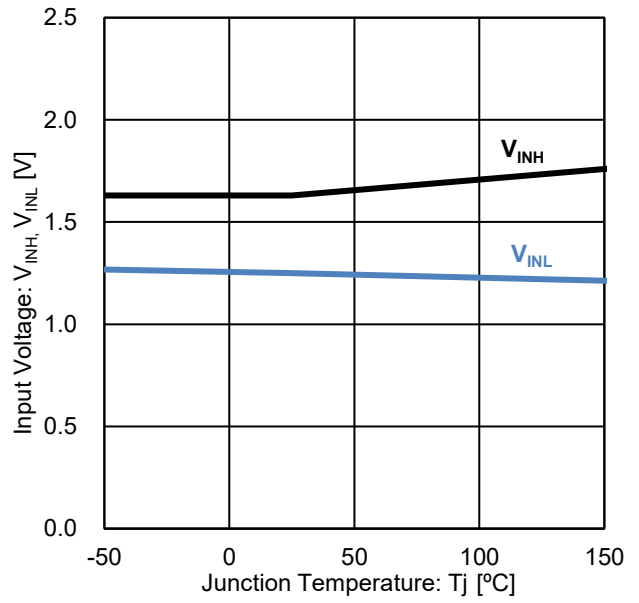


Figure 12. Input Voltage vs Junction Temperature

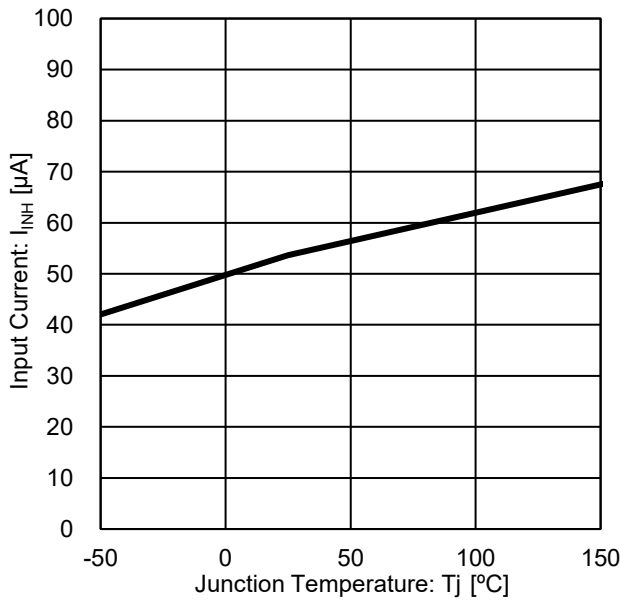


Figure 13. Input Current vs Junction Temperature

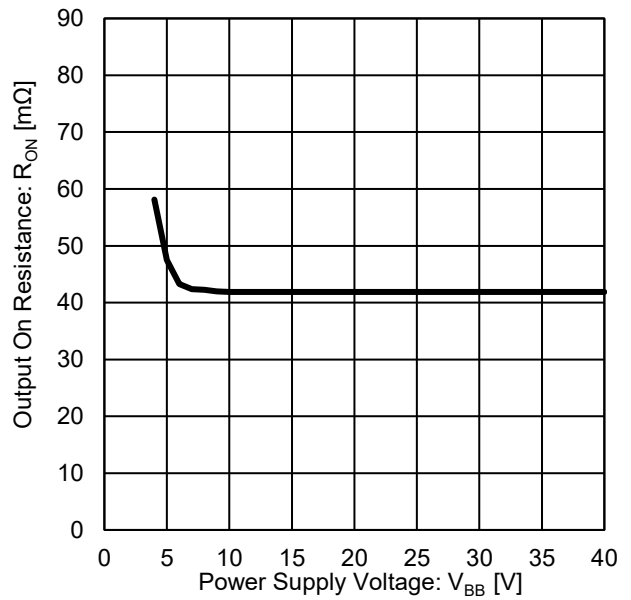


Figure 14. Output ON Resistance vs Supply Voltage

Typical Performance Curves - continued

(Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $I_N = 5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

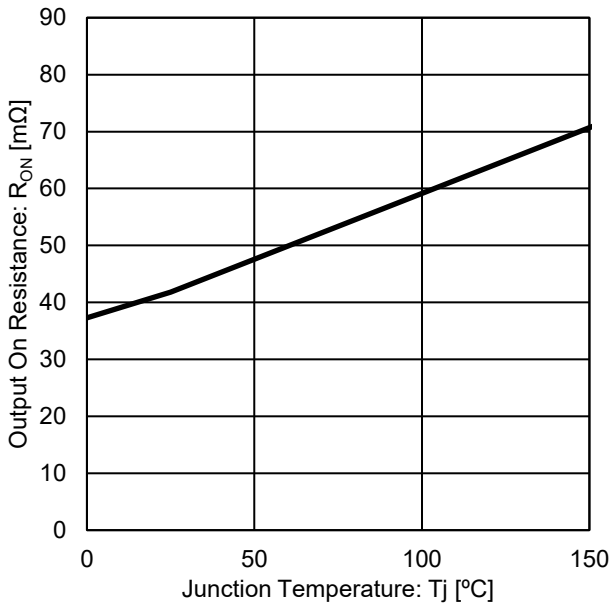


Figure 15. Output ON Resistance vs Junction Temperature

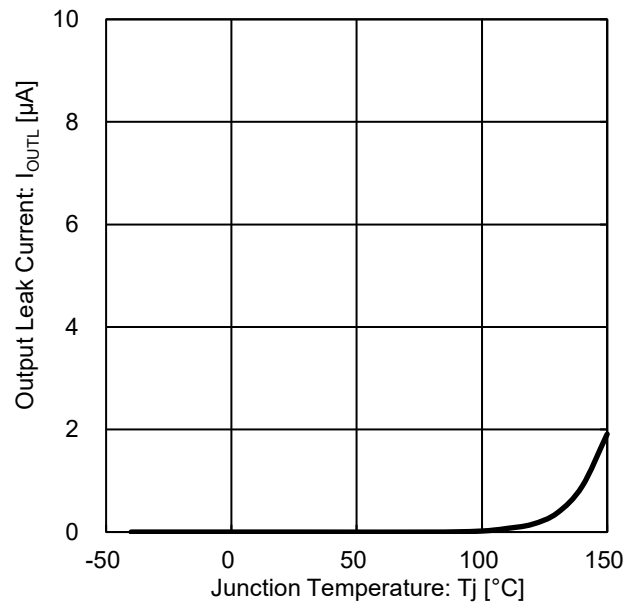


Figure 16. Output leak Current vs Junction Temperature

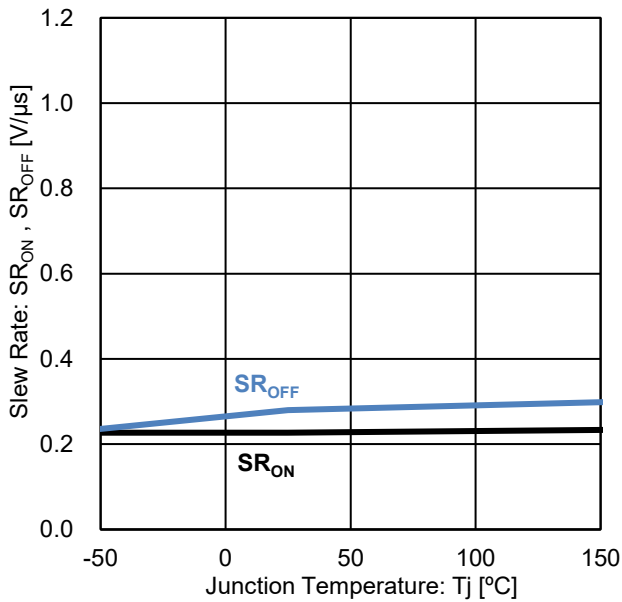


Figure 17. Output Slew Rate vs Junction Temperature

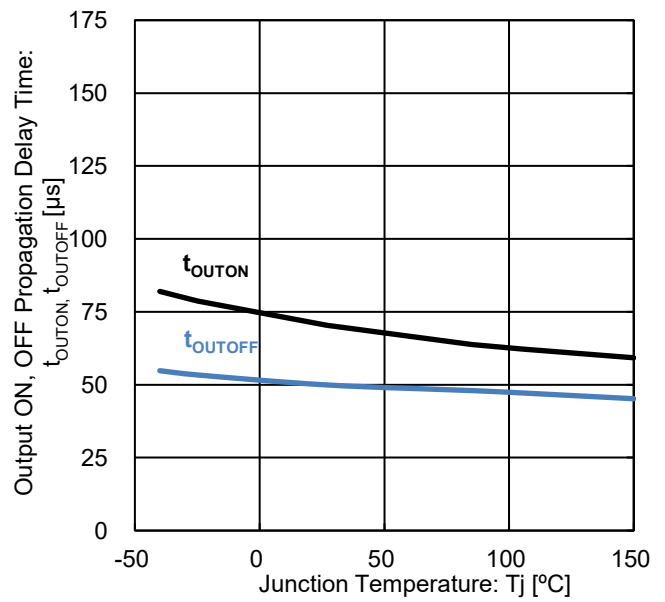


Figure 18. Output ON, OFF Propagation Delay Time vs Junction Temperature

Typical Performance Curves - continued

(Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $I_N = 5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

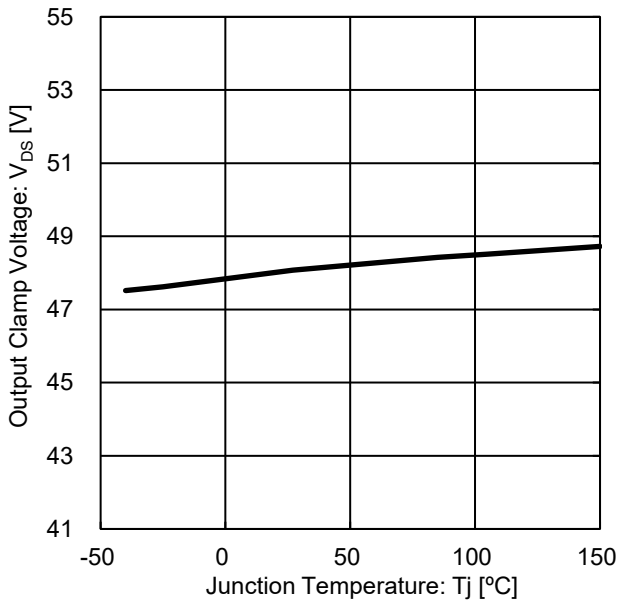


Figure 19. Output Clamp Voltage vs Junction Temperature

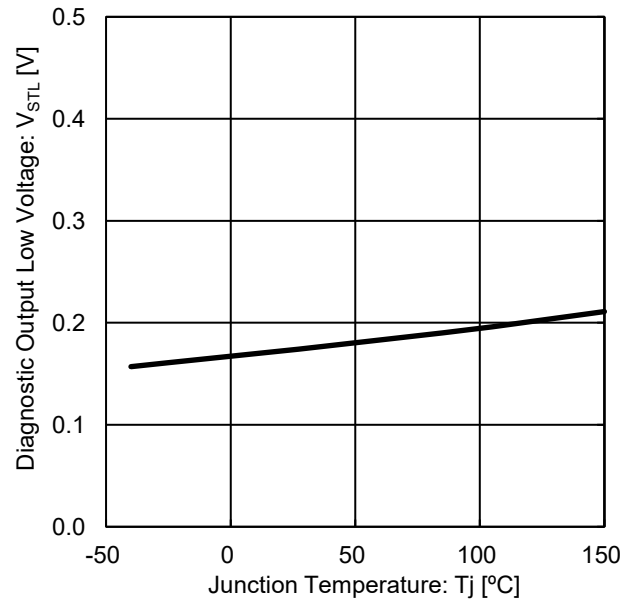


Figure 20. Diagnostic Output Low Voltage vs Junction Temperature

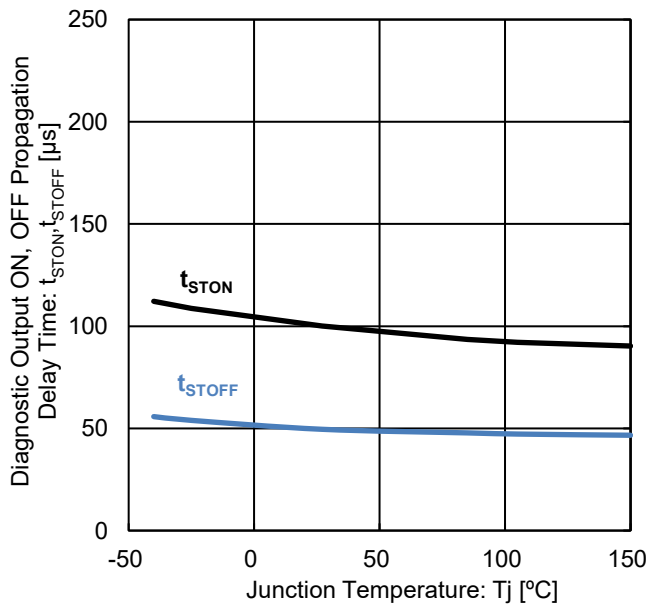


Figure 21. Diagnostic Output ON, OFF Propagation Delay Time vs Junction Temperature

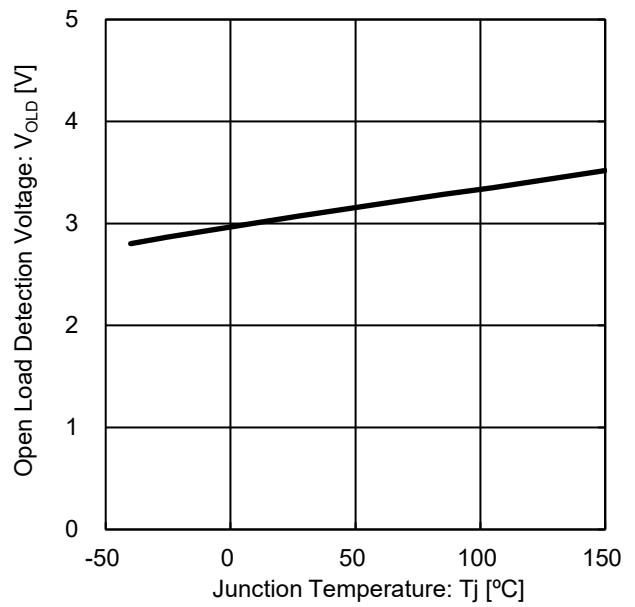


Figure 22. Open Load Detection Voltage vs Junction Temperature

Typical Performance Curves - continued

(Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $I_N = 5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

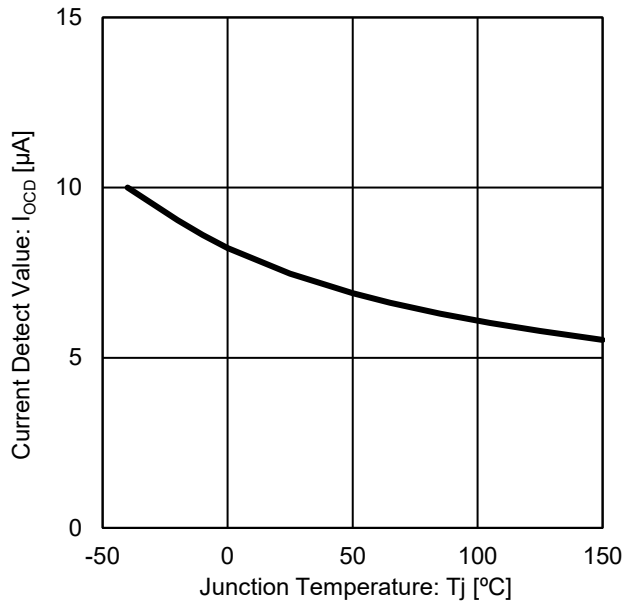


Figure 23. Current Detect Value vs Junction Temperature

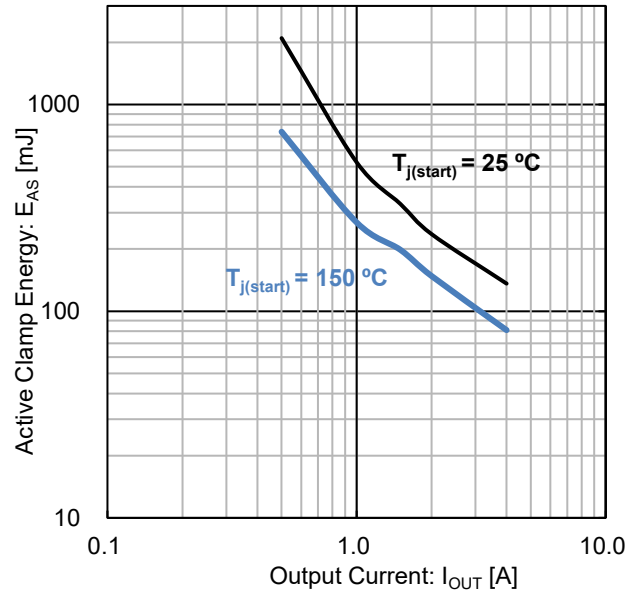


Figure 24. Active Clamp Energy vs Output Current

Measurement Circuit

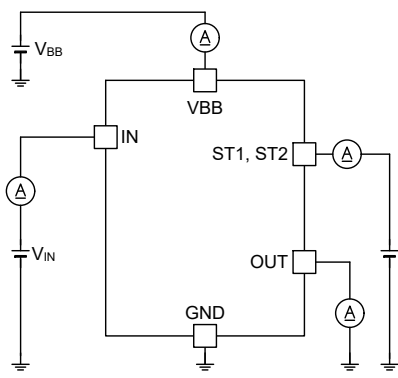


Figure 25. Standby Current  
 Low-Level Input Current  
 Output Leak Current  
 Diagnostic Output Leak Current

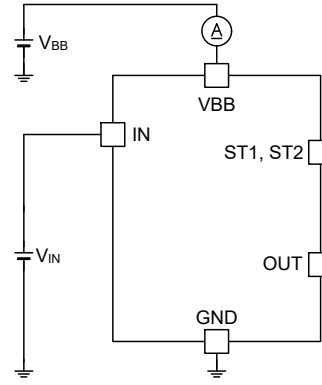


Figure 26. Operating Current

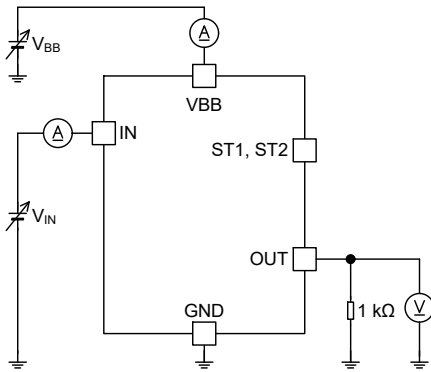


Figure 27. UVLO Detection Voltage  
 UVLO Hysteresis Voltage  
 High Level Input Voltage  
 Low Level Input Voltage  
 Input Hysteresis Voltage  
 High Level Input Current  
 Thermal Shutdown  
 Thermal Shutdown Hysteresis

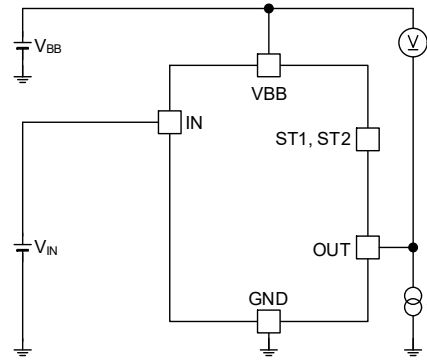


Figure 28. Output ON Resistance  
 Output Clamp Voltage



Measurement Circuit - continued

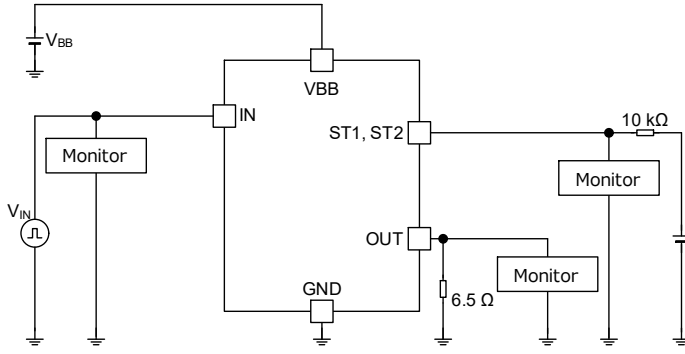


Figure 29. Output ON Slew Rate  
 Output OFF Slew Rate  
 Output ON Propagation Delay Time  
 Output OFF Propagation Delay Time  
 Diagnostic Output ON Propagation Delay Time  
 Diagnostic Output OFF Propagation Delay Time

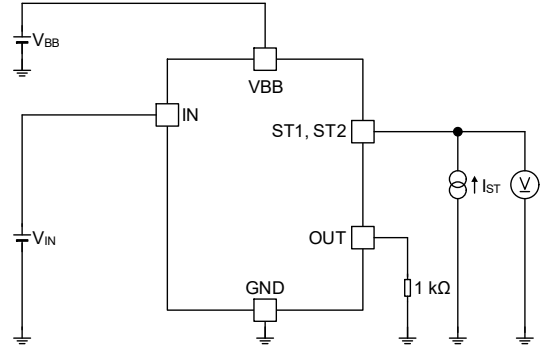


Figure 30. Diagnostic Output Low Voltage

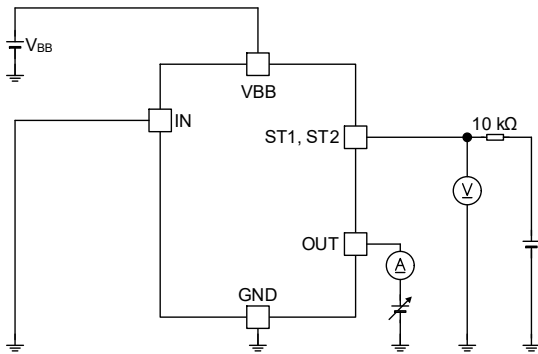


Figure 31. Open Load Detection Voltage  
 Open Load Detection Sink Current

Switching Time Measurement Condition

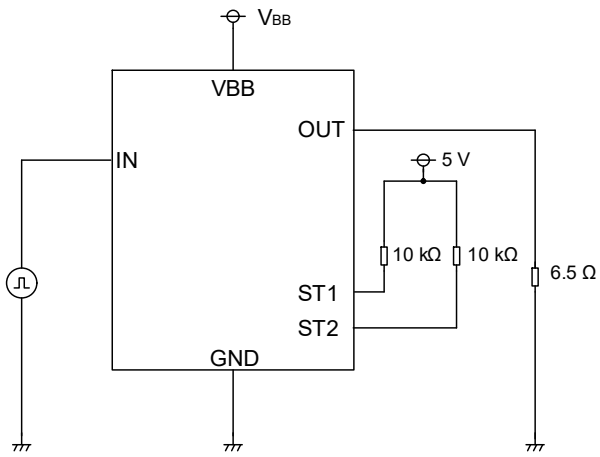


Figure 32. Switching Time Measurement Diagram

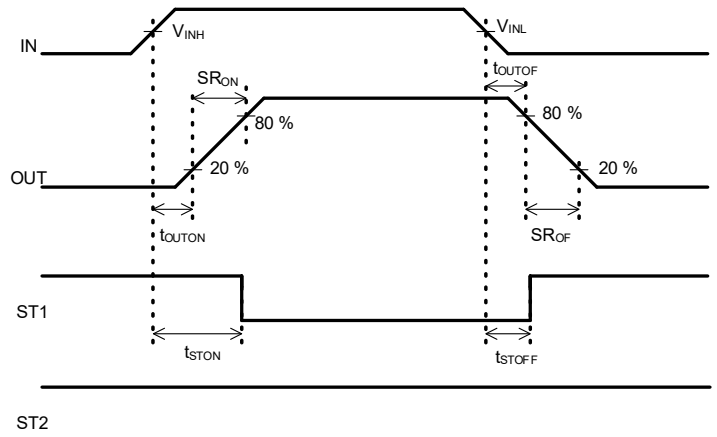


Figure 33. Switching Time Measurement Waveform

Timing Chart

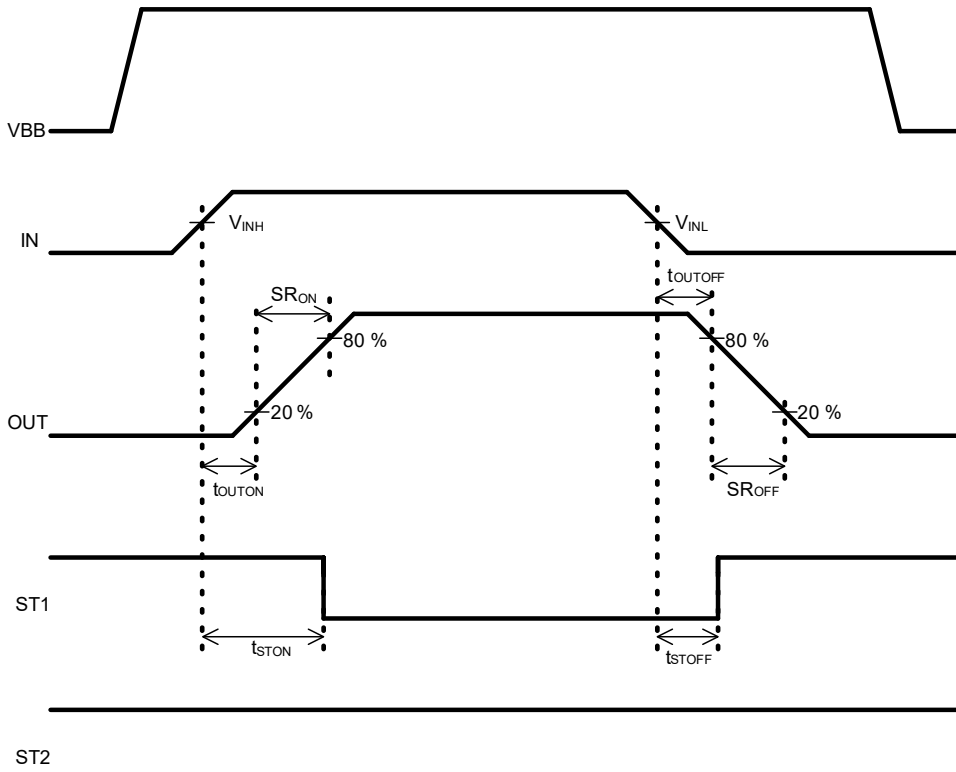


Figure 34. Timing Chart

## Function Description

## 1. Protection Function

Table 1. Detection and Release Conditions of Each Protection Function and Diagnostic Output

Mode		Conditions	IN	ST1	ST2
Normal Condition	Standby	-	Low	High	High
	Operating	-	High	Low	High
Open Load Detect (OLD)		Detect $V_{OUT} \geq 3.0 \text{ V (Typ)}$	Low	Low	High
		Release $V_{OUT} \leq 2.4 \text{ V (Typ)}$	Low	High	High
Short to VBB Detection		Detect $V_{OUT} > V_{BB} - 1.2 \text{ V (Typ)}$	Low	Low	Low
		Release $V_{OUT} < V_{BB} - 2.0 \text{ V (Typ)}$	Low	Low	High
Low Voltage Output OFF (UVLO)		Detect $V_{BB} \leq 5.0 \text{ V (Max)}$	High	High	High
		Release $V_{BB} \geq 6.0 \text{ V (Max)}$	High	Low	High
Thermal Shutdown (TSD) <i>(Note 1)</i>		Detect $T_j \geq 175 \text{ }^\circ\text{C (Typ)}$	High	High	High
		Release $T_j \leq 160 \text{ }^\circ\text{C (Typ)}$	High	Low	High
$\Delta T_j$ Protection <i>(Note 2)</i>		Detect $\Delta T_j \geq 120 \text{ }^\circ\text{C (Typ)}$	High	High	High
		Release $\Delta T_j \leq 80 \text{ }^\circ\text{C (Typ)}$	High	Low	High
Over Current Protection (OCP)		Detect $I_{OUT} \geq 4.0 \text{ A (Typ)}$	High	High	High
		Release $I_{OUT} < 4.0 \text{ A (Typ)}$	High	Low	High

*(Note 1)* Thermal shutdown is automatically restored to normal operation.

*(Note 2)* Protect function by detecting PowerMOS sharp increase of temperature difference with control circuit.

This IC has a built-in protection detection function as mentioned above and outputs the abnormal condition with ST1 and ST2 pins.

ST1 is output for output detect and each protect function.

ST1 change from High to Low when OUT rise by near VBB during normal operation.

And change from Low to High when detect each protection or OUT is less than  $V_{BB} - 1.2 \text{ V (Typ)}$ .

ST2 is output for open load detection and Short to VBB detection during IN = Low.

It is self-rest and operation becomes normal when each protection releases after detecting.

Function Description - continued

2. Overcurrent Protection

This IC has a built-in overcurrent protection function. When overcurrent flows in the output, the output current is limited to 4.0 A (Typ) and self-diagnostic output 1 (ST1) becomes High.

3. Thermal Shutdown and  $\Delta T_j$  Protection Detection

3.1 Thermal Shutdown Protection

This IC has a built-in thermal shutdown protection function. When the IC chip temperature exceeds 175 °C (Typ), the output is turned OFF and self-diagnostic output 1 (ST1) becomes High. When the temperature goes below 160 °C (Typ), output will self-reset and operation becomes normal.

3.2  $\Delta T_j$  Protection

This IC has a built-in  $\Delta T_j$  protection function that turns OFF the output when the temperature difference ( $T_{\Delta T_j}$ ) between the POWER-MOS unit ( $T_{POWER-MOS}$ ) and the control unit ( $T_{AMB}$ ) in the IC is 120 °C (Typ) or more.  $\Delta T_j$  protection also has a built-in hysteresis ( $T_{\Delta T_j HYS}$ ) that returns the output to normal state when the temperature difference becomes 80 °C (Typ) or less.

Figure 35 shows the timing chart of thermal shutdown protection and  $\Delta T_j$  protection during output short to GND fault.

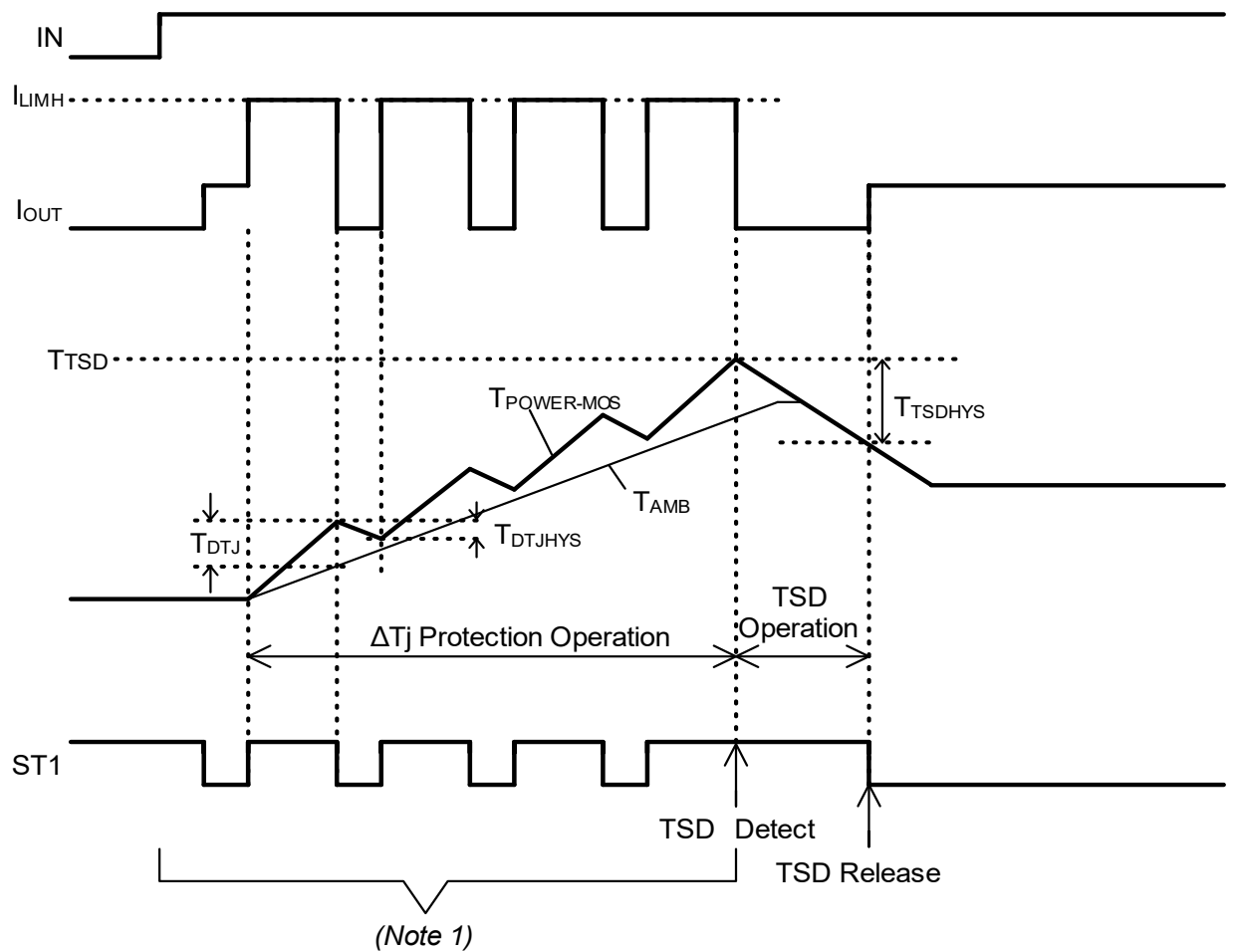


Figure 35. Thermal Shutdown Protection and  $\Delta T_j$  Protection Timing Chart

(Note 1) When output voltage falls to output ON detection voltage ( $V_{SHV}$ ) or less at the output to GND is shorted or rare short, IC is judged that the output voltage is abnormal. Hence, ST1, ST2 may not be able to turn low.

Function Description - continued

4. Open Load Detection

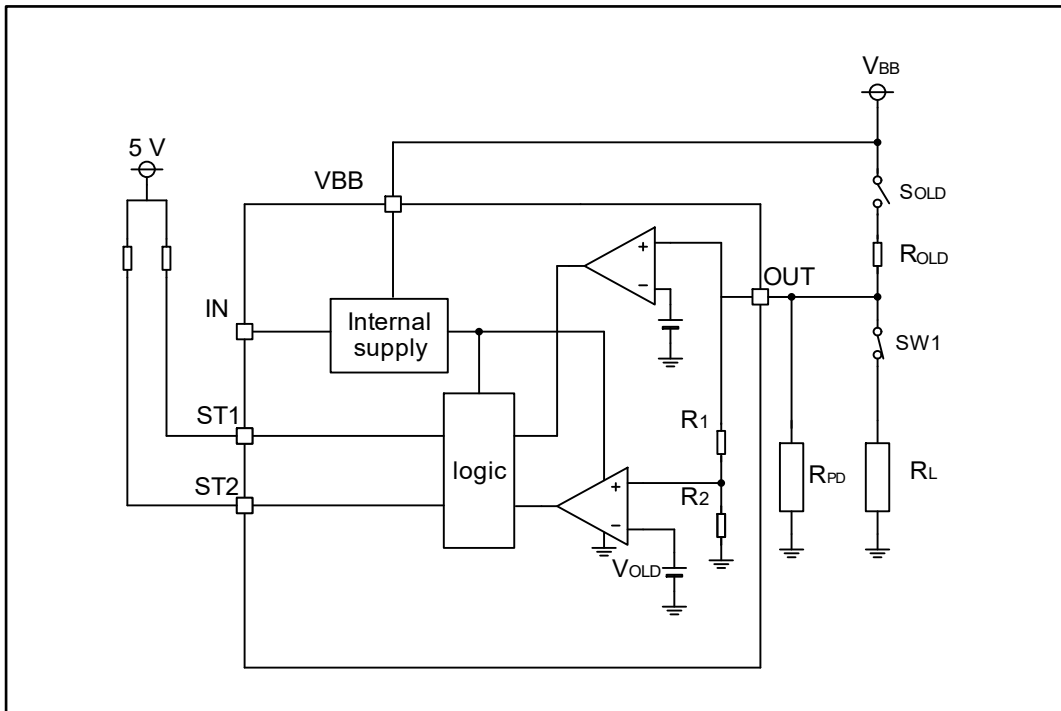


Figure 36. Open Load Detection Block Diagram

Open load can be detected by connecting an external resistance  $R_{OLD}$  between power supply  $V_{BB}$  and output. When output load is disconnected during input is low, diagnostic output the ST1 pin is turned to low to indicate abnormality. To reduce the standby current of the system, an open load resistance switch  $S_{OLD}$  is recommended. When the SW1 is OFF, voltage of the OUT does not fall to GND level. Because, when the IN pin is low, the voltage of the OUT pin does not become under or equal to the Output ON Detection Voltage ( $V_{DSDET}$ ). To pulled down the OUT pin, pulled down resistance  $R_{PD}$  is recommended. The resistance  $R_{PD}$  is 4.3 k $\Omega$  or less for outflow current from the OUT pin.

4.1 When the OUT is pulled down by the load (Normal function)

The value of external resistance  $R_{OLD}$  is decided based on used minimum power supply voltage ( $V_{BB}$ ), internal resistance  $R_1$  and  $R_2$  and open detection voltage  $V_{OLD}$ . External resistance  $R_{PD}$  is unnecessary. The equation for calculating the  $R_{OLD}$  value is shown below.

$$R_{OLD} < \frac{V_{BB} \times (R_{1(Min)} + R_{2(Min)})}{V_{OLD(Max)}} - (R_{1(Min)} + R_{2(Min)}) \text{ } [\Omega]$$

The above formula is summarized as follows.

$$R_{OLD} < V_{BB} \times 75 \times 10^3 - 300 \times 10^3 \text{ } [\Omega]$$

$R_{OLD}$  value is fell below the above calculated result.

4.2 If the SW is OFF, the output is no longer pulled down by the load

The value of external resistance  $R_{OLD}$  is decided based on used minimum power supply voltage ( $V_{BB}$ ), external resistance  $R_{PD}$  and open detection voltage  $V_{OLD}$ . The equation for calculating the  $R_{OLD}$  value is shown below.

$$R_{OLD} < \frac{V_{BB} \times R_{PD}}{V_{OLD(Max)}} - R_{PD} \text{ } [\Omega]$$

When  $R_{PD}$  is 4.3 k $\Omega$ , the above formula is summarized as follows.

$$R_{OLD} < V_{BB} \times 1.075 \times 10^3 - 4.3 \times 10^3 \text{ } [\Omega]$$

$R_{OLD}$  value is fell below the above calculated result

Function Description - continued

5. Other Detection

5.1 GND open protection

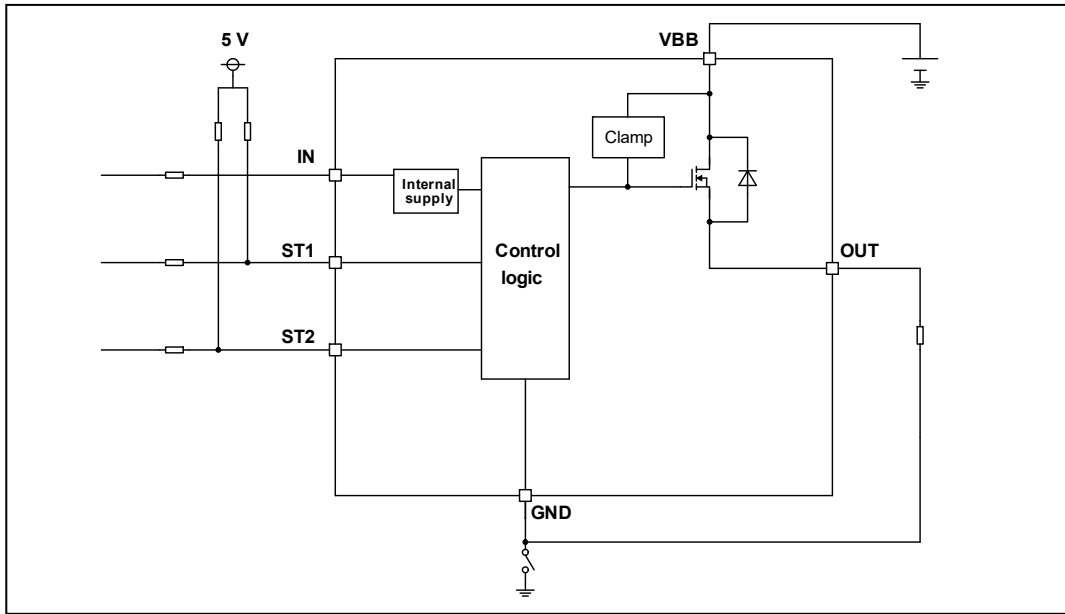


Figure 37. GND Open Detection Block Diagram

When GND of the IC is open, the output is switched OFF regardless of the input voltage. However, self-diagnostic output (ST1, ST2) is not flagged. When an inductive load is connected, the active clamp operates when the GND pin is open

5.2 Reverse-Battery Connection Protection

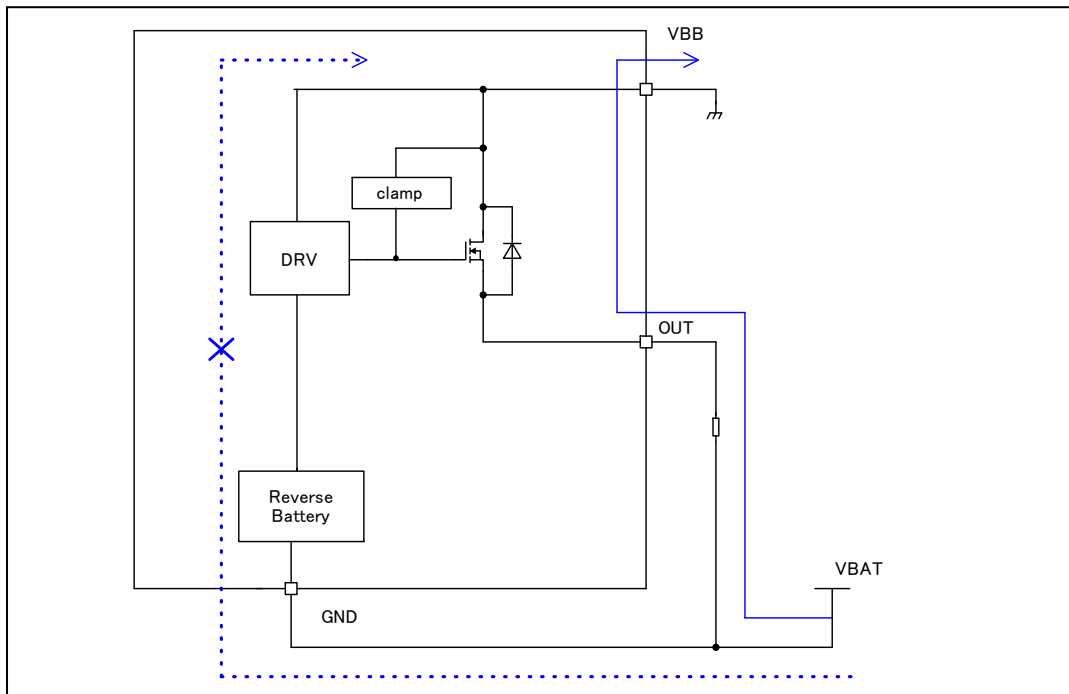


Figure 38. Reverse-Battery Connection Block Diagram

When the battery connection is reversed, an excessive amount of current will flow to internal part of IC and this may sometimes lead to IC destruction. As a countermeasure, this IC has a built-in reverse battery connection protection function without external components such as resistors and diodes.

Function Description - continued  
 5.3 MCU I/O Protection

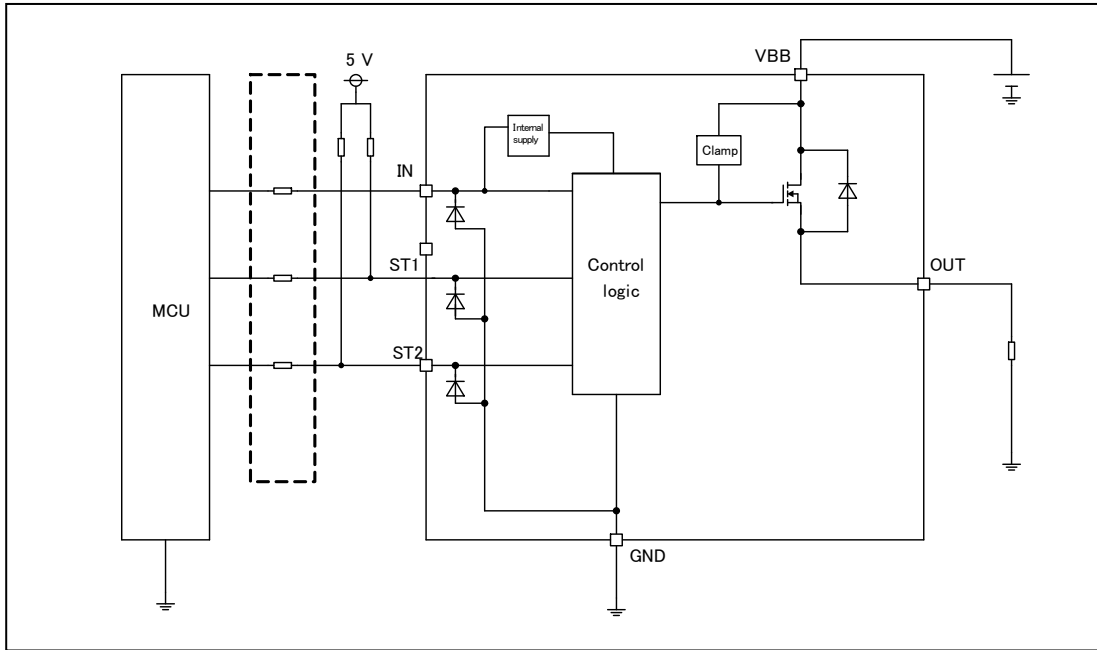


Figure 39. MCU I/O Protection

Negative surge voltage to the IN pin, the ST1 pin and the ST2 pin may cause damage to the MCU's I/O pins. In order to prevent those damages, it is recommended to insert limiting resistors between IC pins and MCU.



Application Circuit Diagram

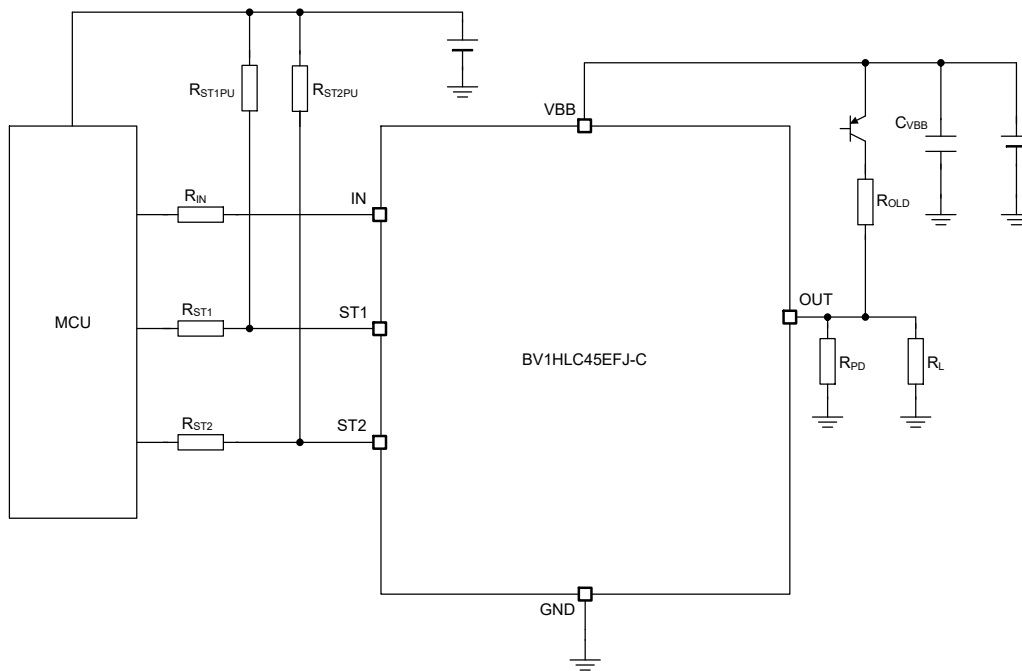
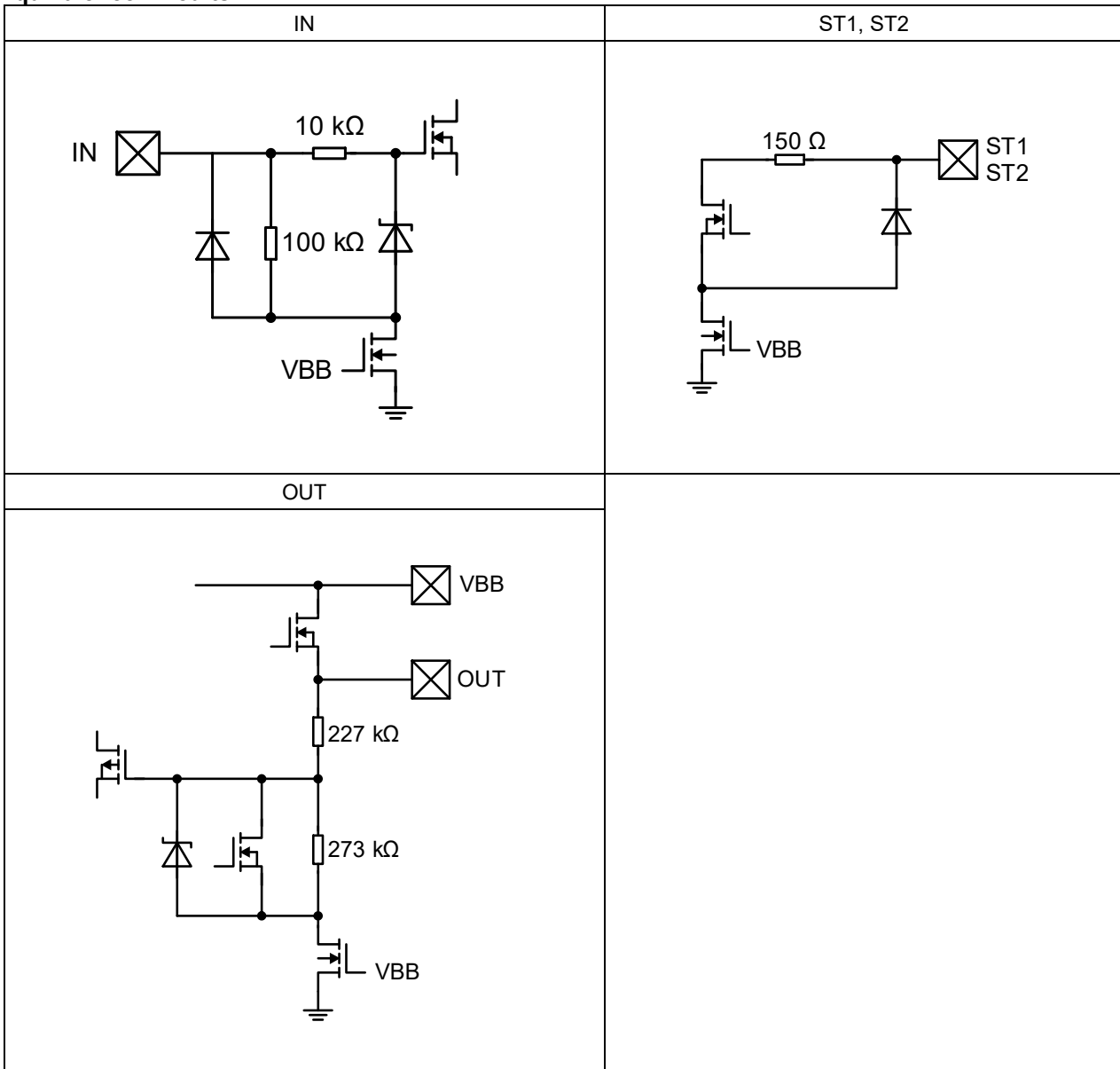


Figure 40. Application Circuit Diagram

Symbol	Value	Purpose
$R_{IN}$	4.7 k $\Omega$	Limit resistance for negative surge
$R_{ST1}, R_{ST2}$	4.7 k $\Omega$	Limit resistance for negative surge
$R_{ST1PU}, R_{ST2PU}$	10 k $\Omega$	Pull up ST1/ST2 pin to MCU power supply, these pins are open drain output
$C_{VBB}$	1 $\mu$ F	For battery line voltage spike filter
$R_{PD}$	4.3 k $\Omega$	For output pulled down
$R_{OLD}$	2 k $\Omega$	For open load detection

I/O Equivalence Circuits



Resistance values shown in the diagrams above are typical values.

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

### 10. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

### 11. Thermal Shutdown Function (TSD)

This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD function that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

**Operational Notes – continued****12. Over Current Protection Function (OCP)**

This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

**13. Active Clamp Operation**

The IC integrates the active clamp function to internally absorb the reverse energy  $E_L$  which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy  $E_L$  is active clamp tolerance  $E_{AS}$  (refer to Figure 24. Active Clamp Energy vs Output Current) or under when inductive load is used.

**14. Open Power Supply Pin**

When the power supply pin (VBB) becomes open at ON (IN = High), the output is switched to OFF regardless of input voltage. If an inductive load is connected, the active clamp operates when VBB is open and becomes the same potential as that on the ground. At this time, the output voltage drops down to -48 V (Typ).

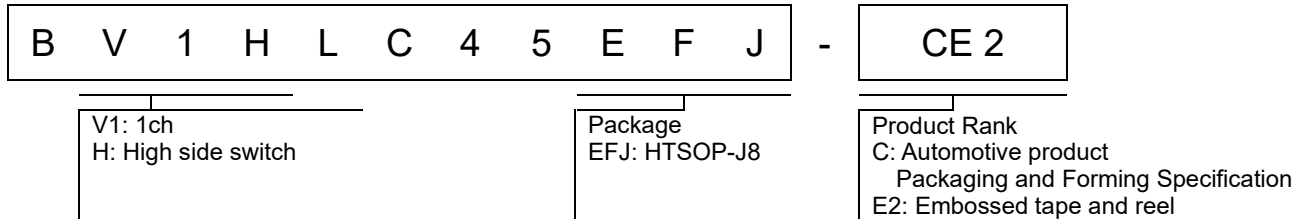
**15. Open GND Pin**

When the GND pin becomes open at ON (IN = High), the output is switched to OFF regardless of input voltage. If an inductive load is connected, the active clamp operates when the GND pin is open.

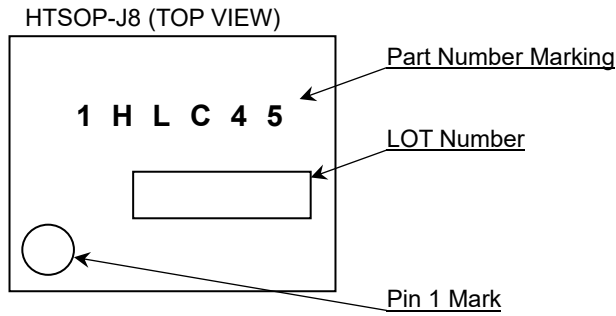
**16. OUT Pin Voltage**

Ensure that keep OUT pin voltage less than (VBB + 0.3 V) at any time, even during transient condition. Otherwise malfunction or other problems can occur.

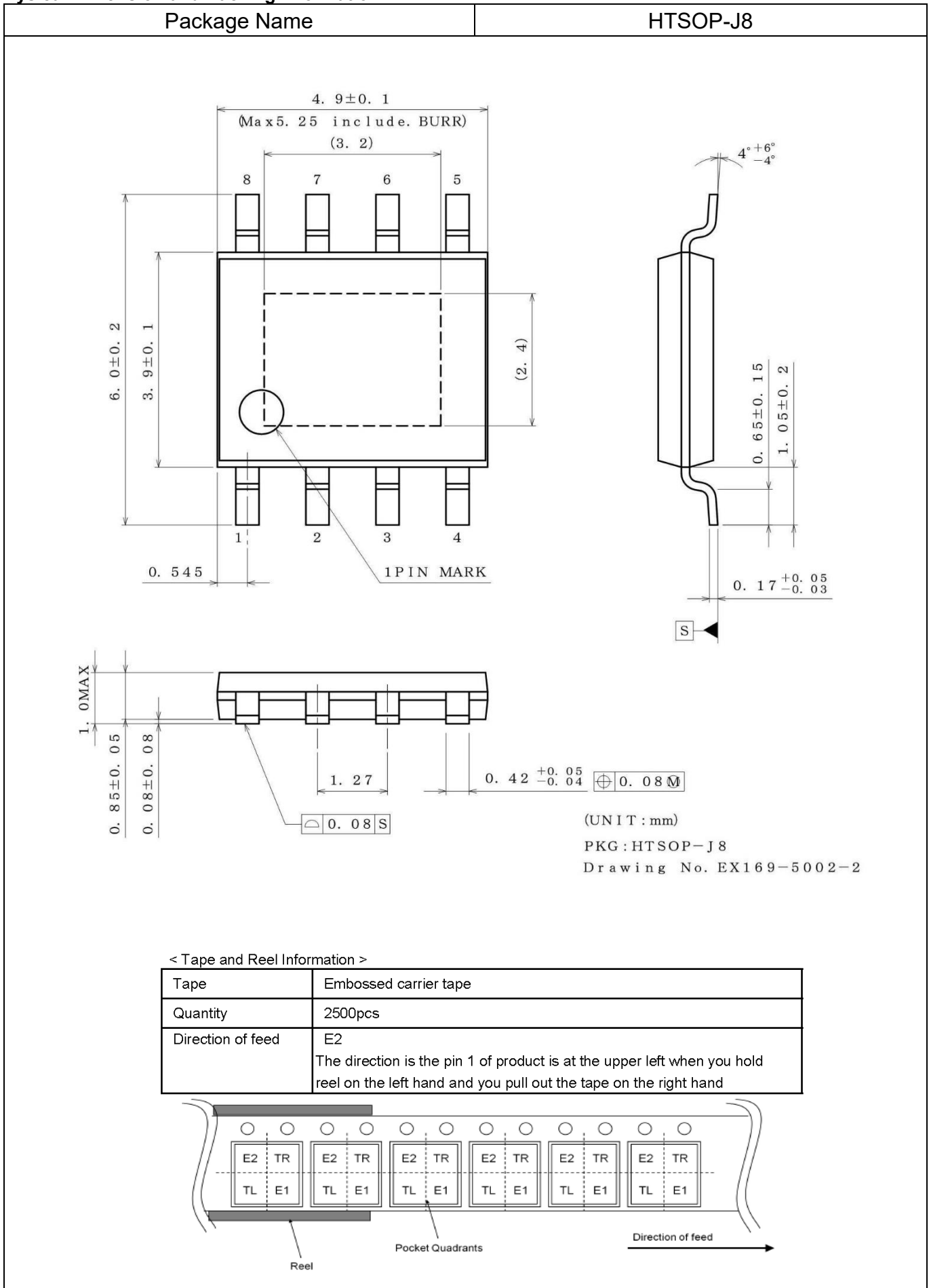
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



**Revision History**

Date	Revision	Changes
03.Sep.2021	001	New Release

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8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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