Matrix LED Driver

Automotive Dynamic Indicator Lamps 8ch Matrix LED Controller

BD18362EFV-M

General Description

BD18362EFV-M is an 8-channel matrix LED controller with an internal FET switch. Switching the FET on and off allows a control of the sequential lighting.
An internal charge pump serves as a power supply for the gate driver. Since sequential lighting pattern is built in, the microcontroller is unnecessary.

Key Specifications

- Input Voltage Range: 5.5V to 60V
- Maximum Total LED's Voltage: 48V(Max)
- Maximum SW Bypass Current 1.0A(Max)
- Internal FET Switch ON Resistance: 230mΩ(Typ)
- Operating Temperature Range: -40°C to +125°C

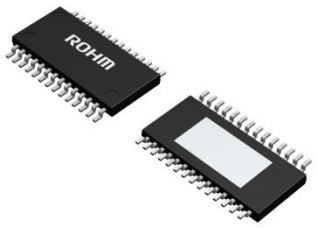
Features

- AEC-Q100 Qualified*(Note 1)*
- 8-channel Matrix Switch
- Up to 2LED's per Switch Control
- Built in Sequential Lighting pattern
- Sequential Lighting Phase Time Setting
- Sequential Lighting Start-up Delay Time Setting
- All-light-up (Hazard Mode)
- LED Open Protection
- LED Short Detection
- Thermal shutdown

(Note 1) Grade1

Package

	W(Typ) x D(Typ) x H(Max)
HTSSOP-B28	9.70mm x 6.40mm x 1.00mm

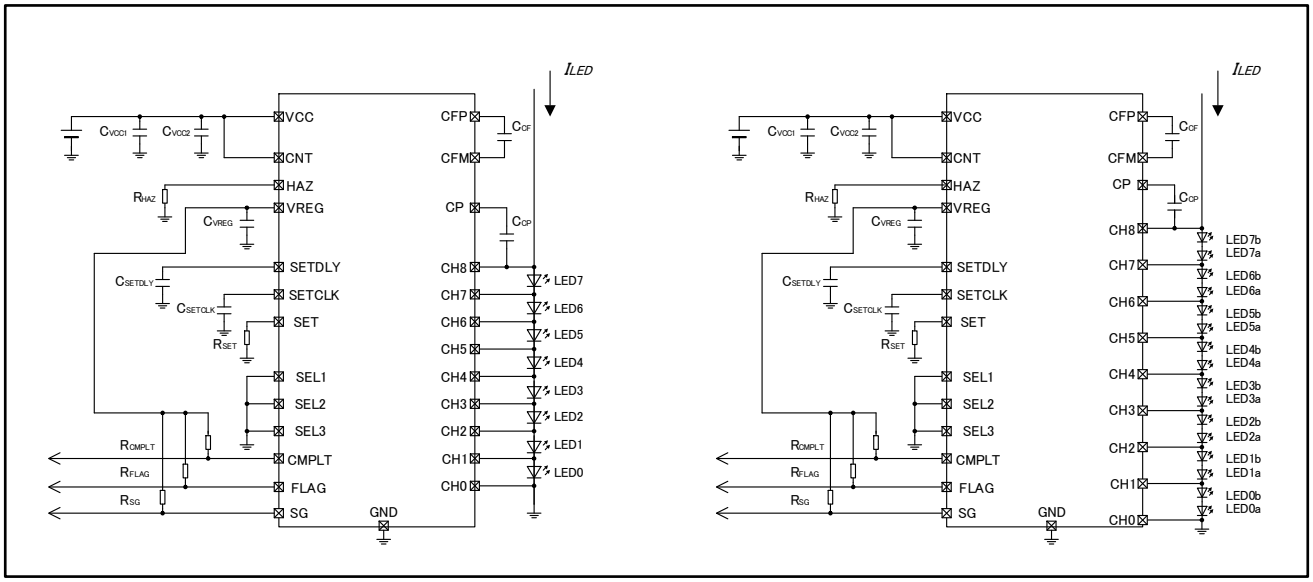


HTSSOP-B28

Applications

- Automotive Exterior Lamps (Dynamic Indicator)

Typical Application Circuit



○Product structure: Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

General Precaution

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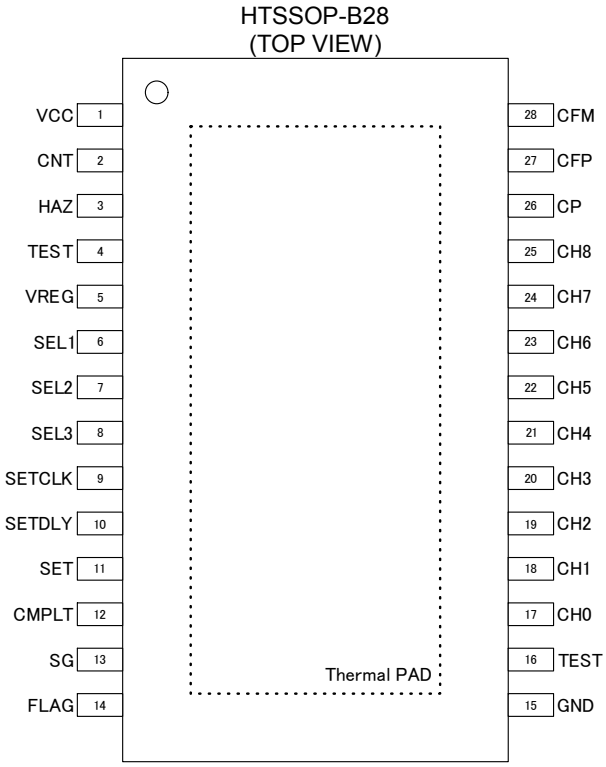
Pin Configuration

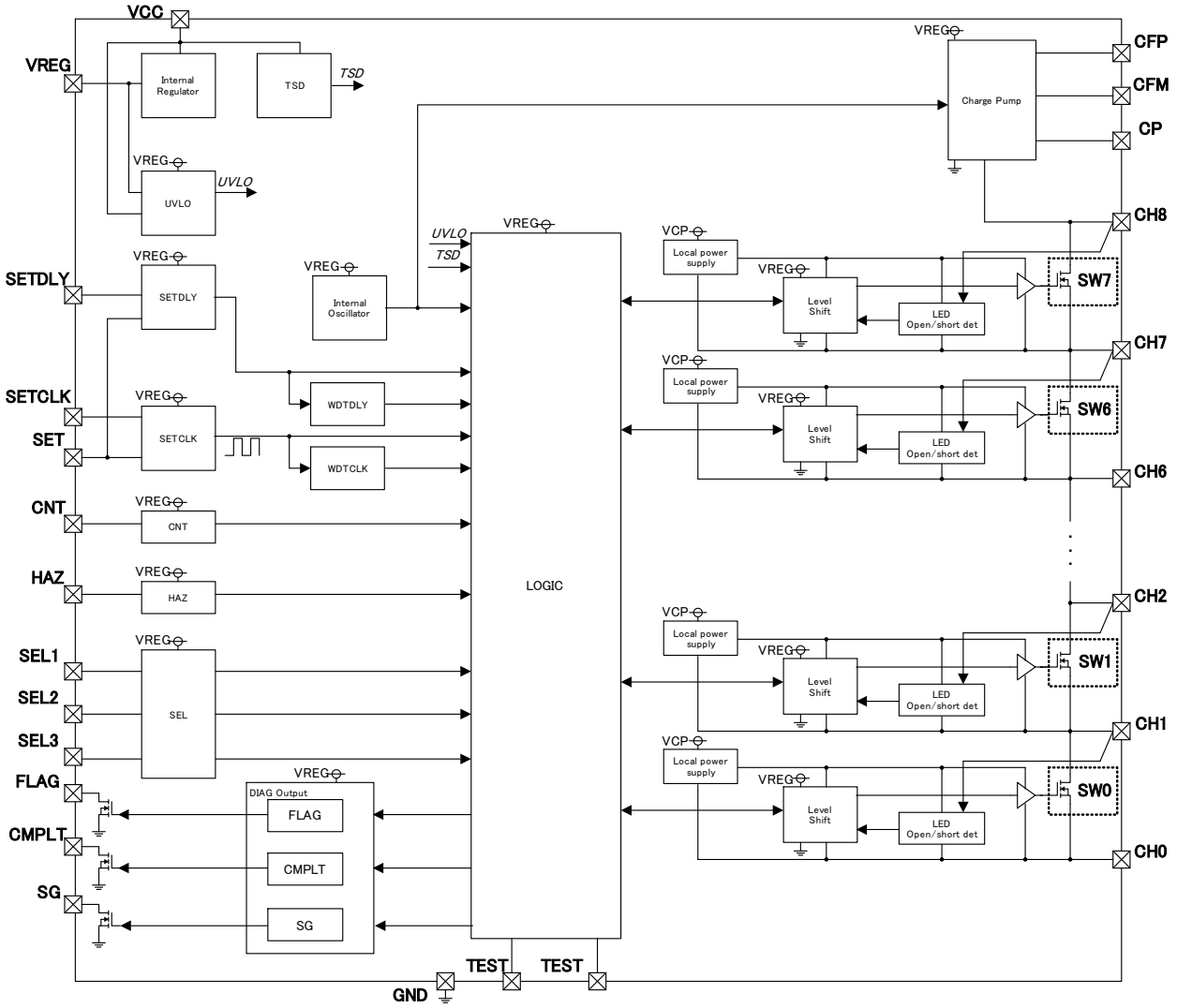


Pin Description

PIN No.	Symbol	Function	PIN No.	Symbol	Function
1	VCC	Input power supply	15	GND	GND
2	CNT	Control input	16	TEST	TEST input (Note 1)
3	HAZ	Hazard mode switching input	17	CH0	LED0 cathode connection
4	TEST	TEST input (Note 1)	18	CH1	LED0 anode & LED1 cathode connection
5	VREG	Internal reference voltage output	19	CH2	LED1 anode & LED2 cathode connection
6	SEL1	Setting of the switch in use 1	20	CH3	LED2 anode & LED3 cathode connection
7	SEL2	Setting of the switch in use 2	21	CH4	LED3 anode & LED4 cathode connection
8	SEL3	Setting of the switch in use 3	22	CH5	LED4 anode & LED5 cathode connection
9	SETCLK	Sequential lighting phase time setting	23	CH6	LED5 anode & LED6 cathode connection
10	SETDLY	Sequential lighting start-up delay time setting	24	CH7	LED6 anode & LED7 cathode connection
11	SET	Sequential lighting phase time/ start-up delay time setting	25	CH8	LED7 anode connection
12	CMPLT	Lighting complete signal output	26	CP	Charge pump output for internal switch
13	SG	Status good output	27	CFP	Connecting capacitor for charge pump +
14	FLAG	Error flag output	28	CFM	Connecting capacitor for charge pump -

(Note 1) Connect to GND

Block Diagram



Description of Blocks

1. Total Function

The BD18362EFV-M is a matrix LED controller able to implement a sequential lighting (Dynamic Indicator) of LEDs without the need for a microcontroller.
An LSI meant for driving LEDs with eight switches connected in a series and is used in conjunction with an LED driver. The switches are connected to the anodes and cathodes of the LED. When the switch is OFF, a current flow through the LED and the LED is light. When the switch is ON, the current is bypassed and the LED is unlighted.
When the CNT pin is given a high input, the switches are turned OFF sequentially from SW0 after the sequential lighting start-up delay time (t_{DLY}) and the LEDs are lighting sequentially from LED0.
The t_{DLY} can be set by means of a capacitor connected to the SETDLY pin and a resistor connected to the SET pin.
The sequential lighting phase time (t_{PS1}), in which the switch is turned from the ON to the OFF position, can be set by means of a capacitor connected to the SETCLK pin and a resistor connected to the SET pin.
When the CNT pin is given a low input, the LEDs are turned to the all-OFF position. However, the switches are turned ON sequentially from SW7 (LEDs are unlighted sequentially) at a fixed time (t_{PSL}). This avoids sudden output voltage fluctuations.
Additionally, the BD18362EFV-M is built in hazard mode function. When the HAZ pin is given a high input at the lighting condition, the LEDs are turned from the all-OFF to the all-ON position. However, the switches are turned OFF sequentially from SW0 (LEDs are light sequentially) at a fixed time (t_{PSH}). This avoids sudden output voltage fluctuations.

Although there are 8 switches to the BD18362EFV-M, it is also possible to use it with 7 switches or less. The number of used switches can be set by pulling up the SEL1 pin, the SEL2 pin and the SEL3 pin to the VREG pin or by pulling down to GND.
Also, it is possible to use two BD18362EFV-M if more than 9 switches are employed. A sequential lighting of more than 9 switches is possible by connecting the CMPLT pin and the CNT pin so the phase shift of the second BD18362EFV-M will start after the phase shift of the first BD18362EFV-M has been completed.

The BD18362EFV-M is built in a diagnostic function for LED open and LED short on each switch. If the LED open diagnosis detects an open during the period when the LED is light (the switch is OFF), the immediately corresponding switch is turned ON and the current is bypassed. Additionally, the FLAG pin will have a low output in order to report the LED open. In the same way, the LED short diagnosis detects a short during the period when the LED is light (the switch is OFF). The FLAG pin will have a low output in order to report the LED short.

BD18362EFV-M built in an internal watchdog timer.
●Watchdog timer for sequential lighting start-up delay time
If the capacitor connected to the SETDLY pin has a short, the LED will be unlighted, since the sequential lighting start-up delay time cannot be set. When t_{WDTDLY} has passed, there is a time-out and the FLAG pin will have a low output. Also, the LEDs are automatically all light. As in the hazard mode, the switches are turned OFF sequentially at fixed time.
●Watchdog timer for sequential lighting phase time
If the capacitor connected to the SETCLK pin has a short, the LED will be unlighted, since the phase shift time t_{PS1} cannot be set. When t_{WDTCLK} has passed, there is a time-out and the FLAG pin will have a low output. Also, the LEDs are automatically all light. As in the hazard mode, the switches are turned OFF sequentially at fixed time.

The BD18362EFV-M is built in charge pump serving as a power supply for the switch gate drive. All switches and gate drive circuits form a floating circuit and operate under the voltage generated by the charge pump circuit.

The BD18362EFV-M has high voltage switches and each of switches can connect with up to 2 LEDs in series. Achieve the 16 LEDs solution by 8-channels with 2LEDs in each of switches.

Description of Blocks – continued

2. SG [Status Good]

After the VCC is supplied, the switches may happen to be OFF until the internal circuit comes to a stable condition. In this condition, the LED might flicker when the LED current is supplied.
The BD18362EFV-M can report by the SG pin for internal condition as ready to switch in stable. In order to prevent a flickering, it is recommended to provide an LED current after the SG pin switches from a low to Hiz.
If the VCC pin voltage rises above the UVLO release voltage (V_{UVR}) and the SG delay time (t_{dSG}) has passed, the SG pin will switch from a low to Hiz.
During UVLO detection or thermal shutdown detection, the SG pin will switch to a low. If the SG delay time (t_{dSG}) has passed after a UVLO release and thermal shutdown release, the SG pin will switch from a low to Hiz.
(refer to Figure19 (b))
The SG pin is open drain and needed pulled up resistor for monitoring output signal.

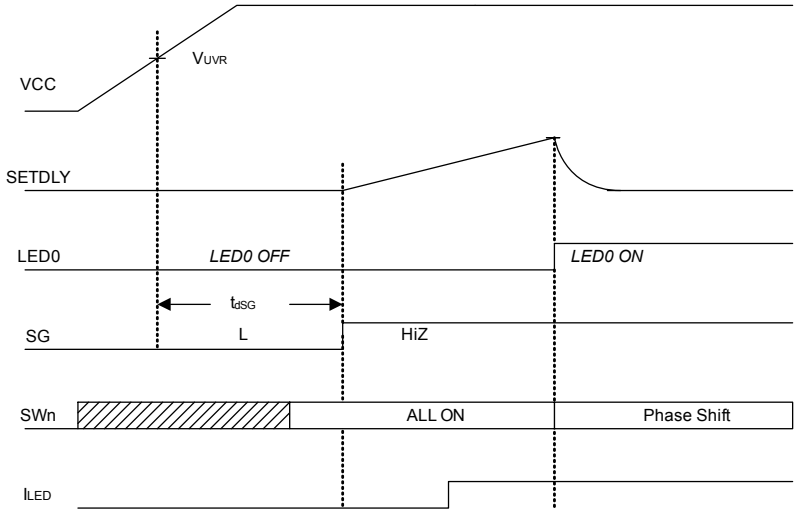


Figure 1. Timing Chart
(Status Good Function)

To avoid the LED flicker, it is recommended to connect the SG pin and the current source LED drivers control pin (e.g. enable pin and PWM pin). Pull up the SG pin to the VREG pin (BD18362EFV-M) with resister, connect the SG pin and the current source LED drivers control pin. Design with sufficient consideration of the threshold voltage input, inside impedance, pull up resister value and VREG voltage value.

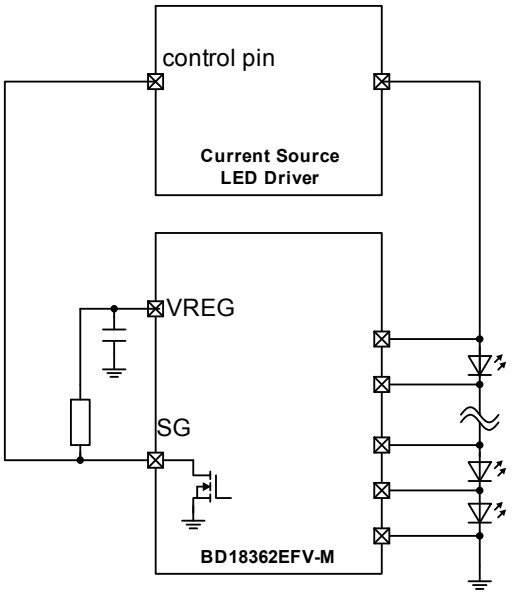


Figure 2. Application of Connecting with the SG Pin to the current source LED Driver

Description of Blocks – continued

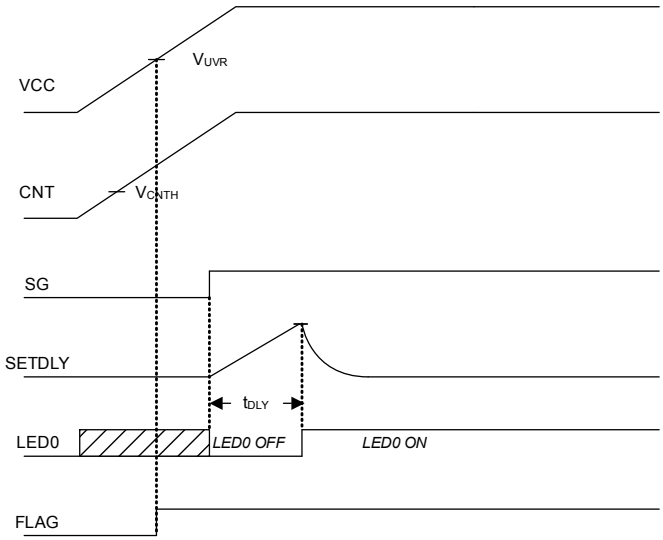
3. SETDLY [Sequential Lighting Start-up Delay Time Setting]

The delay time until the switch is turned OFF must be set in order not to have a planned sequential operation where BD18362EFV-M turns the switches OFF before the current supply to the LED (e.g. LED driver) operates. The setting can be done the capacitor connected to the SETDLY pin (C_{SETDLY}) and the resistor connected to the SET pin (R_{SET}).
The charging of the capacitor connected to the SETDLY pin starts when the SG pin change from low to Hiz and the CNT pin voltage has risen above the V_{CNTH} voltage. SW0 turn OFF (LED0 turn ON) after the setting time (t_{DLY}).

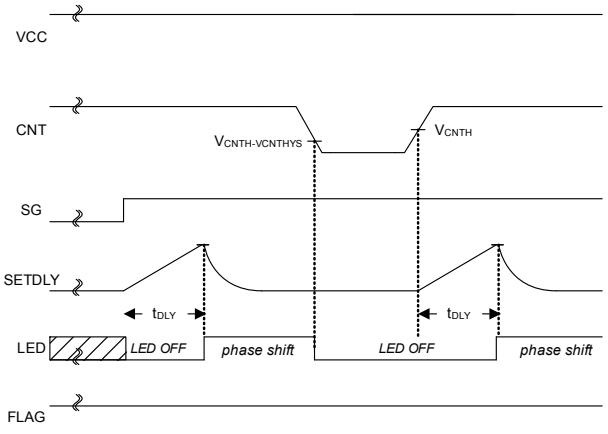
Sequential Lighting Start-up Delay Time

$$t_{DLY} = K_{DLY} \times R_{SET} \times C_{SETDLY} \quad [s]$$

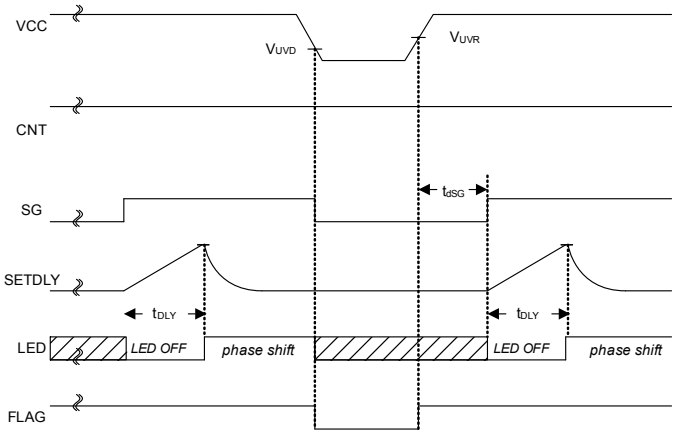
When the Sequential lighting start-up delay time is passed, the SETDLY pin is discharged.
A recharge is possible under the following 3 conditions: (1) or (2) or (3)
(1) UVLO detection → UVLO release → Status good delay time passed → Recharge
(2) Thermal shutdown detection → Thermal shutdown release → Status good delay time passed → Recharge
(3) Input $V_{CNT} \leq V_{CNTH}$-V_{CNTHYS} → Input $V_{CNT} \geq V_{CNTH}$ → Recharge



(a) Start-up



(b) CNT control



(c) Re-start

Figure 3. Timing Chart
(Sequential Lighting Start-up Delay Time)

Description of Blocks – continued

4. SETCLK [Sequential Lighting Phase Time Setting]

Through the BD18362EFV-M it is possible to change the sequential lighting phase time.
The sequential lighting phase time (t_{PS1}) is determined by the clock period (t_{CLK}), which is set by the capacitor connected to the SETCLK pin (C_{SETCLK}) and the resistor connected to the SET pin (R_{SET}).

Clock Period

$$t_{CLK} = \frac{K_{PS} \times R_{SET} \times C_{SETCLK}}{256} \quad [s]$$

Sequential Lighting Phase Time

$$t_{PS1} = K_{PS} \times R_{SET} \times C_{SETCLK} \quad [s]$$

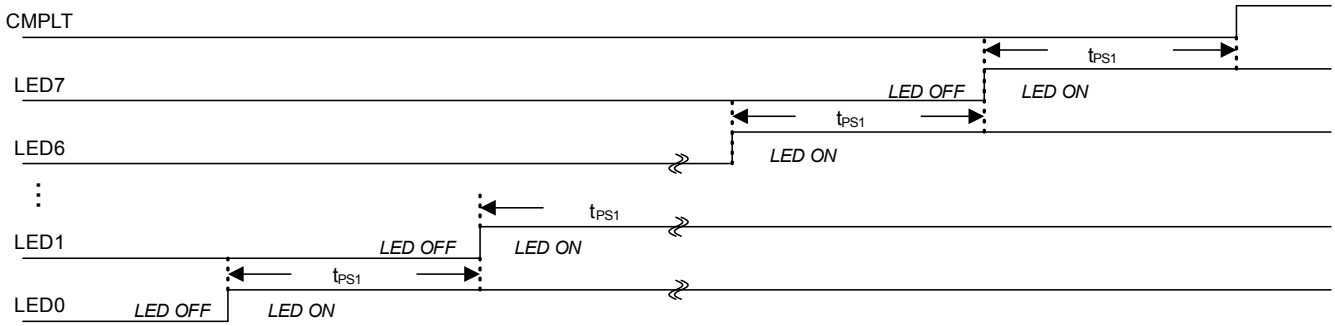


Figure 4. Timing Chart
(Sequential Lighting Phase Shift HAZ=L)

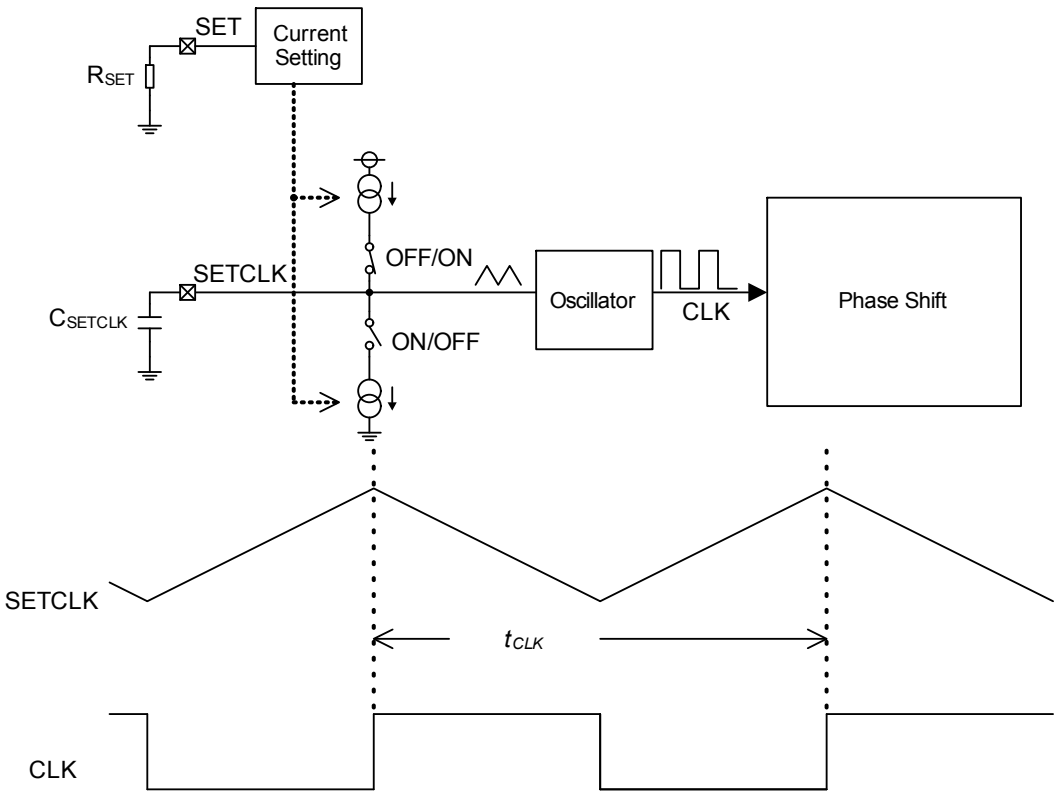


Figure 5. CLK Generation Circuit for Sequential Lighting Phase Shift

Description of Blocks – continued

5. HAZ [Hazard Mode Switching Input]

The BD18362EFV-M is built in hazard mode function. If the HAZ pin is given a high input (≥V_{HAZH}), the LEDs are turned from the all-OFF to the all-ON position after sequential lighting start-up delay (t_{DLY}) passed. However, the switches are turned OFF sequentially (LEDs are light sequentially) at a fixed time (t_{PSH}), this avoids sudden output voltage fluctuations.

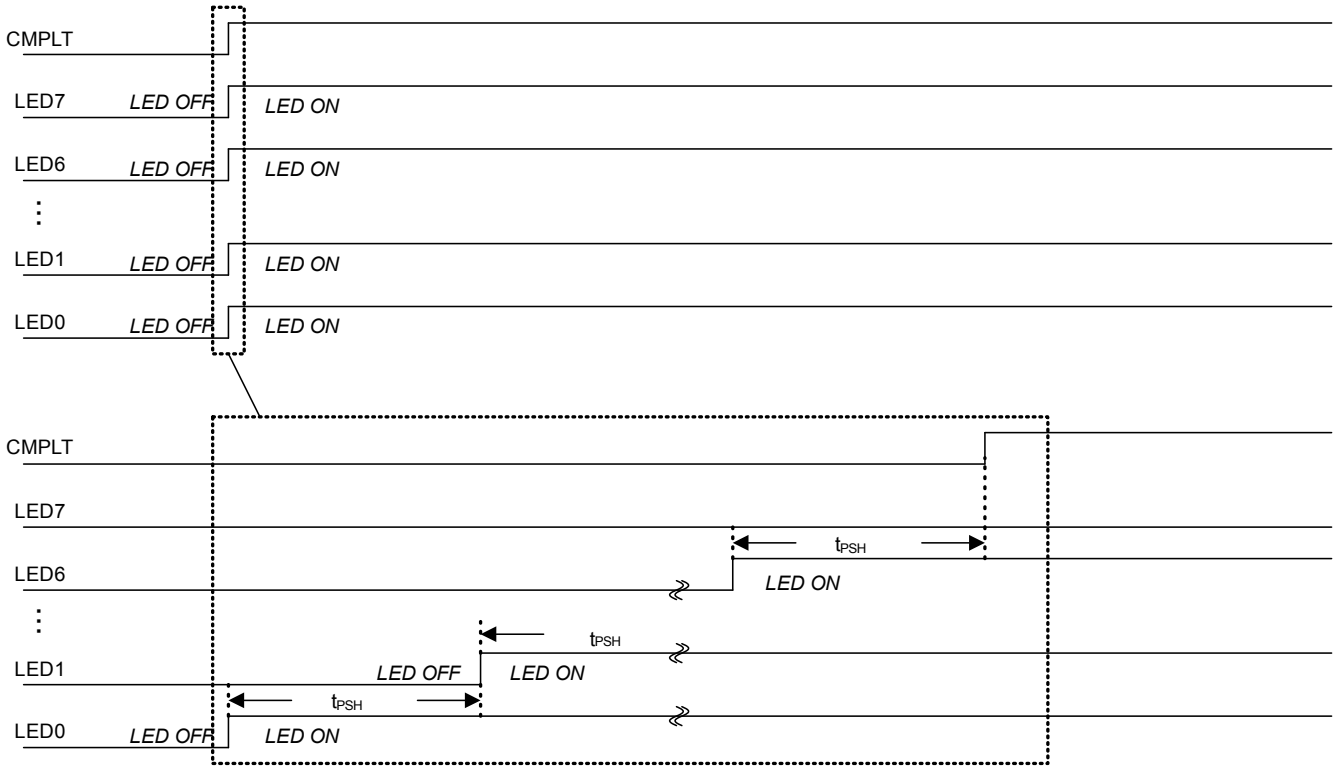


Figure 6. Timing Chart
(Hazard mode HAZ=H)

Description of Blocks – continued

6. SEL [Setting pin for switches in use]

The BD18362EFV-M has 8 switches. Therefore, in cases where only 7 or less switches are used, please short-circuit the board with the pins that are not used. The protective function must be disabled for those switches that are not being used, so that the short detection will not run.

The switches in use determine if the SEL1pin, the SEL2 pin and the SEL3 pin are setting high input ($\geq V_{SELH}$) or low input ($\leq V_{SELL}$).

Switches in use	Protective Function Invalidity Switches	SEL1	SEL2	SEL3
0, 1, 2, 3, 4, 5, 6, 7	-	low	low	low
0, 1, 2, 3, 4, 5, 6	7	high	low	low
0, 1, 2, 3, 4, 5	6, 7	low	high	low
0, 1, 2, 3, 4	5, 6, 7	high	high	low
0, 1, 2, 3	4, 5, 6, 7	low	low	high
0, 1, 2	3, 4, 5, 6, 7	high	low	high
0, 1	2, 3, 4, 5, 6, 7	low	high	high
0	1, 2, 3, 4, 5, 6, 7	high	high	high

The setting will not be changed even if the SEL pin voltage switches temporarily during the sequential lighting phase shift operation.

The settings are changed at a restart. A restart is possible under the following 3 conditions: (1) or (2) or (3)

(1) UVLO detection → UVLO release → Status good delay time passed → Set SEL condition

(2) Thermal shutdown detection → Thermal shutdown release → Status good delay time passed → Set SEL condition

(3) Input $V_{CNT} \leq V_{CNTH}-V_{CNTHYS}$ → Input $V_{CNT} \geq V_{CNTH}$ → Set SEL condition

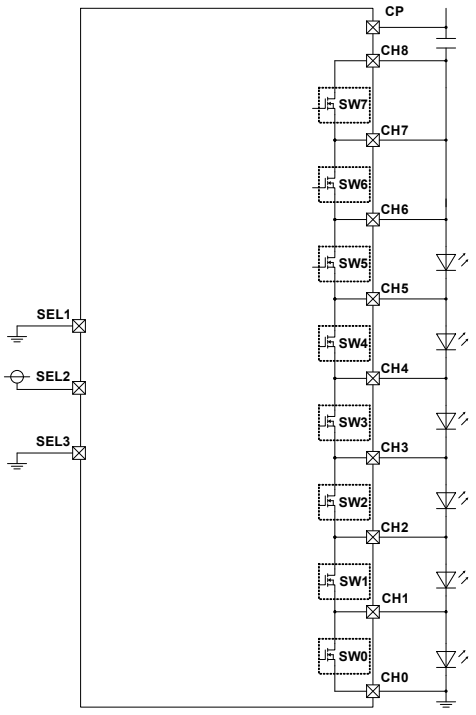


Figure 7. A Circuit for Setting SEL (for using 6 Switches)

Description of Blocks – continued

7. CMPLT [Lighting Complete Signal Output]

When the sequential lighting is complete, the CMPLT pin changes from a low to Hiz.
The BD18362EFV-M has 8 switches. Therefore, in cases where 9 or more switches are used for sequential lighting, a second BD18362EFV-M comes into use. When the lighting of LED by an IC (A) is complete, the CMPLT pin of an IC (A) will give a Hiz output. By connecting the CMPLT pin of an IC (A) and the CNT pin of an IC (B), the LED lighting of an IC (B) will start after the LED lighting of an IC (A) is complete.
Also, the “lighting complete” timing is changed according to the used switches set by the SEL1 pin, the SEL2 pin and the SEL3 pin.
If the 6 and 7 switches are invalidated, the CMPLT pin will have a Hiz output at the time when the start-up of switch 5 is completed.
The CMPLT pin will change Hiz to low under following conditions. (1) or (2) or (3) (refer to Figure19 (c))

(1) UVLO detection → CMPLT=L
(2) Thermal shutdown detection → CMPLT=L
(3) Input $V_{CNT} \leq V_{CNTH}-V_{CNTHYS}$ → CMPLT=L

The CMPLT pin is open drain and needed pulled up resistor for monitoring output signal.

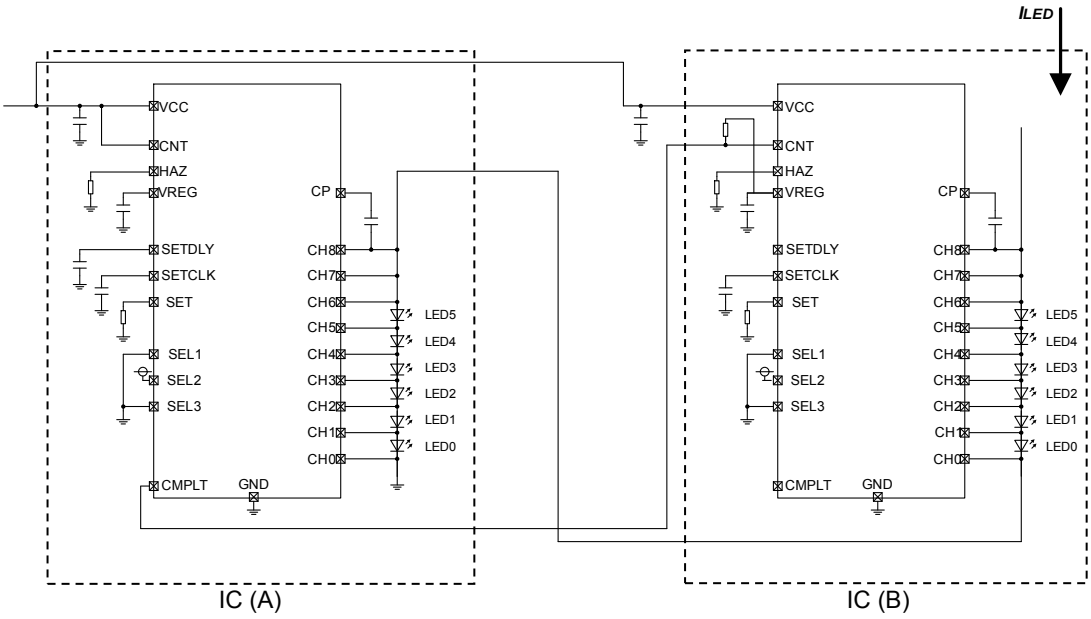


Figure 8. Application Example
(for using 12 Switches)

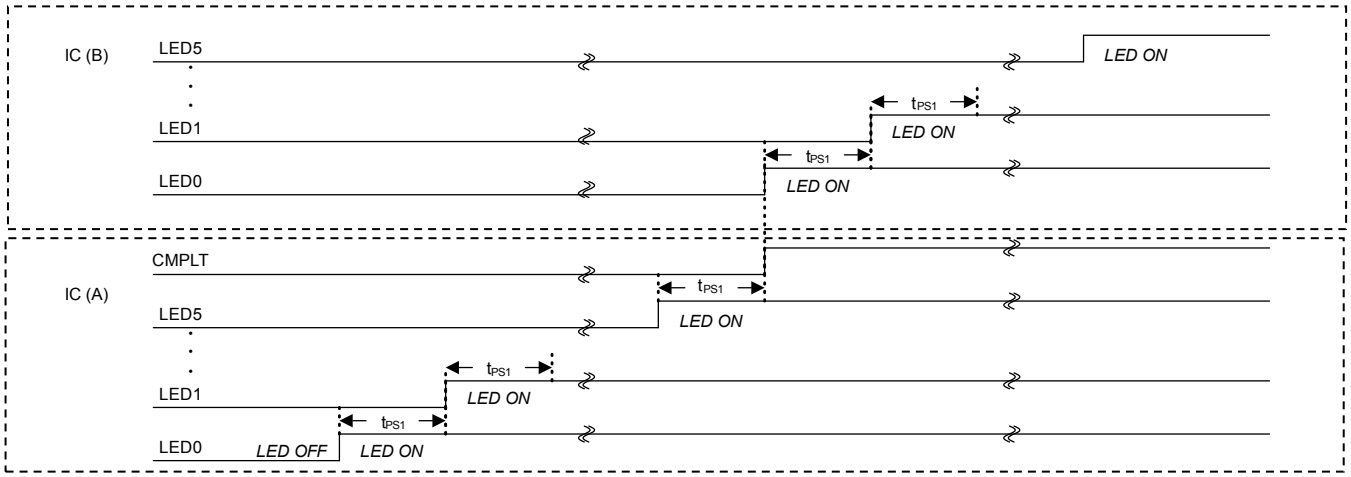


Figure 9. Timing Chart
(for using 12 Switches)

Description of Blocks – continued

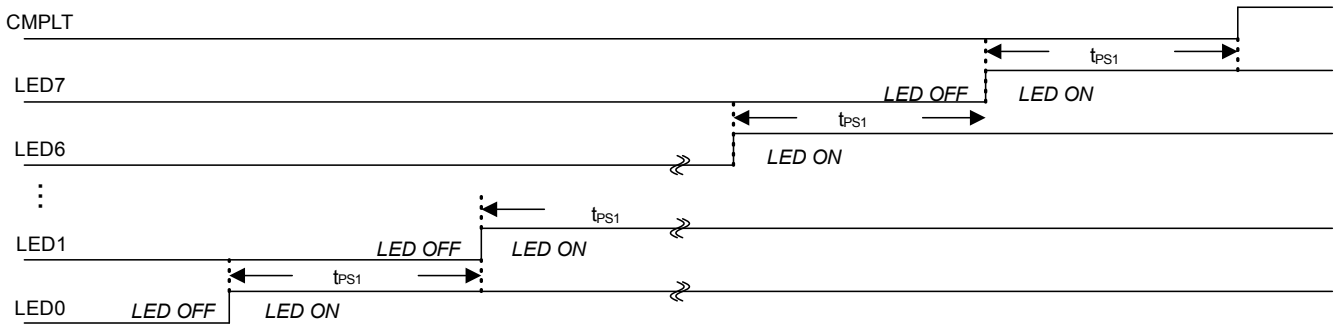


Figure 10. Timing Chart
(CMPLT output function SEL1=L, SEL2=L, SEL3=L)

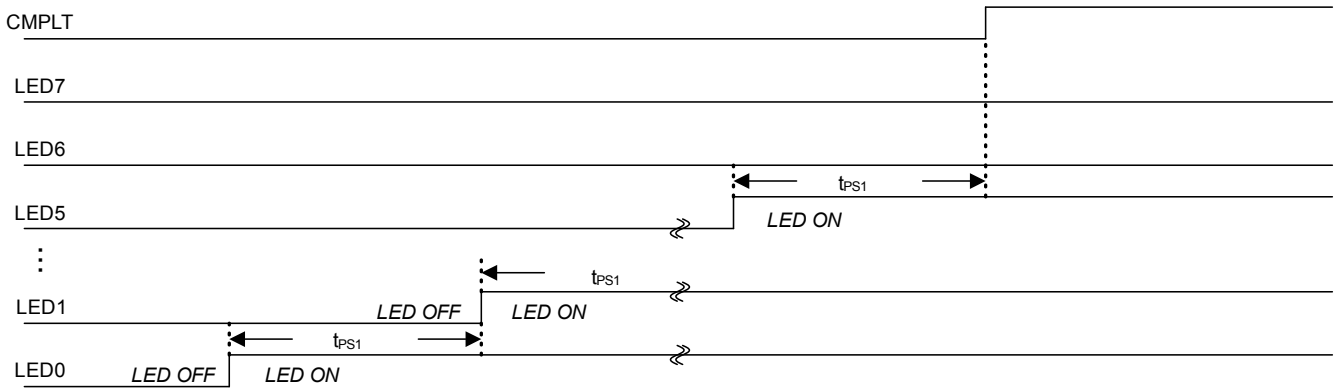


Figure 11. Timing Chart
(CMPLT output function SEL1=L, SEL2=H, SEL3=L)

Description of Blocks – continued

8. CNT [Lighting On/Off Control]

It is possible to control the switches through the CNT pin.
If the CNT pin is given a high input (≥V_{CNTH}), the switches will be turned OFF sequentially and the LEDs are light sequentially after the sequential lighting start-up delay time t_{DLY}.
If the CNT pin is given a low input (≤V_{CNTH}-V_{CNTHYS}), the switches will be turned ON sequentially and the LEDs are unlighted sequentially. Also, the CMPLT pin will have a low output.
The switches are turned ON sequentially (LEDs are unlighted sequentially) at a fixed time (t_{PSL}), this avoids sudden output voltage fluctuations.
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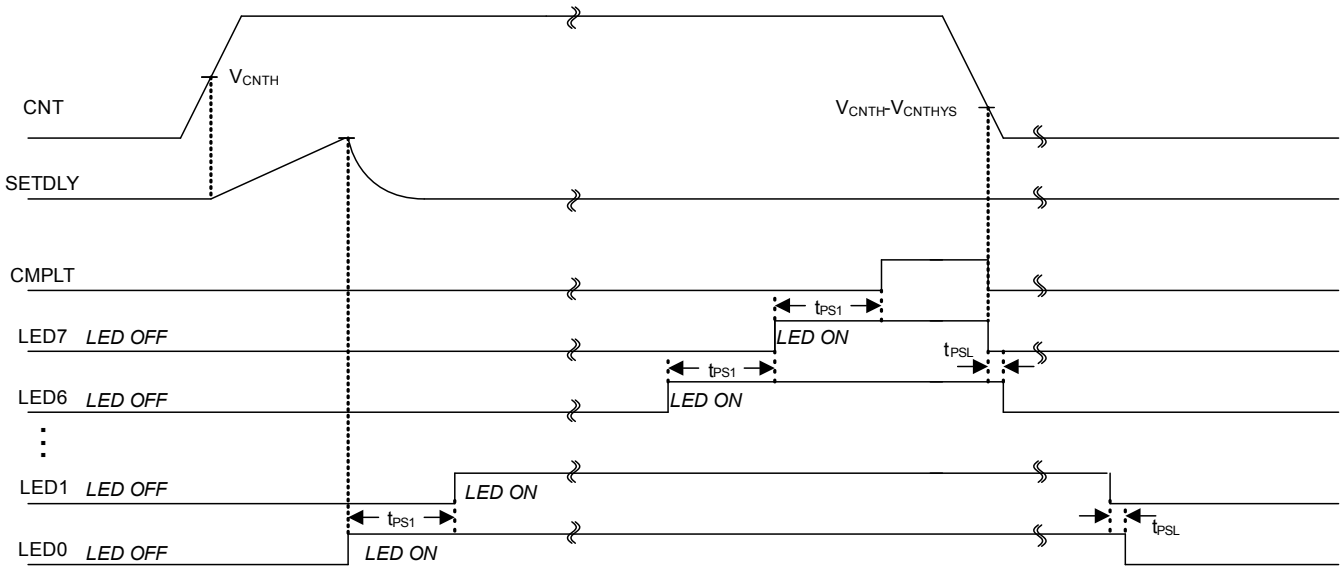


Figure 12. Timing Chart
(The CNT Pin Function)

Description of Blocks – continued

9. LED Short Detection

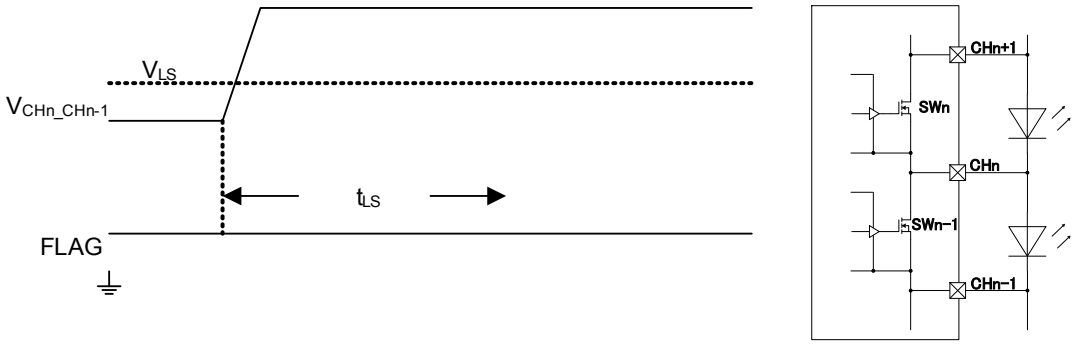
The BD18362EFV-M is built in LED short detection.
While switch is turned OFF, the voltage between CHn-CHn-1 is monitored. If the voltage between CHn-CHn-1 falls below the LED short detection voltage (V_{LS}), an LED short is detected. The FLAG pin will change to low. When SWn-1 turn OFF, the short detection function will be disable in the time (t_{LS}).

$$t_{LS} = t_{PS1} \times 0.5 \ (Typ)$$ when V_{HAZ}=L(≤V_{HAZH} -V_{HAZHYS})

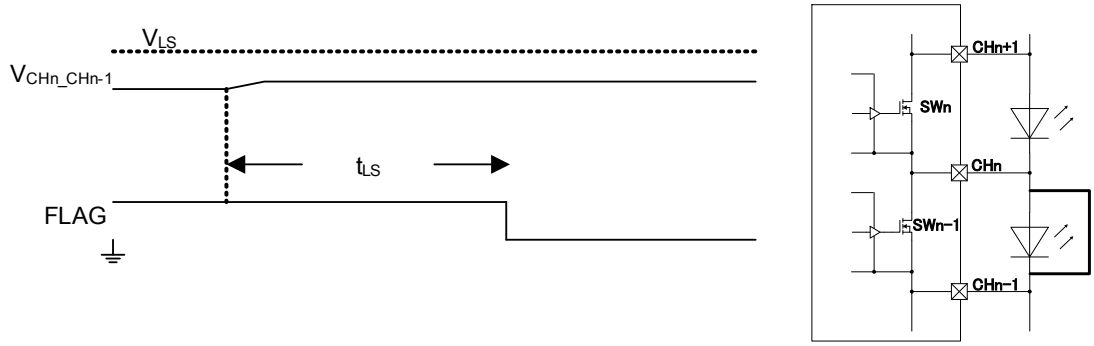
$$t_{LSH} = t_{PSH} \times 0.5 \ (Typ)$$ when V_{HAZ}=H(≥V_{HAZH})

The FLAG pin will change low to Hiz under following conditions. (1) or (2) or (3) (refer to Figure19 (a))
(1) UVLO detection → UVLO release → Status good delay time passed → FLAG=Hiz
(2) Thermal shutdown detection → Thermal shutdown release → FLAG=Hiz
(3) Input V_{CNT} ≤ V_{CNTH}-V_{CNTHYS} → FLAG=Hiz

The LED short detection function is invalid with regard to the unused switches set by the SEL pin.



(a) Normal Operation



(b) LED Short Operation

Figure 13. Functionality of LED Short Detection

Description of Blocks – continued

10. LED Open Protection

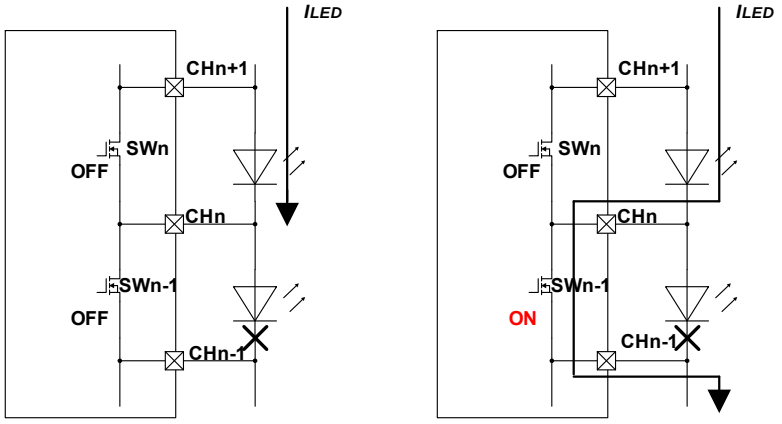
The BD18362EFV-M is built in LED open protection.
While switch is turned OFF, the voltage between CHn-CHn-1 is monitored. If the voltage between CHn-CHn-1 is detected to be the LED open protection voltage (V_{LO}) during the monitoring, SWn-1 will be turned ON immediately and this will prevent a destruction of the switch. When the t_{LO} time has passed after SWn-1 turned OFF, the FLAG pin will change to low. The other switches keep lighting phase shift after detecting LED open.

$$t_{LO} = t_{PS1} \times 0.5 \ (Typ)$$ when V_{HAZ}=L(≤V_{HAZH} -V_{HAZHYS})

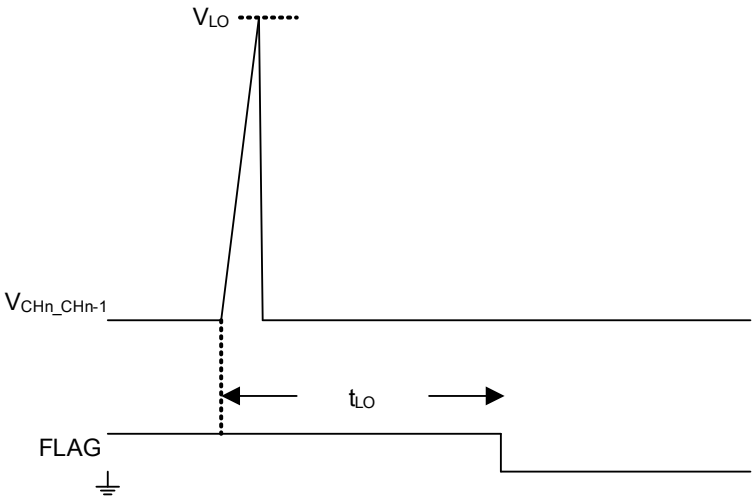
$$t_{LOH} = t_{PSH} \times 0.5 \ (Typ)$$ when V_{HAZ}=H(≥V_{HAZH})

The FLAG pin will change low to Hiz under following conditions. (1) or (2) or (3) (refer to Figure 19)
(1) UVLO detection → UVLO release → FLAG=Hiz
(2) Thermal shutdown detection → Thermal shutdown release → FLAG=Hiz
(3) Input V_{CNT} ≤ V_{CNTH}-V_{CNTHYS} → FLAG=Hiz

The LED open protection function is invalid with regard to the unused switches set by the SEL pin.



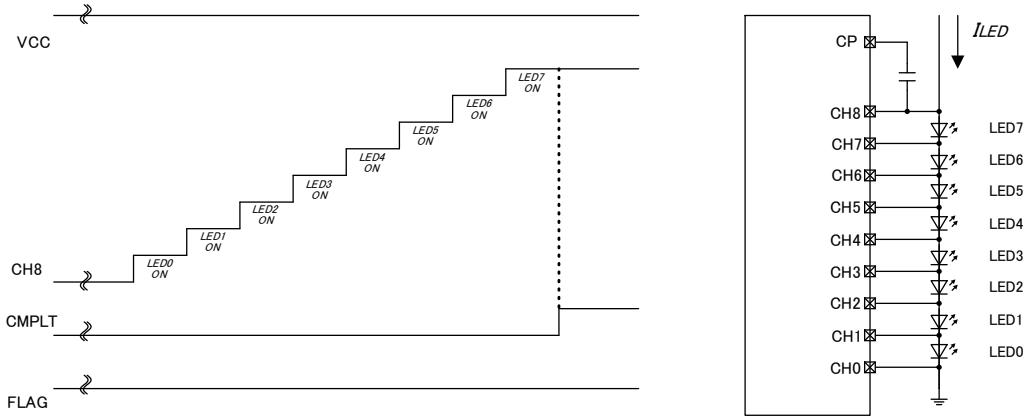
(a) LED Open (SW=OFF) (b) LED Open (SW=ON)



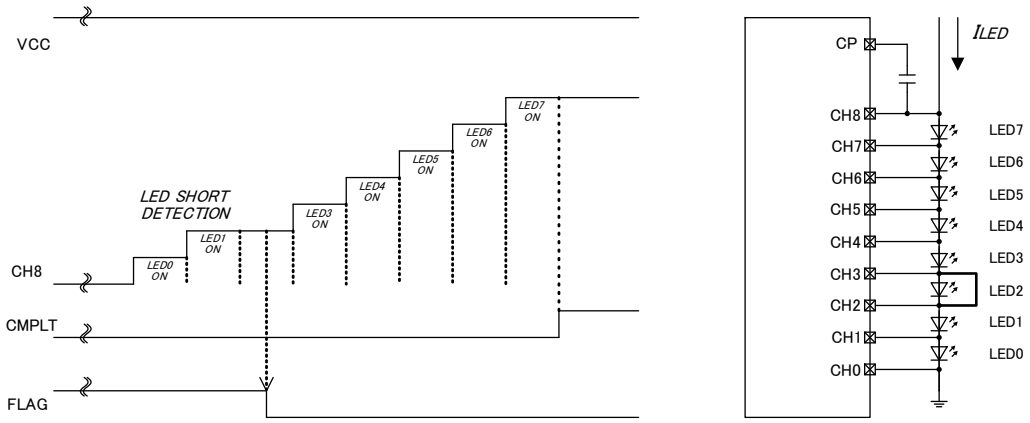
(c) LED Open (Timing chart)

Figure 14. Functionality of LED Open Protection

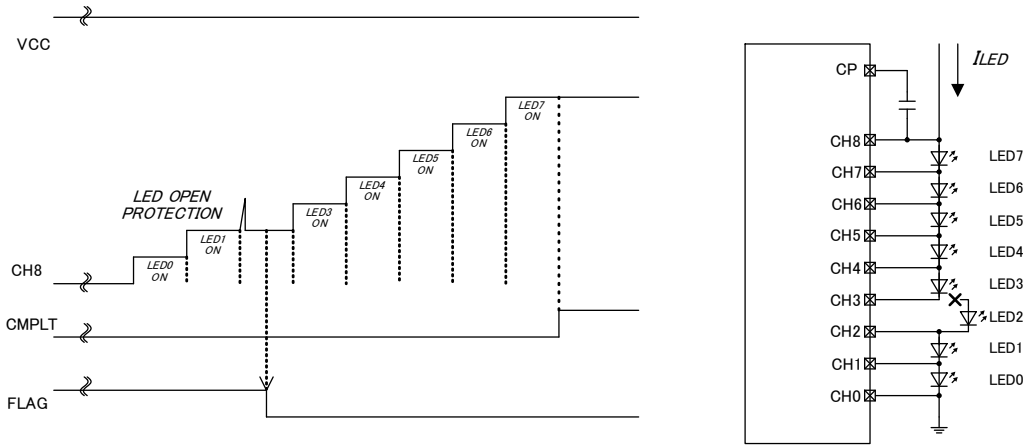
Description of Blocks – continued



(a) Normal Operation



(b) LED Short Detection (e.g. LED2 Short Mode)



(c) LED Open Protection (e.g. LED2 Open Mode)

Figure 15. Timing Chart
(LED Short/LED Open)

Description of Blocks – continued

11. WDTDLY [Watchdog Timer for SETDLY]

The BD18362EFV-M monitors the t_{DLY} (sequential lighting start-up delay time). Since the t_{DLY} cannot be set if the capacitor connected to the SETDLY pin has a short, the LEDs will come unlighted.
The WDTDLY starts monitoring when the SG pin output has a Hiz and the CNT pin is given a high input (≥V_{CNTH}).
If the t_{DLY} is not detected within t_{WDTDLY}, there will be a time-out and the FLAG pin changes to low.
When there is a time-out, the LEDs will all-light automatically. However, the switches are turned OFF sequentially (LEDs are light sequentially) at a fixed time (t_{PSH}).

The FLAG pin will change low to Hiz under following conditions. (1) or (2) or (3) (refer to Figure 19 (a))
(1) UVLO detection → UVLO release → FLAG=Hiz
(2) Thermal shutdown detection → Thermal shutdown release → FLAG=Hiz
(3) Input $V_{CNT} \leq V_{CNTH}$-V_{CNTHYS} → FLAG=Hiz

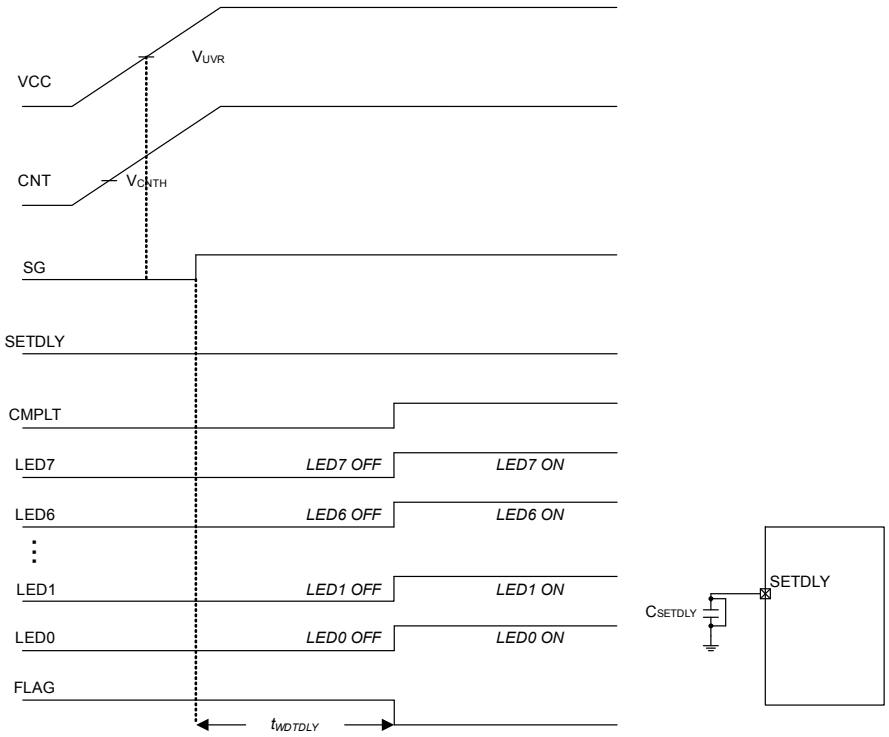


Figure 16. Timing Chart
(The SETDLY short to GND)

Description of Blocks – continued

12. WDTCLK [Watchdog Timer for SETCLK]

The BD18362EFV-M monitors the sequential lighting phase time. Since the t_{CLK} cannot be set if the capacitor connected to the SETCLK pin has a short, the LEDs will come unlighted.
The WDTCLK starts monitoring when the SG pin change from low to Hiz and the CNT pin is given a high input (≥V_{CNTH}). If the clock period (t_{CLK}) is not detected within t_{WDTCLK}, there will be a time-out and the FLAG pin changes to low.
When there is a time-out, the LEDs will all-light automatically. However, the switches are turned OFF sequentially (LEDs are light sequentially) at a fixed time (t_{PSH}).

The FLAG pin will change low to Hiz under following conditions. (1) or (2) or (3) (refer to Figure 19)
(1) UVLO detection → UVLO release → FLAG = Hiz
(2) Thermal shutdown detection → Thermal shutdown release → FLAG = Hiz
(3) Input $V_{CNT} \leq V_{CNTH}$-V_{CNTHYS} → FLAG = Hiz

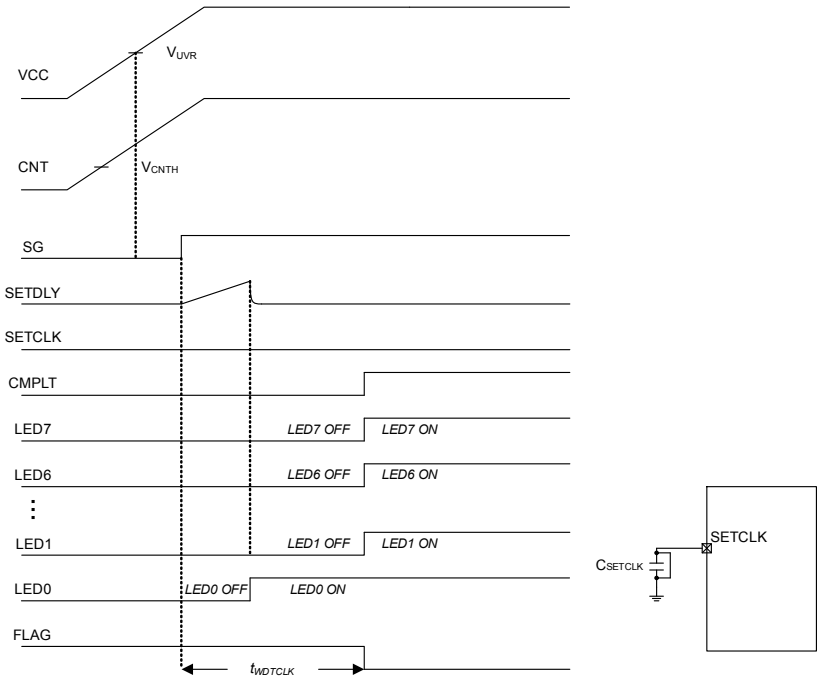


Figure 17. Timing Chart
(The SETCLK Short to GND)

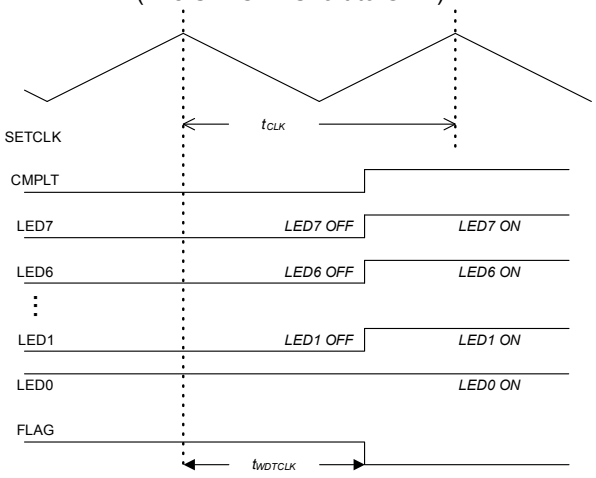
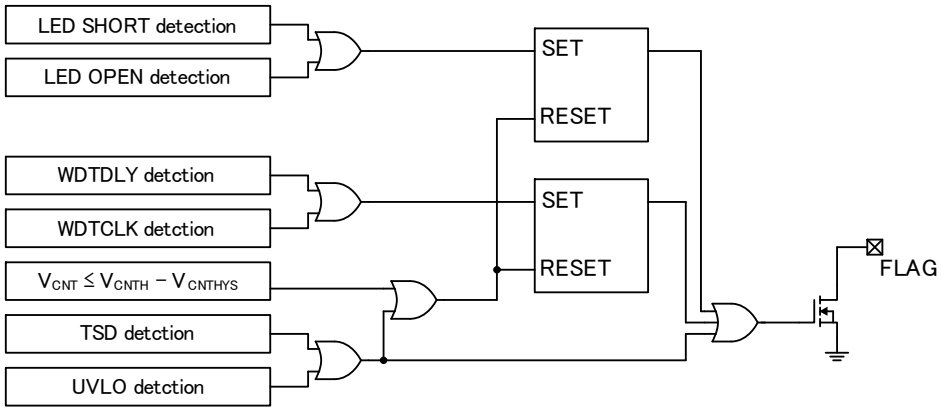


Figure 18. Timing Chart
(The CLK in Abnormal)

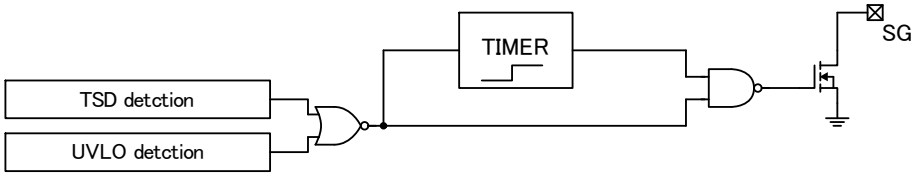
Description of Blocks – continued

13. Monitor Function

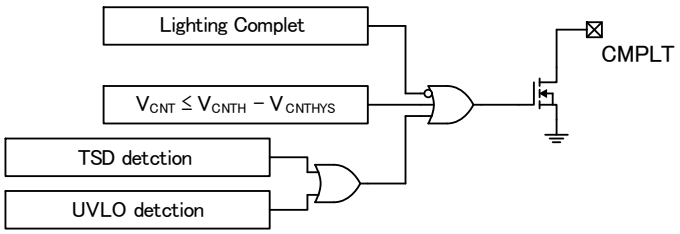
BD18362EFV-M has pins (SG, FLAG and CMPLT) for monitoring condition. These pins are open drain and needed pull up resistor for monitoring condition.



(a) The FLAG Pin Equivalence Circuit



(b) The SG Pin Equivalence Circuit



(c) The CMPLT Pin Equivalence Circuit

Figure 19. Monitor Pin Equivalence Circuits

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage (VCC)	V_{CC}	-0.3 to +70	V
CNT, HAZ Voltage	V_{CNT}, V_{HAZ}	-0.3 to +70	V
VREG Voltage	V_{REG}	-0.3 to +7 ≤ V_{CC}	V
SETDLY, SETCLK Voltage	V_{SETDLY}, V_{SETCLK}	-0.3 to V_{REG}+0.3 ≤ +7	V
SEL1, SEL2, SEL3 Voltage	V_{SEL1}, V_{SEL2}, V_{SEL3}	-0.3 to V_{REG}+0.3 ≤ +7	V
CMPLT, SG, FLAG Voltage	V_{CMPLT}, V_{SG}, V_{FLAG}	-0.3 to +7	V
CP Voltage	V_{CP}	-0.3 to +67	V
CP to CH8 Voltage	V_{VCP_CH8}	-0.3 to +7	V
CFP to CFM Voltage	V_{CFP_CFM}	-0.3 to +7	V
CHn Voltage*(Note 1)*	V_{CHn}	-0.3 to +60	V
CHn to CHn-1 Voltage*(Note 1)*	V_{CHn_CHn-1}	-0.3 to +20	V
Maximum SWn Bypass Current*(Note 2)*	I_{SWn}	1.0	A
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

(Note 1) CHn: n=0 to 8

(Note 2) SWn: n=0 to 7

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSSOP-B28				
Junction to Ambient	θ_{JA}	107.0	25.1	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	6	3	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Input Voltage(Note 6) (Note 7)	V_{CC}	5.5	13	60	V
Operating Temperature	Topr	-40	+25	+125	°C
Maximum Total LED Voltage	V_{LED}	-	-	48	V
CHn to CHn-1 LED Input Range	V_{CHn_CHn-1}	1.2	-	9	V
Sequential Lighting Phase Time Setting Range	t_{PS1}	5	-	100	ms
Sequential Lighting Start-up Delay Time Setting Range	t_{DLY}	-	-	225	ms

(Note 6) Supply input voltage range can be considered based on power dissipation.
(Note 7) At start-up time, please apply a voltage above 6.0V once. The value is the voltage range after the temporary rise to 6.0V.

Recommended Setting Parts Range

Parameter	Symbol	Min	Typ	Max	Unit
Capacitor Connecting to the VREG Pin	C_{VREG}	1.0	2.2	4.7	µF
Capacitor for Charge Pump	C_{CP}, C_{CF}	0.001	0.047	0.22	µF
Resistor for Sequential Lighting Phase Time/ Sequential Lighting Start-up Delay Time	R_{SET}	6	-	40	kΩ
Capacitor for Sequential Lighting Start-up Delay Time	C_{SETDLY}	-	-	10	µF
Capacitor for Sequential Lighting Phase Time	C_{SETCLK}	0.001	-	0.047	µF

Electrical Characteristics (Unless otherwise specified: V_{CC}=13V Ta=-40°C to +125°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Total]						
VCC Input Current	I_{VCC}	-	3.8	7.0	mA	V_{CNT}=0V, V_{CH0}=0V R_{SET}=22kΩ, C_{SETCLK}=0.01μF
UVLO Detection Voltage	V_{UVD}	4.7	5.1	5.5	V	V_{CC}: Sweep down
UVLO Release Voltage	V_{UVR}	4.95	5.40	5.85	V	V_{CC}: Sweep up
UVLO Hysteresis Voltage	V_{HYS}	-	0.3	-	V	
[Internal Reference Voltage]						
Regulator Output	V_{REG}	4.5	5.0	5.5	V	C_{VREG}=2.2μF I_{VREG}=0mA to 2mA
[Charge Pump]						
Charge Pump Output Voltage	V_{CP}	-	-	7	V	V_{CP}-V_{CH8}
Differential Voltage of Flying Capacitor	V_{CF}	-	-	7	V	V_{CFP}-V_{CFM}
[SET, SETDLY, SETCLK]						
Coefficient for Sequential Lighting Phase Time	K_{PS}	278	320	368	-	t_{PS1}=K_{PS} x R_{SET} x C_{SETCLK} [s] V_{HAZ} =0V
Coefficient for Sequential Lighting Start-up Delay Time	K_{DLY}	2.23	2.67	3.20	-	t_{DLY}=K_{DLY} x R_{SET} x C_{SETDLY} [s]
Sequential Lighting Phase Time In the Hazard Mode	t_{PSH}	105	140	180	μs	V_{HAZ}=5V
Turn Off Phase Time In the CNT=L	t_{PSL}	105	140	180	μs	V_{CNT}=5V→0V
[CMPLT, SG, FLAG]						
CMPLT Output Voltage Low	V_{CMPLTL}	-	-	0.2	V	I_{CMPLT}=1mA
CMPLT Leak Current	$I_{CMPLTLK}$	-	-	1	μA	V_{CMPLT}=5.5V
SG Output Voltage Low	V_{SGL}	-	-	0.2	V	I_{SG}=1mA
SG Leak Current	I_{SGLK}	-	-	1	μA	V_{SG}=5.5V
FLAG Output Voltage Low	V_{FLAGL}	-	-	0.2	V	I_{FLAG}=1mA
FLAG Leak Current	I_{FLAGLK}	-	-	1	μA	V_{FLAG}=5.5V
SG Delay Time	t_{dSG}	415	590	765	μs	
WDTDLY Time Out	t_{WDTDLY}	245	350	455	ms	
WDTCLK Time Out	t_{WDTCLK}	80	115	150	ms	

Electrical Characteristics – continued (Unless otherwise specified: V_{CC}=13V Ta=-40°C to +125°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[CNT, HAZ]						
CNT Pin Input Current 1	I_{CNT1}	-10	-2.5	-	μA	V_{CNT}=0V
CNT Pin Input Current 2	I_{CNT2}	-	0	5	μA	V_{CNT}=60V
CNT Threshold Voltage	V_{CNTH}	0.9	1.0	1.1	V	Sweep up
CNT Threshold Hysteresis Voltage	V_{CNTHYS}	-	100	-	mV	
HAZ Pin Input Current 1	I_{HAZ1}	-10	-2.5	-	μA	V_{HAZ}=0V
HAZ Pin Input Current 2	I_{HAZ2}	-	0	5	μA	V_{HAZ}=60V
Hazard Mode Threshold Voltage	V_{HAZH}	0.9	1.0	1.1	V	Sweep up
Hazard Mode Threshold Hysteresis Voltage	V_{HAZHYS}	-	100	-	mV	
[SEL1, SEL2, SEL3]						
SEL1, SEL2, SEL3 High Level Input Voltage	V_{SELH}	3.6	-	V_{REG}	V	
SEL1, SEL2, SEL3 Low Level Input Voltage	V_{SELL}	0	-	1.1	V	
SEL1, SEL2, SEL3 Pin Input Current	I_{SEL}	10	20	30	μA	V_{SEL1}=5V, V_{SEL2}=5V, V_{SEL3}=5V
[CH]						
CHn to CHn-1 Switch ON Resistance	R_{SW}	-	230	460	mΩ	I_{SW}=300mA
CH8 to CH0 Switch Total ON Resistance	R_{SW70}	-	0.95	2.2	Ω	All Switches On I_{SW70}=300mA
LED Open Detection Voltage	V_{LO}	9.0	-	15	V	V_{CHn_CHn-1}: Sweep up
LED Short Detection Voltage	V_{LS}	-	-	1.2	V	V_{CHn_CHn-1}: Sweep up

Typical Performance Curves (Reference Data)
(Unless otherwise specified: Ta=25°C V_{CC}=13V)

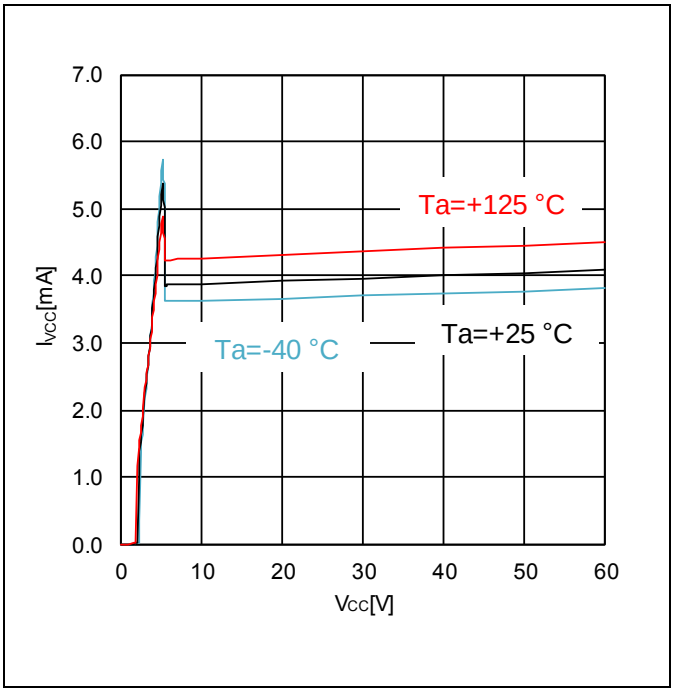


Figure 20. I_{VCC} vs V_{CC}

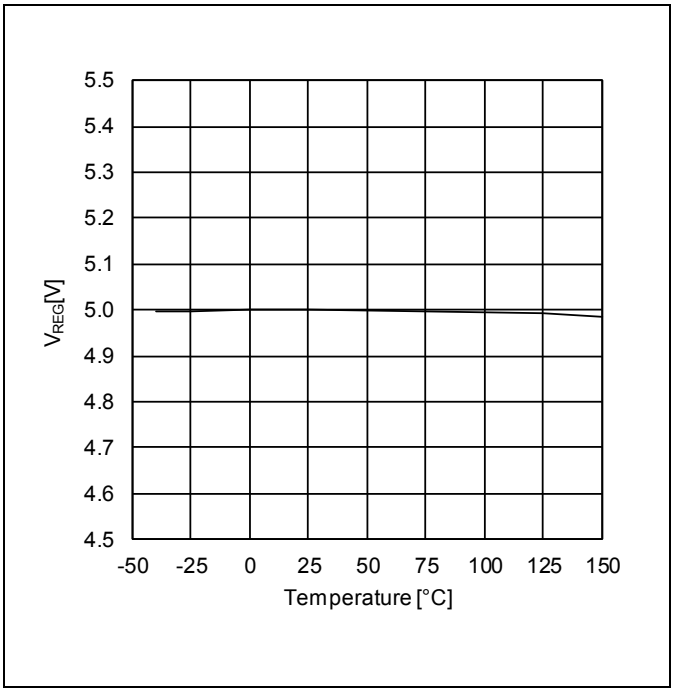


Figure 21. V_{REG} vs Temperature

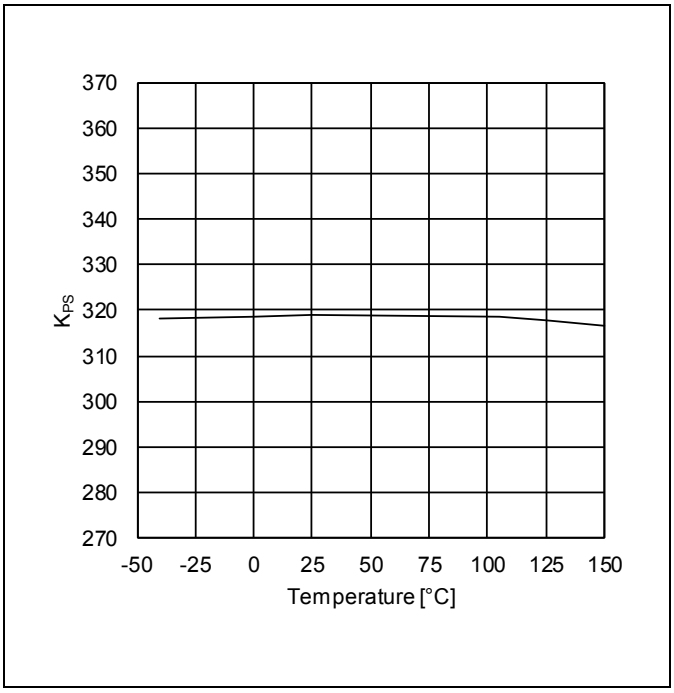


Figure 22. K_{PS} vs Temperature
(C_{SETCLK}=0.0047µF, R_{SET}=10kΩ)

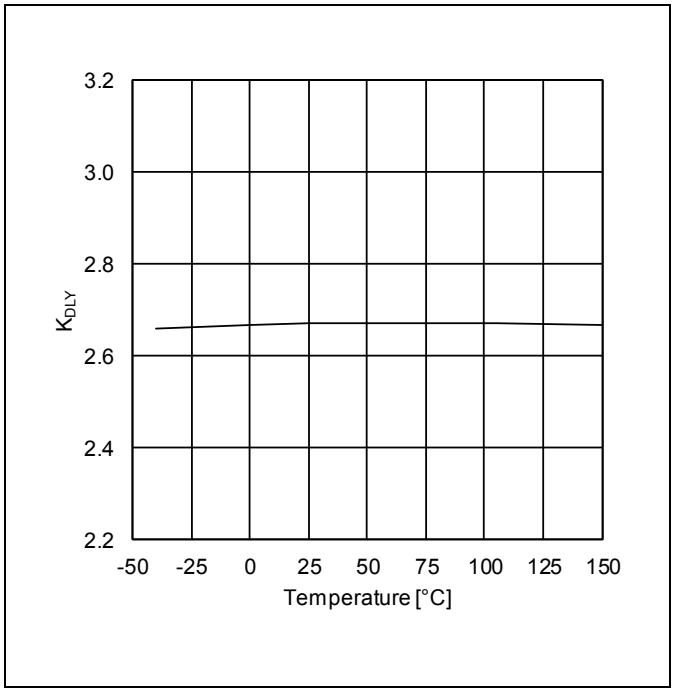


Figure 23. K_{DLY} vs Temperature
(C_{SETDLY}=0.01µF, R_{SET}=10kΩ)

Typical Performance Curves (Reference Data) - continued
(Unless otherwise specified: Ta=25°C V_{CC}=13V)

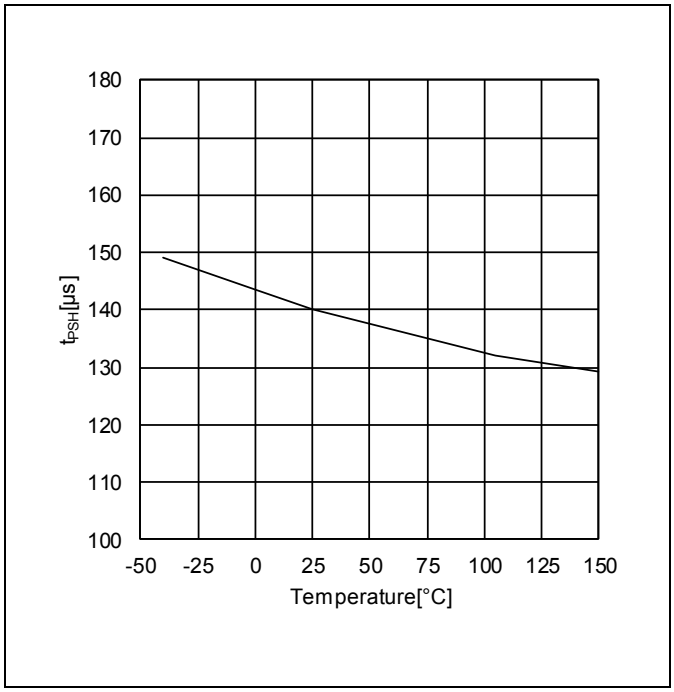


Figure 24. t_{PSH} vs Temperature

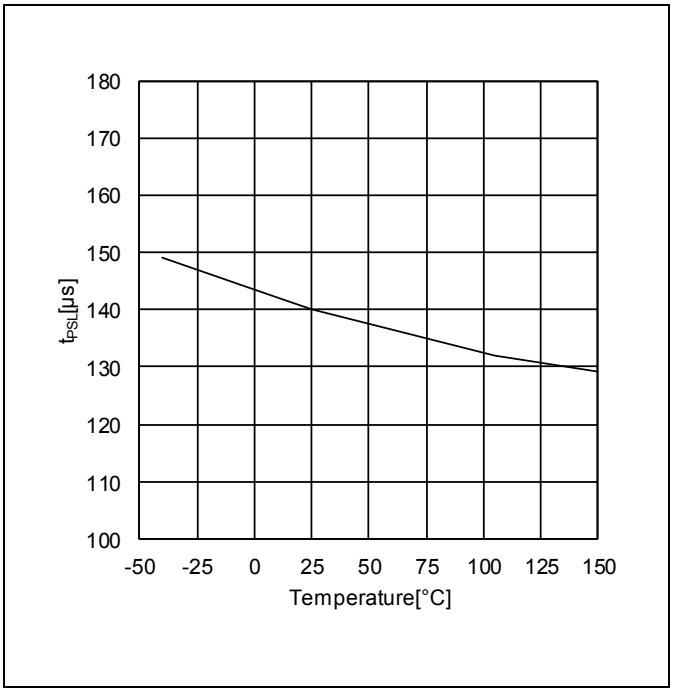


Figure 25. t_{PSL} vs Temperature

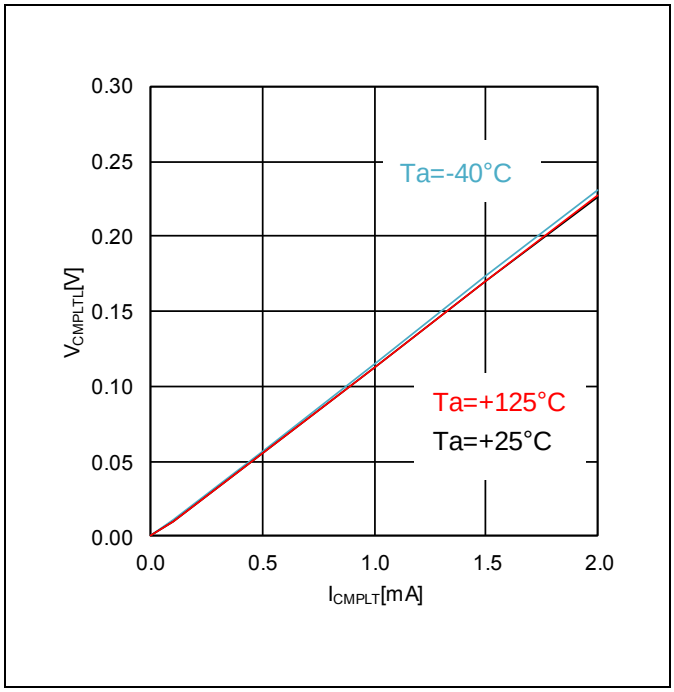


Figure 26. V_{CMPLTL} vs I_{CMPLT}

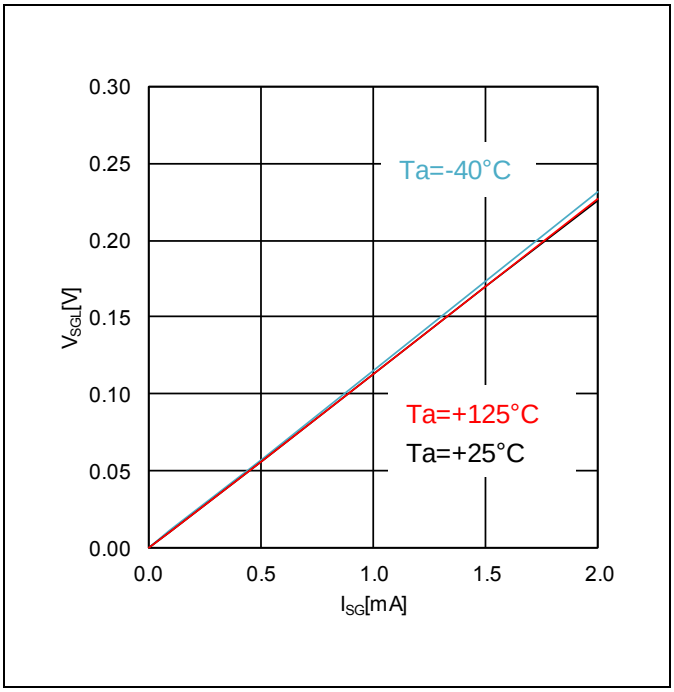


Figure 27. V_{SGL} vs I_{SG}

Typical Performance Curves (Reference Data) - continued
(Unless otherwise specified: Ta=25°C V_{CC}=13V)

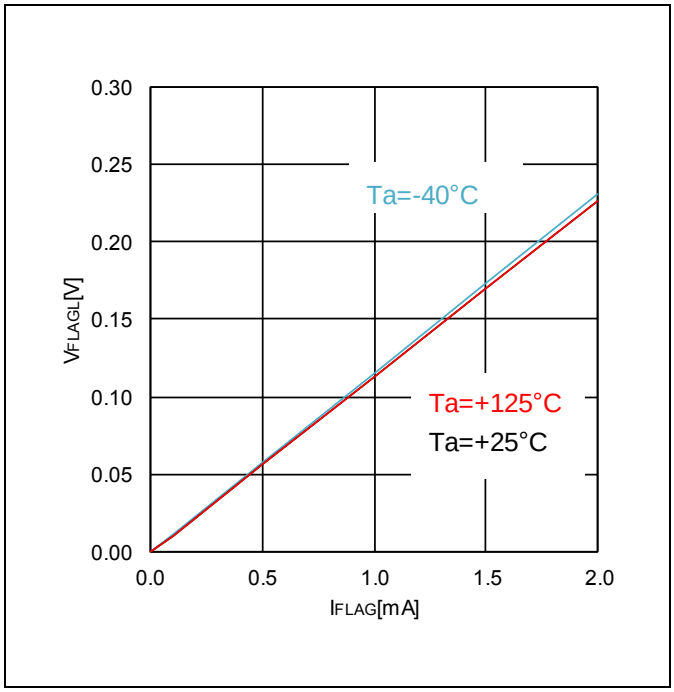


Figure 28. V_{FLAGL} vs I_{FLAG}

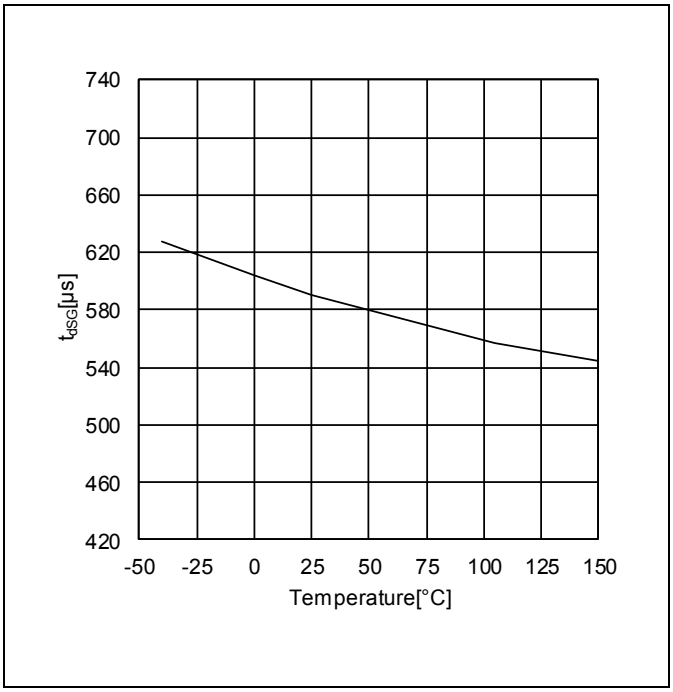


Figure 29. t_{dSG} vs Temperature

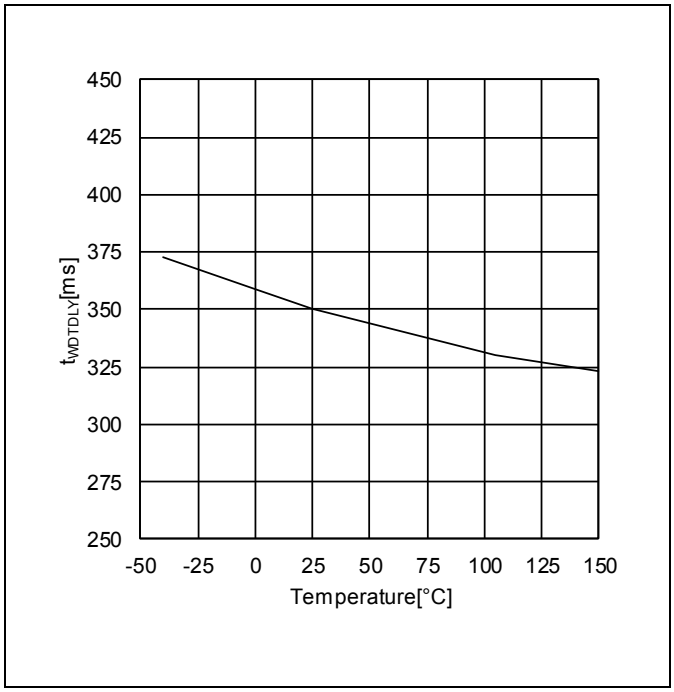


Figure 30. t_{WDTDLY} vs Temperature

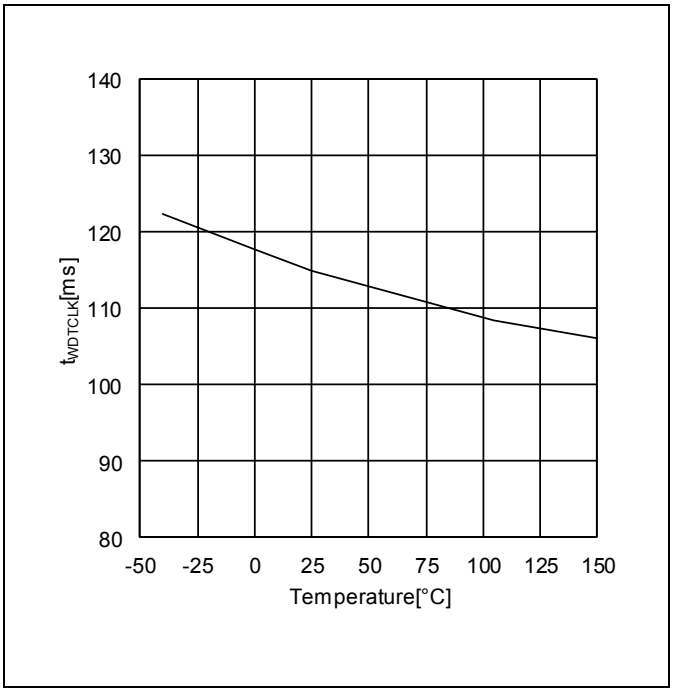


Figure 31. t_{WDTCLK} vs Temperature

Typical Performance Curves (Reference Data) - continued
(Unless otherwise specified: Ta=25°C V_{CC}=13V)

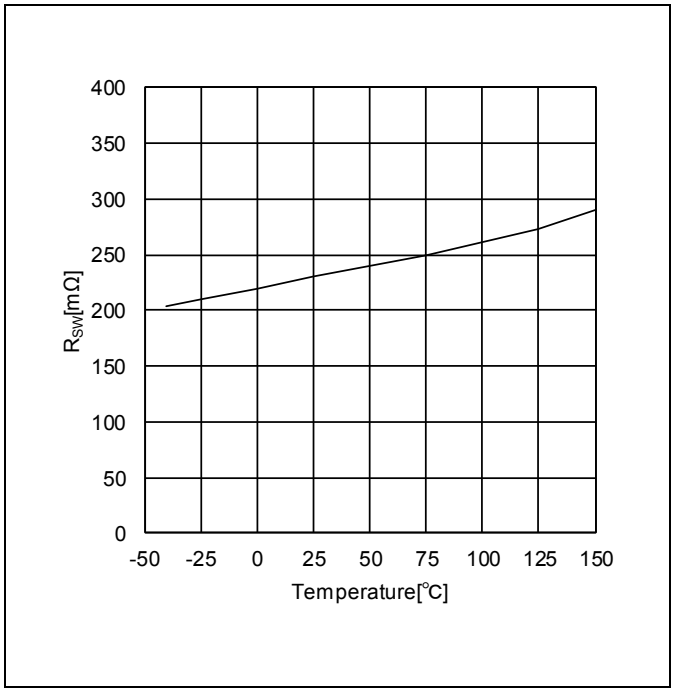


Figure 32. R_{SW} vs Temperature
(I_{SW}=300mA)

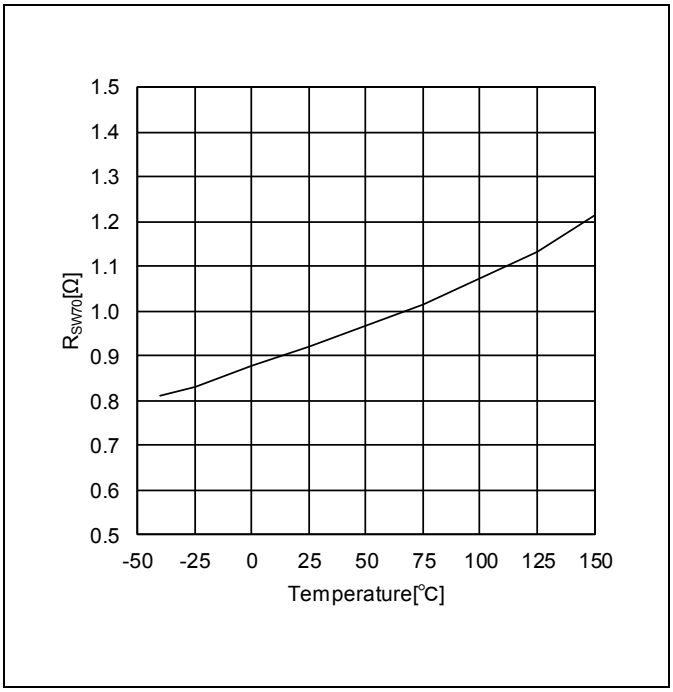


Figure 33. R_{SW70} vs Temperature
(I_{SW70}=300mA)

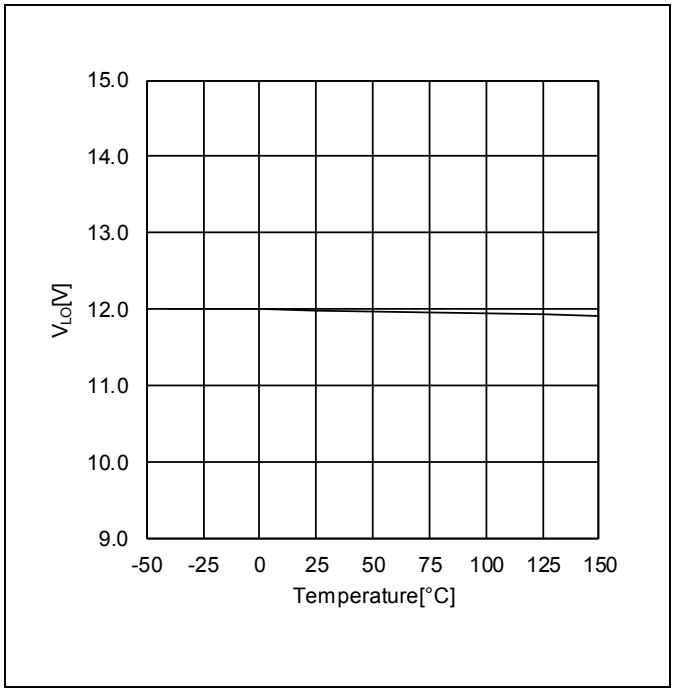


Figure 34. V_{LO} vs Temperature

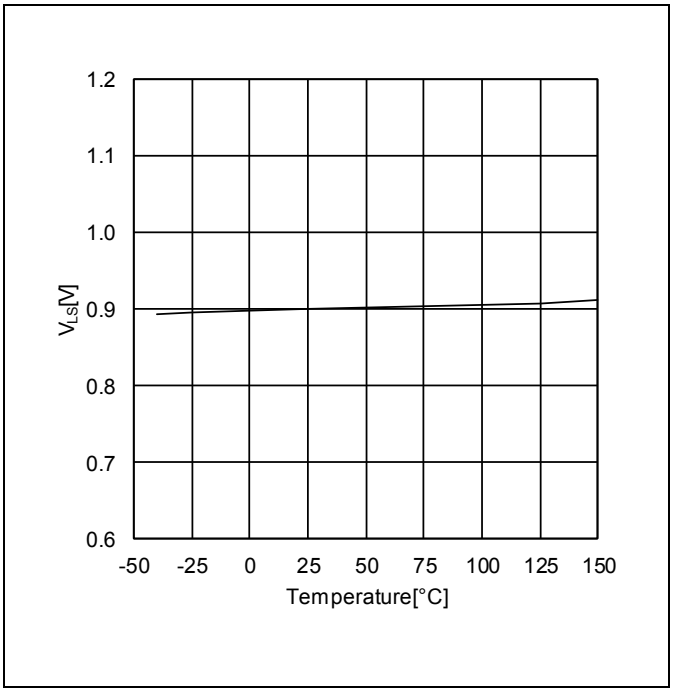


Figure 35. V_{LS} vs Temperature

Timing Chart

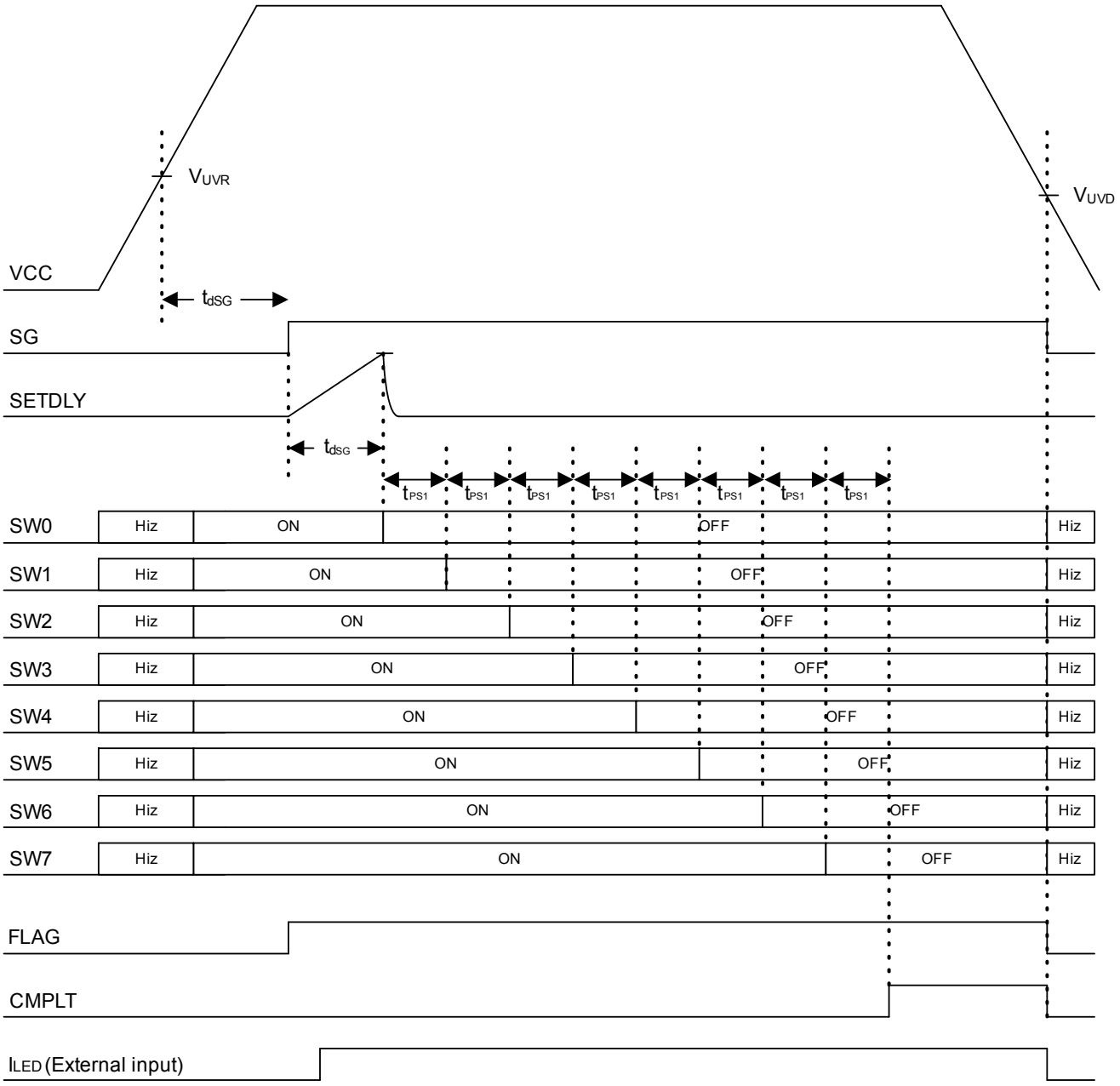
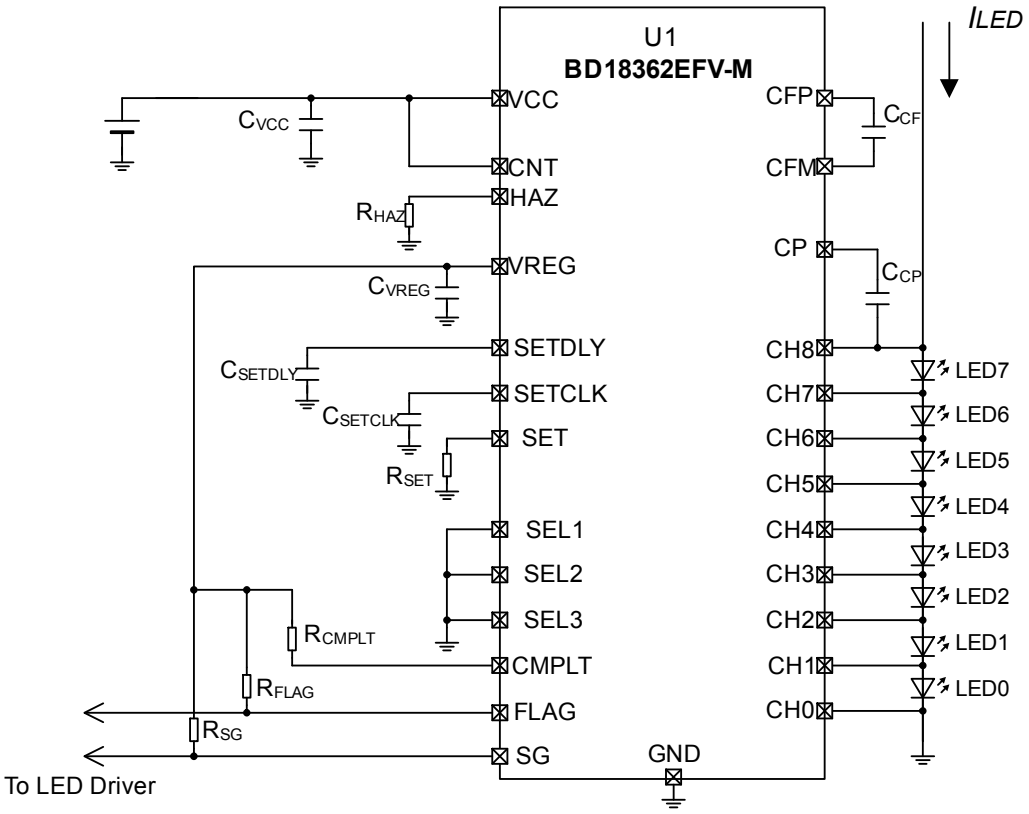


Figure 36. Typical Timing Chart

Recommended Application Circuit



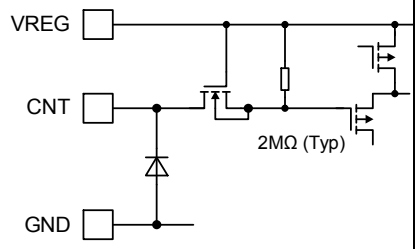
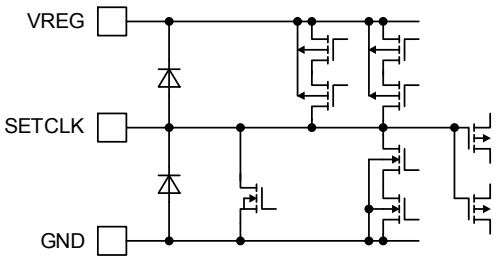
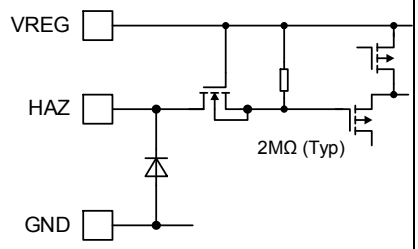
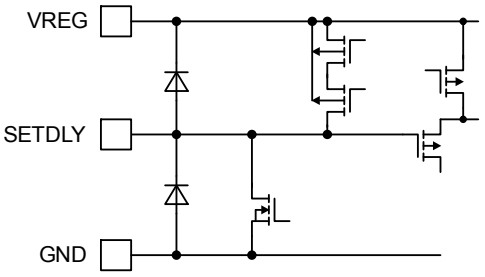
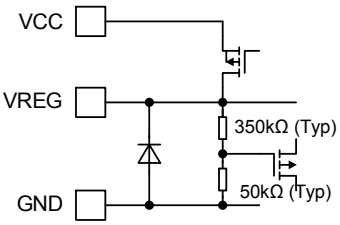
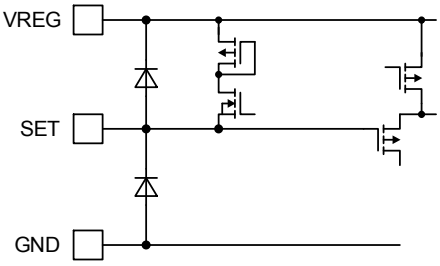
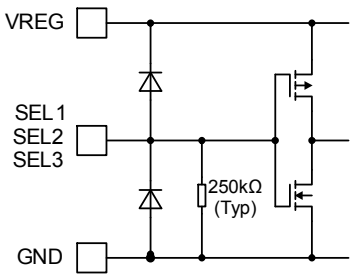
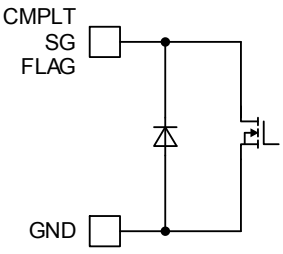
Recommended Parts List

(8 switches, t_{PS1}=15ms, t_{DLY}=1.25ms)

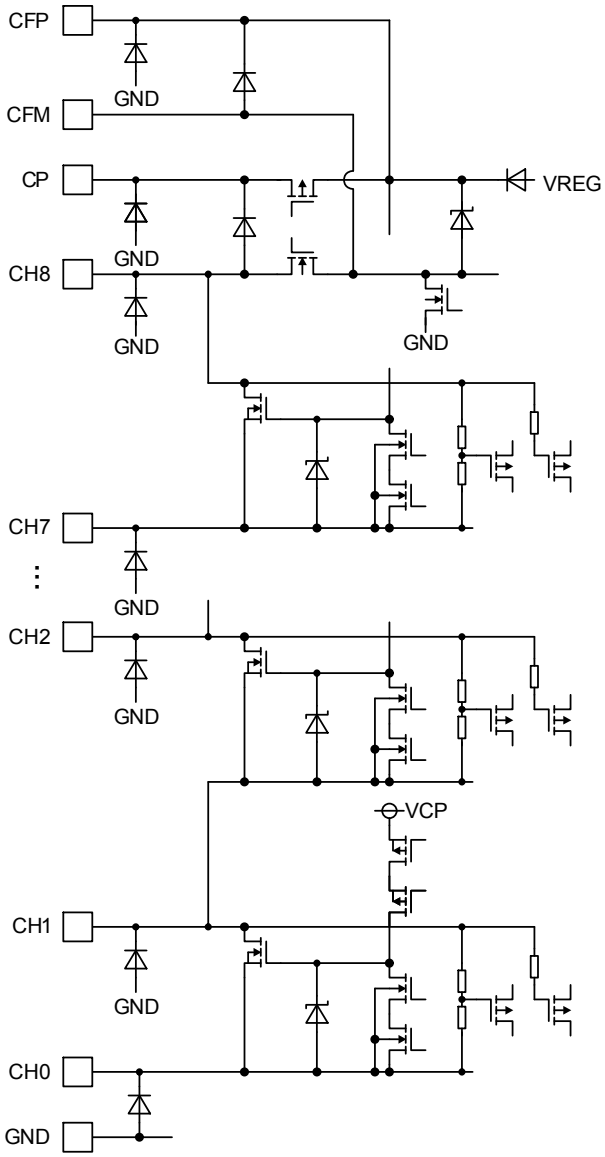
Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18362EFV-M	-	-	ROHM
Resistor	R_{HAZ}	MCR03EZPJ103	10	kΩ	ROHM
	R_{SET}	MCR03EZPD1002	10	kΩ	ROHM
	R_{CMPLT}	MCR03EZPJ223	22	kΩ	ROHM
	R_{FLAG}	MCR03EZPJ223	22	kΩ	ROHM
	R_{SG}	MCR03EZPJ223	22	kΩ	ROHM
Capacitor	C_{VCC}	GCM31CC72A225KE01L	2.2	μF	murata
	C_{VREG}	GCM21BR71C225KA49	2.2	μF	murata
	C_{SETDLY}	GCM188R11H473JA40	0.047	μF	murata
	C_{SETCLK}	GCM2162C1H472JA01	0.0047	μF	murata
	C_{CF}	GCM188R11H473JA40	0.047	μF	murata
	C_{CP}	GCM188R11H473JA40	0.047	μF	murata

- C_{VCC}: Choose rated voltage according to input voltage range.
- In case of BD18362EFV-M and the LEDs are connected with long wires, it might be triggered the malfunction of LED open protection and LET short detection by ringing in the voltage which is produced by switching on and off of SW between IC channels. Moreover, if the ringing level becomes higher than the case of above, it might damage the IC. Confirm the ringing level with enough evaluation and respond to it by placing RC snubber circuit between CH_n and CH_{n-1}.

I/O Equivalence Circuits

No.	Symbol	Equivalence Circuit	No.	Symbol	Equivalence Circuit
2	CNT		9	SETCLK	
3	HAZ		10	SETDLY	
5	VREG		11	SET	
6 7 8	SEL1 SEL2 SEL3		12 13 14	CMPLT SG FLAG	

I/O Equivalence Circuits - continued

No.	Symbol	Equivalence Circuit
17 18 19 20 21 22 23 24 25 26 27 28	CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8 CP CFP CFM	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

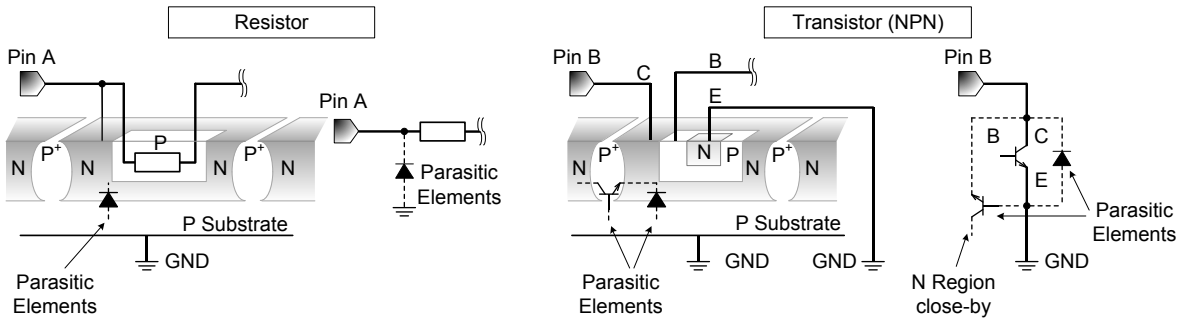


Figure 37. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

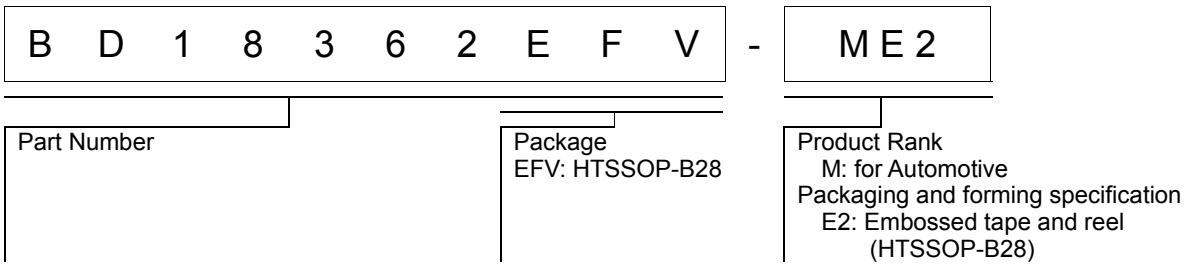
13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

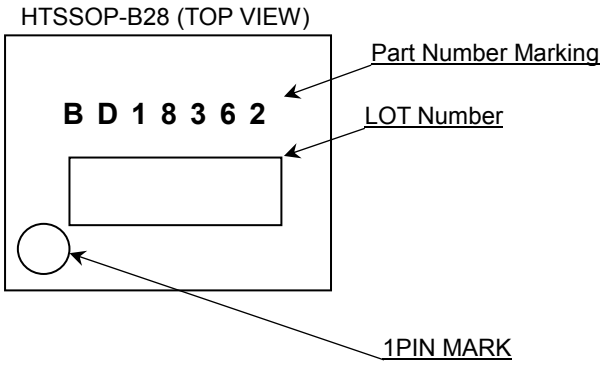
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

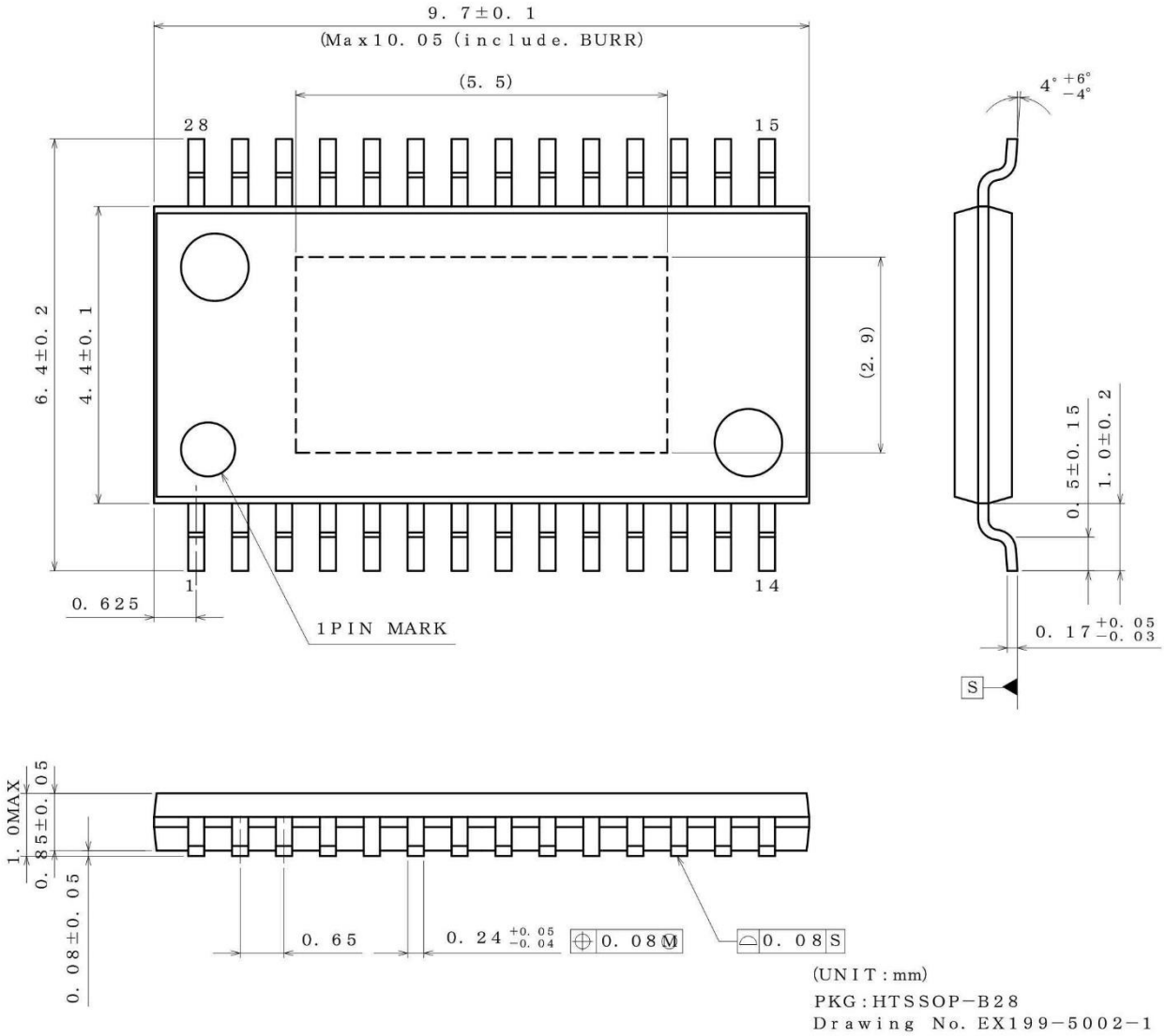


Marking Diagrams



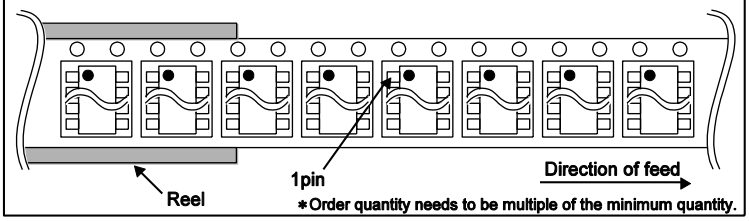
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Rev.	Changes
13.Jun.2017	001	New Release
28.Oct.2020	002	Page 21 Electrical Characteristics SET Pin Output Voltage Delete Page 33 Marking Diagrams D18362 → BD18362

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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