Ultra-Low Jitter, Fixed-Frequency SMD Clock Oscillator

AK5 Series

Request Samples | Check Inventory

ESD Sensitive

5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
MSL Level = 1

Features

- 3rd overtone solution
- Ultra-Low jitter: 75 fs typ RMS (F= 156.25MHz LVPECL)
- Frequency range: 100MHz to 212.5MHz
- Lowest in-class power consumption (16mA typ LVDS)
- ± 20ppm & ± 25ppm stability (-40 to +85ºC) options available (dependent on frequency)
- 3.3V, 2.5V, 1.8V Vdd supply
- LVPECL, LVDS, & HCSL differential output options
- Output enable standard

Applications

- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Common Key Electrical Specifications

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range		100		212.5	MHz	
Standard Available Frequencies		100MHz 122.88MHz 125MHz 148.5MHz 156.25MHz 200MHz 212.5MHz				Contact Abracon for availability of frequencies not listed
Supply Voltage (Vdd) [Note 1]		2.97	3.3	3.63	V	Option "A"
		2.37	2.5	2.62		Option "B"
		1.71	1.8	1.89		Option "C"
Supply Current (Idd)	LVPECL		30	50	mA	@ 200MHz; @ Vdd=3.3V
	LVDS		16	27		@ 200MHz; @ Vdd=3.3V
	HCSL		17	30		@ 200MHz; @ Vdd=3.3V
Operating Temperature Range		-20		+70	°C	Option "D"
		-40		+85		Option "F" or "Q"
Storage Temperature		-55		+150	°C	
Frequency Accuracy (Initial Set-Tolerance) at time of shipment (Pre-Reflow) @ +25°C		-10	< ±5	+10	ppm	Relative to carrier frequency
Frequency Stability over [Note 2, 3] Operating Temperature Range		-15		+15	ppm	Option "D" (-20°C to +70°C)
		-20		+20		Option "Q" (-40°C to +85°C)
		-25		+25		Option "F" (-40°C to +85°C)
Aging over 20 Year Product Life [Note 4]		-15		+15	ppm	

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RoHS/RoHS II Compliant
MSL Level = 1

Common Key Electrical Specifications Cont.

Parameters			Min.	Typ.	Max.	Units	Notes
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life [Notes 4, 5]			-40		+40	ppm	Option "D" (-20°C to +70°C)
			-45		+45		Option "Q" (-40°C to +85°C)
			-50		+50		Option "F" (-40°C to +85°C)
Rise (Tr) / Fall (Tf) Time 20% to 80% Vpeak to peak		LVPECL		0.2	0.4	ns	@ Vdd=3.3V, R_L=50Ω
				0.3	0.6		@ Vdd=2.5V, R_L=50Ω
		LVDS		0.15	0.4		@ Vdd=3.3V, R_L=100Ω
				0.15	0.4		@ Vdd=2.5V, R_L=100Ω
				0.3	0.5		@ Vdd=1.8V, R_L=100Ω
		HCSL		0.3	0.5		@ Vdd=3.3V, R_L=50Ω to GND
				0.3	0.5		@ Vdd=2.5V, R_L=50Ω to GND
				0.3	0.6		@ Vdd=1.8V, R_L=50Ω to GND
Duty Cycle			45		55	%	
Start-up Time [Note 2]				< 2	5.0	ms	
Differential Output High Voltage (V_{OH}) Output Low Voltage (V_{OL})	LVPECL	V_{OH}	Vdd-1.03		Vdd-0.88	V	RL=50Ω to Vdd–2.0V on both outputs
		V_{OL}	Vdd-1.85		Vdd-1.60		
	LVDS	V_{OH}		1.40	1.60		RL=100Ω between both outputs
		V_{OL}	0.90	1.10			
	HCSL	V_{OH}	0.40	0.74	0.85		RL=50Ω to ground on each output
		V_{OL}	-0.15	0.00	0.15		
Output Voltage Swing			0.595	0.750	0.930	V	LVPECL
			0.250	0.350	0.450		LVDS
			0.620	0.700	0.780		HCSL
Output Enable & Disable Control			0.7*(V_{dd})			V	Output Enable or No Connect
					0.3*(V_{dd})		Output Disable (High Impedance)
Output Enable Time				< 1	5.0	ms	
Output Disable Time					0.2	µs	
Output Disable Current Consumption					< 10	µA	OE ≤ 0.3V
RMS Phase Jitter [Note 6, 7, 8] @ +25°C (12kHz-20MHz BW)	**@ 200 MHz**	LVPECL		115	140	fsec	@ Vdd=3.3V
				115	140		@ Vdd=2.5V
		LVDS		125	150		@ Vdd=3.3V
				65	90		@ Vdd=2.5V
		HCSL		120	145		@ Vdd=3.3V
				125	150		@ Vdd=2.5V

Note 1: Supply voltage (Vdd) = 1.8V option not available with LVPECL output
Note 2: Relative to initial measured frequency @ +25°C
Note 3: Option Q only available in select frequencies. Please contact Abracon for availability
Note 4: Relative to post-reflow frequency
Note 5: Includes temperature stability, initial frequency accuracy, load pulling, power supply variation, and 20-year aging

Ultra-Low Jitter, Fixed-Frequency SMD Clock Oscillator

AK5 Series

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5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
MSL Level = 1

Common Key Electrical Specifications Cont.

Parameters			Min.	Typ.	Max.	Units	Notes
RMS Phase Jitter [Note 6, 7, 8] @ +25°C (12kHz-20MHz BW)	**@ 156.25 MHz**	LVPECL		75	100	fsec	@ Vdd=3.3V
				80	105		@ Vdd=2.5V
		LVDS		75	100		@ Vdd=3.3V
				100	125		@ Vdd=2.5V
		HCSL		120	145		@ Vdd=3.3V
				120	145		@ Vdd=2.5V
	@ 148.5 MHz	LVPECL		75	100	fsec	@ Vdd=3.3V
				80	105		@ Vdd=2.5V
		LVDS		125	150		@ Vdd=3.3V
				120	145		@ Vdd=2.5V
		HCSL		115	140		@ Vdd=3.3V
				115	140		@ Vdd=2.5V
	@ 125 MHz	LVPECL		95	120	fsec	@ Vdd=3.3V
				125	150		@ Vdd=2.5V
		LVDS		185	210		@ Vdd=3.3V
				175	300		@ Vdd=2.5V
				145	170		@ Vdd=1.8V
		HCSL		135	160		@ Vdd=3.3V
				125	150		@ Vdd=2.5V
				135	160		@ Vdd=1.8V
	@ 122.88 MHz	LVPECL		105	130	fsec	@ Vdd=3.3V
				115	140		@ Vdd=2.5V
		LVDS		195	220		@ Vdd=3.3V
				180	205		@ Vdd=2.5V
				145	170		@ Vdd=1.8V
		HCSL		125	150		@ Vdd=3.3V
				115	140		@ Vdd=2.5V
				180	205		@ Vdd=1.8V
	@ 100 MHz	LVPECL		185	210	fsec	@ Vdd=3.3V
				160	185		@ Vdd=2.5V
		LVDS		305	330		@ Vdd=3.3V
				300	325		@ Vdd=2.5V
				195	220		@ Vdd=1.8V
		HCSL		170	195		@ Vdd=3.3V
				180	205		@ Vdd=2.5V
				175	200		@ Vdd=1.8V

Note 6: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs
Note 7: Phase jitter measured with Keysight E5052B Signal Source Analyzer
Note 8: Refer to the next section for phase noise test setup and representative phase noise plots

Ultra-Low Jitter, Fixed-Frequency SMD Clock Oscillator

AK5 Series

Request Samples | Check Inventory | ESD Sensitive

5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
MSL Level = 1

Options and Part Identification [Note 10]

AK5 [ ] [ ] [ ] [ ] - [ ] [ ]

(1) Output
P: LVPECL
D: LVDS
H: HCSL

(2): Vdd
A: 3.3V
B: 2.5V
C: 1.8V (*)

(*) Excluding LVPECL

(3): Stability over OTR
D: ±15 ppm over -20°C to +70°C
Q: ±20 ppm over -40°C to +85°C (**)
F: ±25 ppm over -40°C to +85°C

(**) Contact Abracon for availability

(4): OE Function
1: OE Pin 1; Active High
3: OE Pin 2; Active High

(5): Output Frequency in MHz
Please specify the Frequency in units of MHz out to 4-digit accuracy after the decimal. Example: "156.2500"=156.25MHz

(6): Packaging
Blank: Bulk (***)
T2: Tape &Reel 250 units
T: Tape &Reel 1,000 units

(***) MOQ: 25 units

Part Number Example:

AK5PAF1-156.2500
AK5PAF1-156.2500T2
AK5PAF1-156.2500T

Note 10: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal

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AK5 Series

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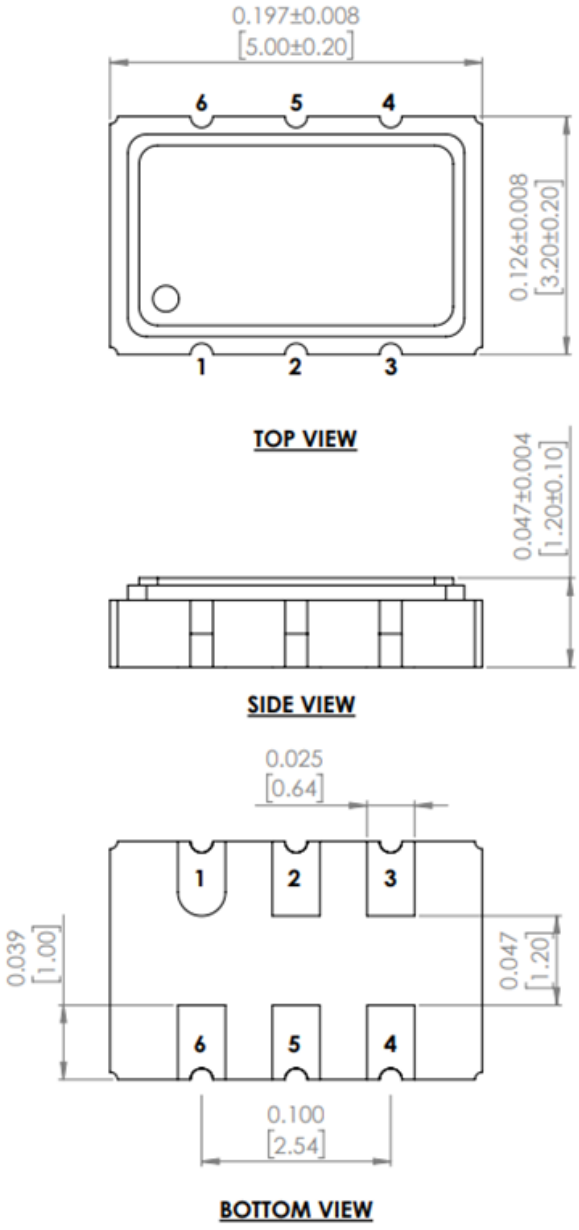
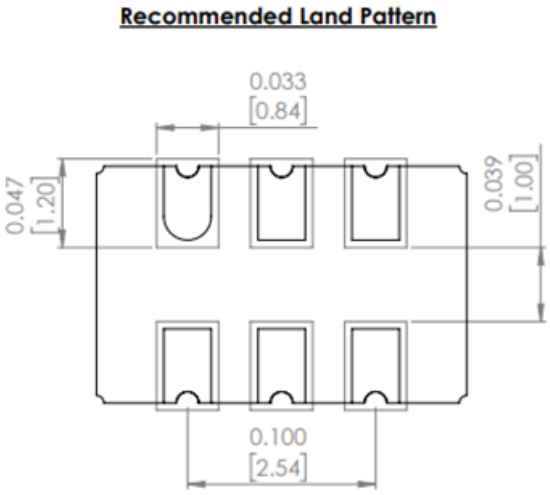
5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
MSL Level = 1

Mechanical Dimensions





Case 1 Pin #1=Output Enable/Disable Function *where* OE is Active HIGH		Case 2 Pin #2=Output Enable/Disable Function *where* OE is Active HIGH	
Pin	**Description**	**Pin**	**Description**
# 1	Output Enable = Logic High, "1", Vdd	# 1	No Connect
	Output Disable = Logic Low, "0", GND	# 2	Output Enable = Logic High, "1", Vdd
# 2	No Connect		Output Enable = Logic Low, "0", GND
# 3	GND	# 3	GND
# 4	Output	# 4	Output
# 5	Complementary output	# 5	Complementary output
# 6	Supply Voltage (Vdd)	# 6	Supply Voltage (Vdd)

Dimensions: inches (mm)

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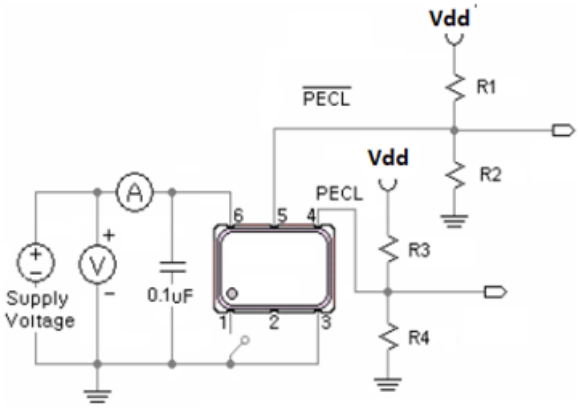
RoHS/RoHS II Compliant
MSL Level = 1

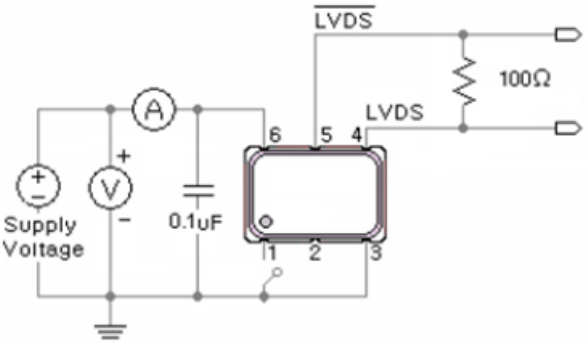
Recommended Test Circuit [Note 11]

LVPECL

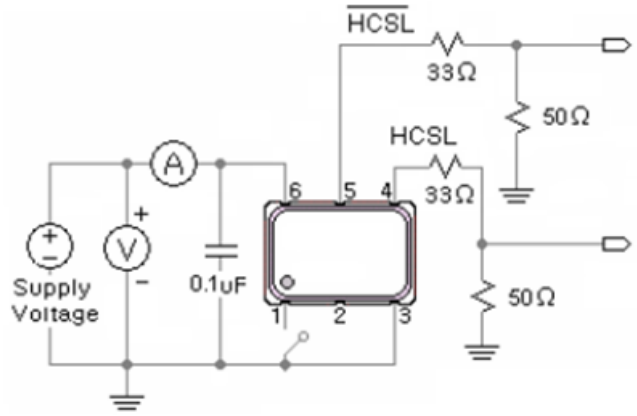


Vdd= 3.3V: R1=R3=127Ω; R2=R4=82.5Ω
Vdd= 2.5V: R1=R3=250Ω; R2=R4=62.5Ω

LVDS



HCSL



Note 11: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.

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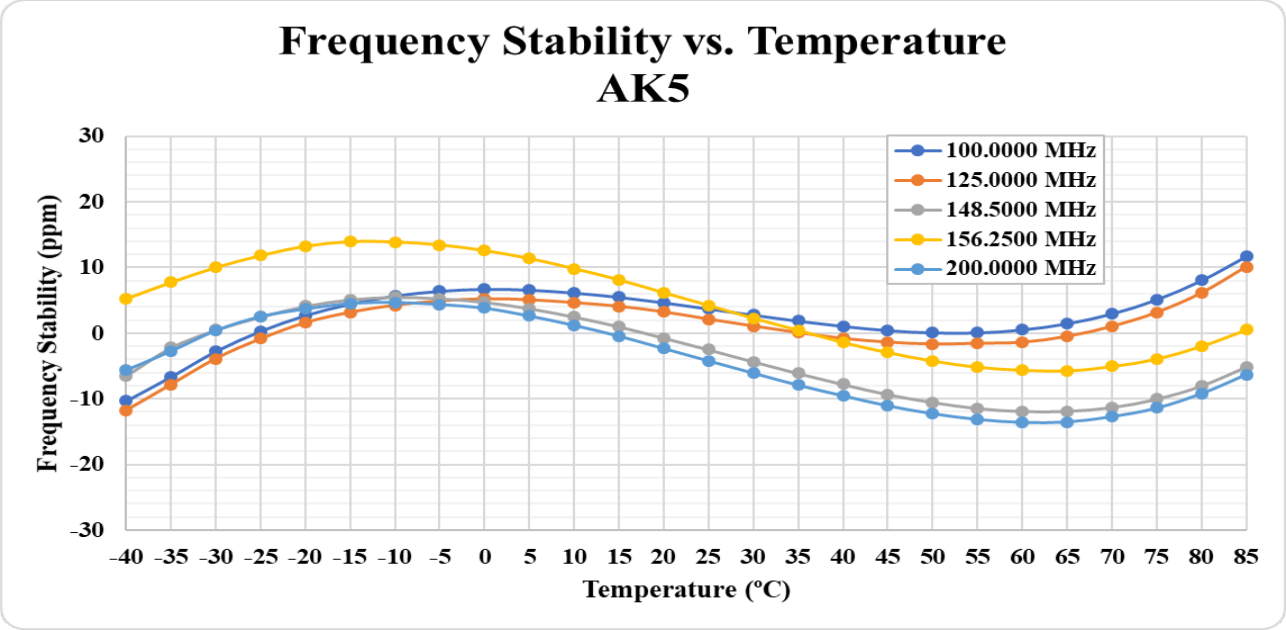
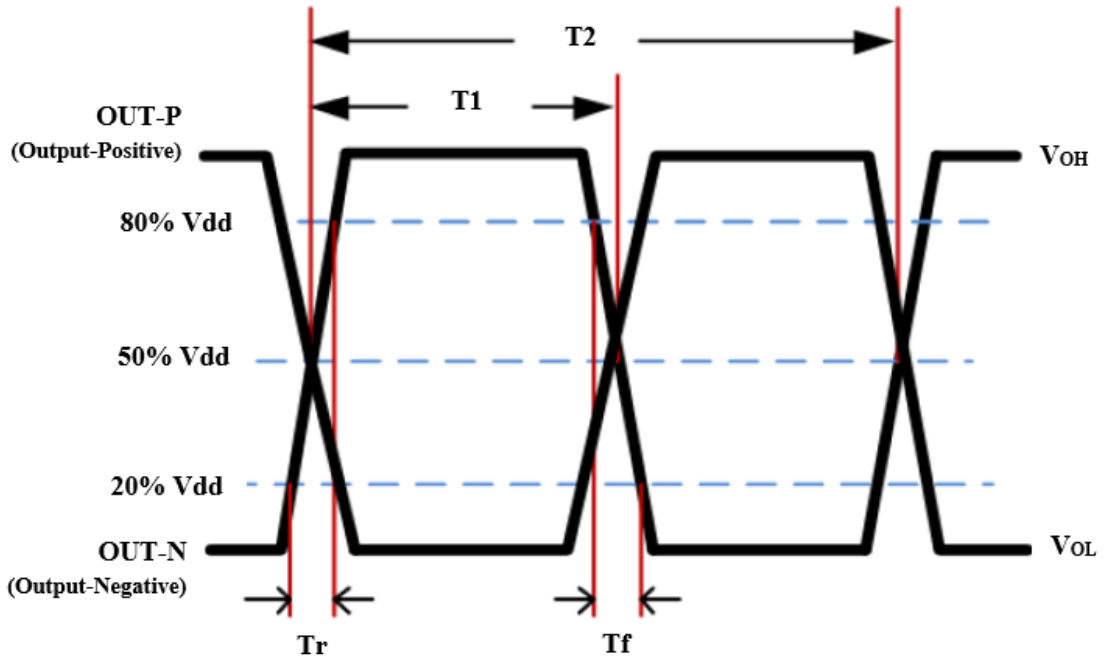
MSL Level = 1

Typical Frequency vs. Temperature Characteristics



Differential Output Wave from



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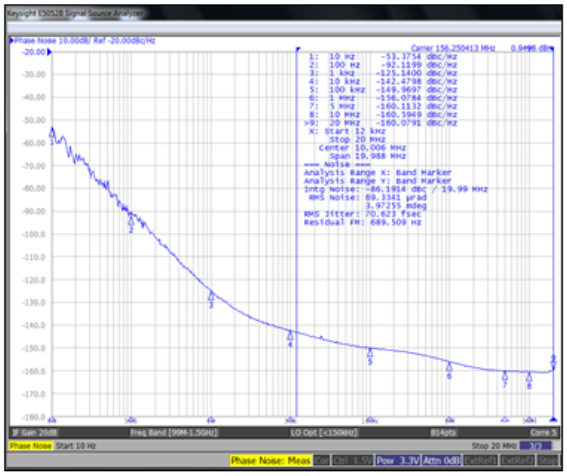
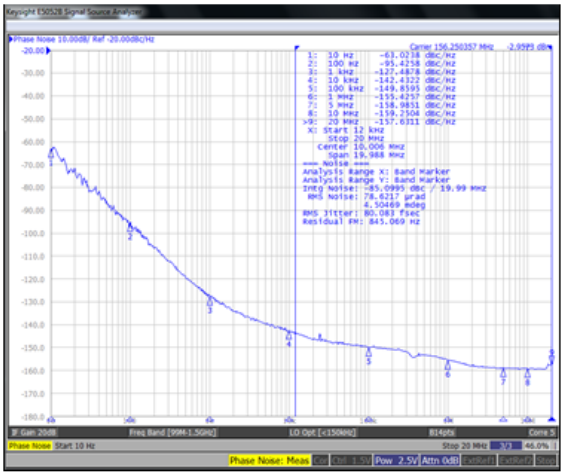
Phase Noise Test Setup [Note 9]

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = Not omitted (Normalized in dBc/Hz)
- Specifed Spur Omission Function = Not enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

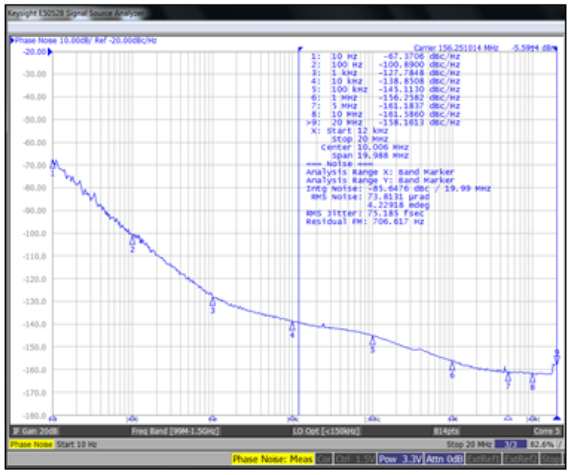
F=156.2500MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 70 fsec



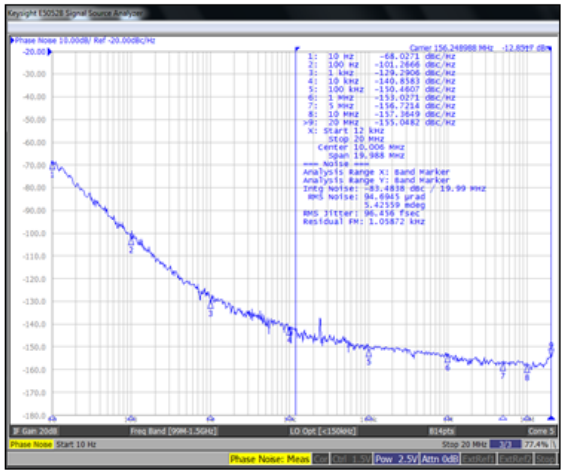
F=156.2500MHz | V_{dd}=2.5V | LVPECL
RMS Phase Jitter = 80 fsec



F=156.2500MHz | V_{dd}=3.3V | LVDS
RMS Phase Jitter = 75 fsec



F=156.2500MHz | V_{dd}=2.5V | LVDS
RMS Phase Jitter = 96 fsec



Note 9: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats

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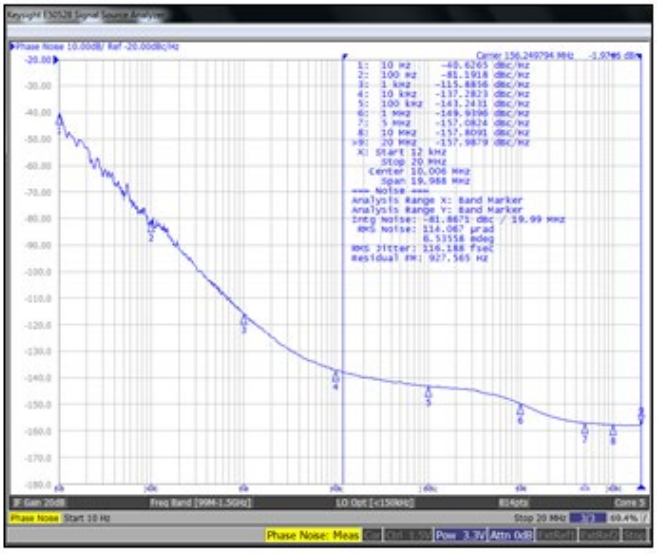
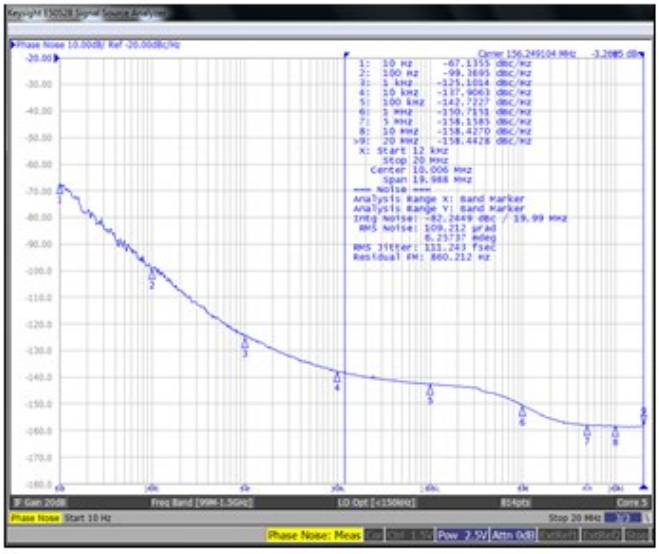
Representative Phase Noise Plots @ +25°C [Note 9]

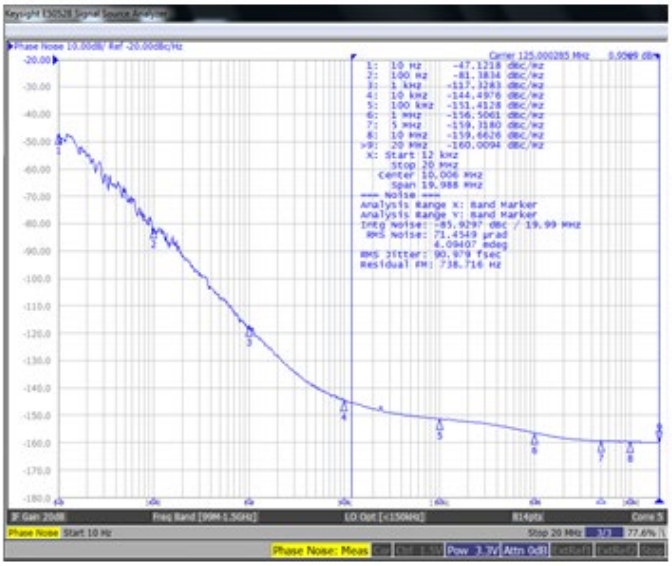
F=156.2500MHz | V_{dd}=3.3V | HCSL
RMS Phase Jitter = 116 fsec



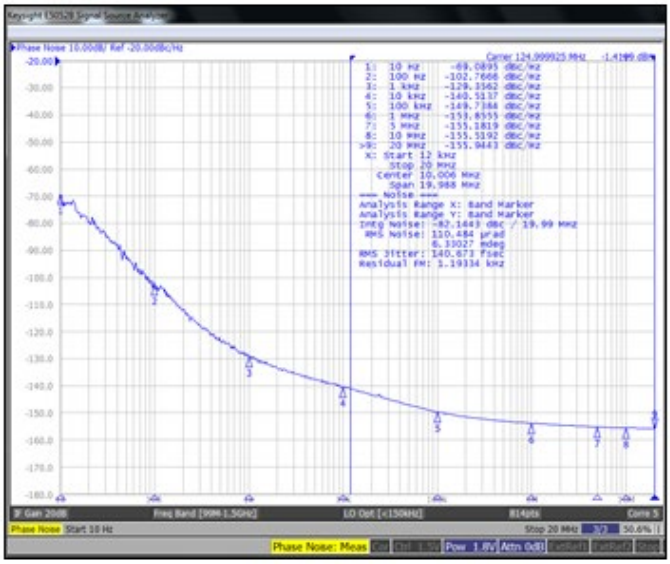
F=156.2500MHz | V_{dd}=2.5V | HCSL
RMS Phase Jitter = 111 fsec



F=125.0000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 90 fsec



F=125.0000MHz | V_{dd}=1.8V | LVDS
RMS Phase Jitter = 140 fsec



Note 9: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats

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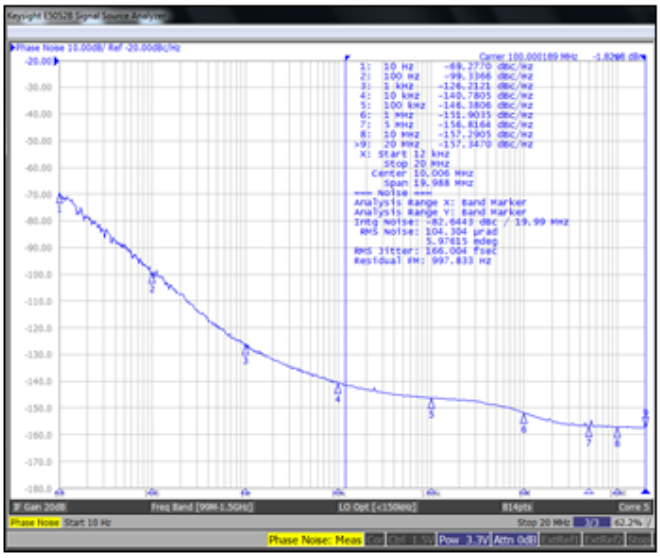
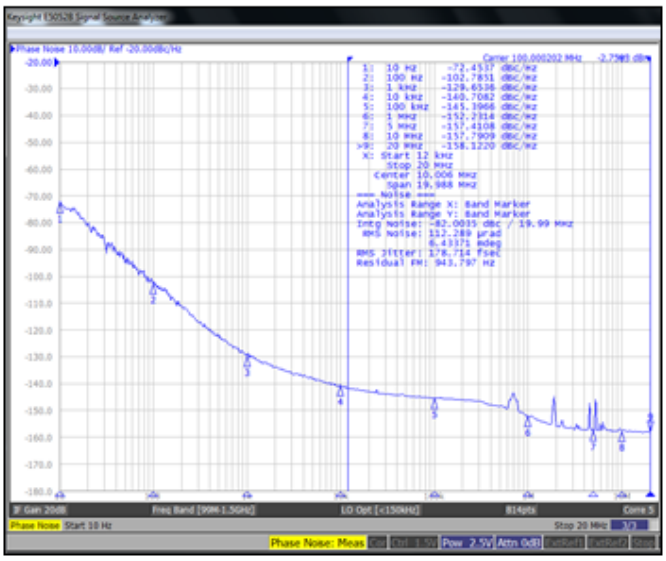
Representative Phase Noise Plots @ +25°C Cont. [Note 9]

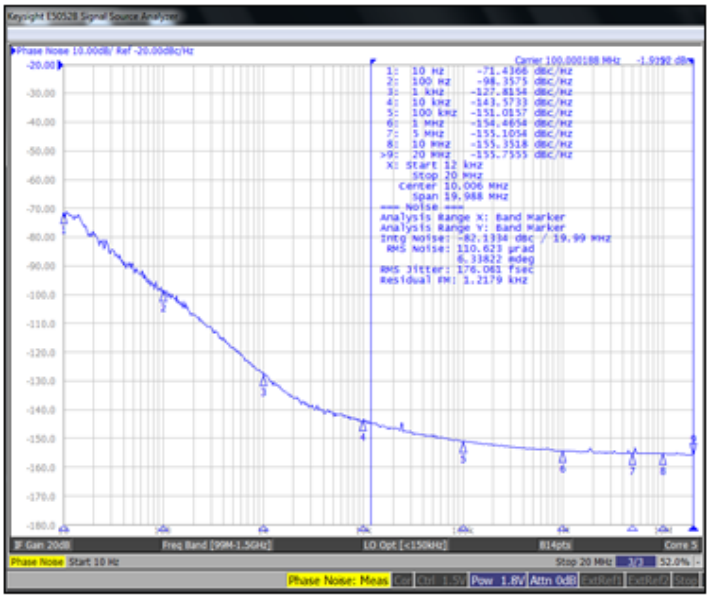
F=100.0000MHz | V_{dd}=3.3V | HCSL
RMS Phase Jitter = 166 fsec



F=100.0000MHz | V_{dd}=2.5V | HCSL
RMS Phase Jitter = 178 fsec



F=100.0000MHz | V_{dd}=1.8V | HCSL
RMS Phase Jitter = 176 fsec



Note 9: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats

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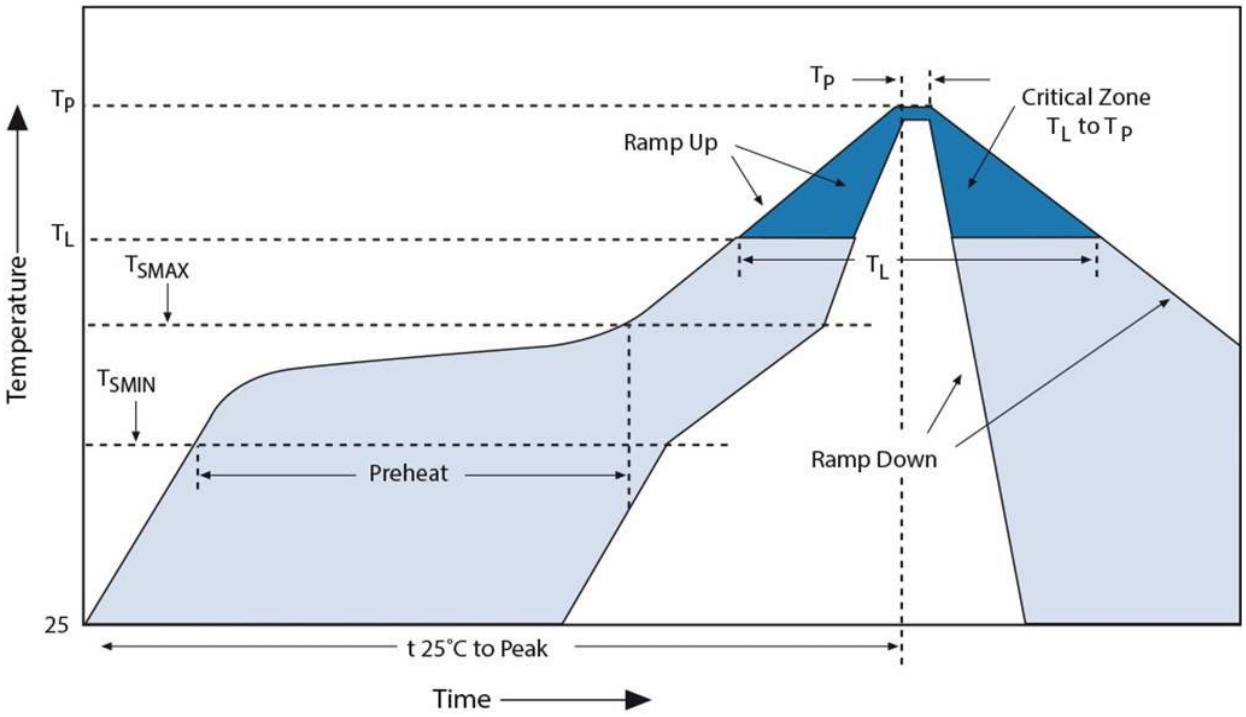
RoHS/RoHS II Compliant
MSL Level = 1

Recommended Reflow Profile [Note 12]



Zone	Description	Temperature	Time
1	Preheat / Soak	T_{SMIN} ~ T_{SMAX} 150°C ~ 200°C	60 ~ 180 sec.
2	Reflow	T_L 217°C	60 ~ 150 sec.
3	Peak heat	T_P 260°C±5°C	20 ~ 40 sec.

Note 12: Can withstand 2 reflows
Note 13: Ramp Up Rate (T_L → T_P) = 3°C / sec. MAX
Note 14: Ramp Down Rate (T_P → T_L) = 6°C / sec. MAX
Note 15: Time 25°C to Peak Temperature (25°C → T_P) = 8 minutes MAX
All temperatures refer to topside of the package, measured on the package body surface

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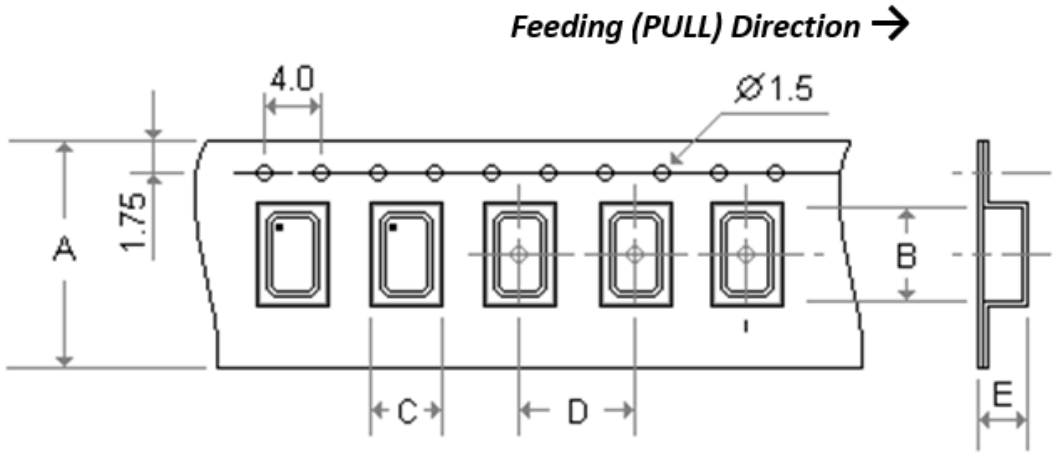
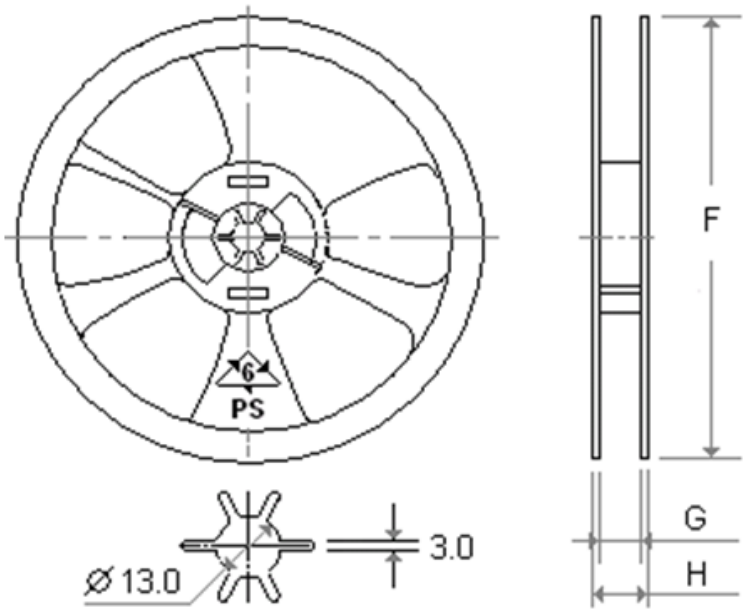
5.0 x 3.2 x 1.3 mm
RoHS/RoHS II Compliant
MSL Level = 1

Packaging

Bulk (MOQ=25 units)
T2 = Tape & Reel 250 units/reel
T= Tape & Reel 1,000 units/reel



Tape Dimensions	
A	12.00
B	5.30
C	3.60
D	8.00
E	1.40
Reel Dimensions	
F	180.00
G	13.00
H	16.00



Dimensions: mm

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