System Reset IC

■FEATURES

- Suitable for replacement from MB3771
- Detection voltage V_{SA}=4.2V±1.0%
- Adjustable detection voltage V_{SB}=1.23V±1.0%
- Possible to detect over voltage V_{SC}=1.245V±1.0%
- V_{SA} and V_{SB} have hysteresis characteristics at reset release
- Operating temperature Ta=-40 to 125°C
- Low quiescent current 280µA typ.
- Reference voltage can be taken out
- Low reset operation voltage 0.8V typ.
- Package EMP8

■GENERAL DESCRIPTION

The NJU2103B is a power supply voltage monitoring IC that instantaneously detects abnormality such as power supply voltage cutoff or drop and generates reset signal.

It can monitor 2 systems of 5 V power supply and arbitrarily set voltage.

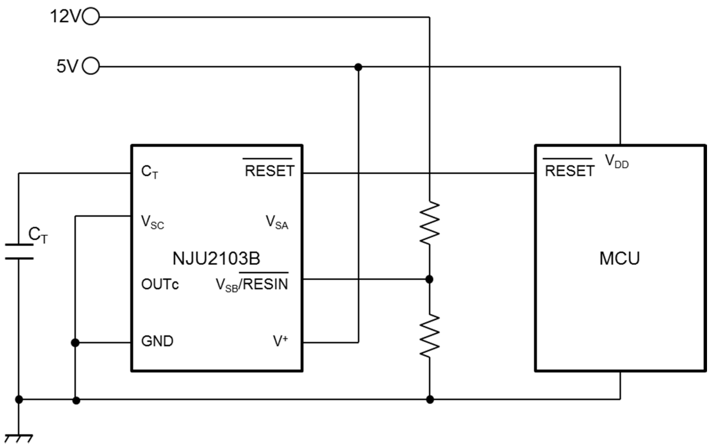
Since V_{SB} Detecting Voltage, V_{SC} Detecting Voltage and $\overline{RESET}$ Output Pulse Width are adjusted from NJU2103A, it is more suitable for replacement from MB3771.

Furthermore, it improves usability by extending operating temperature, and making each parameter highly accurate.

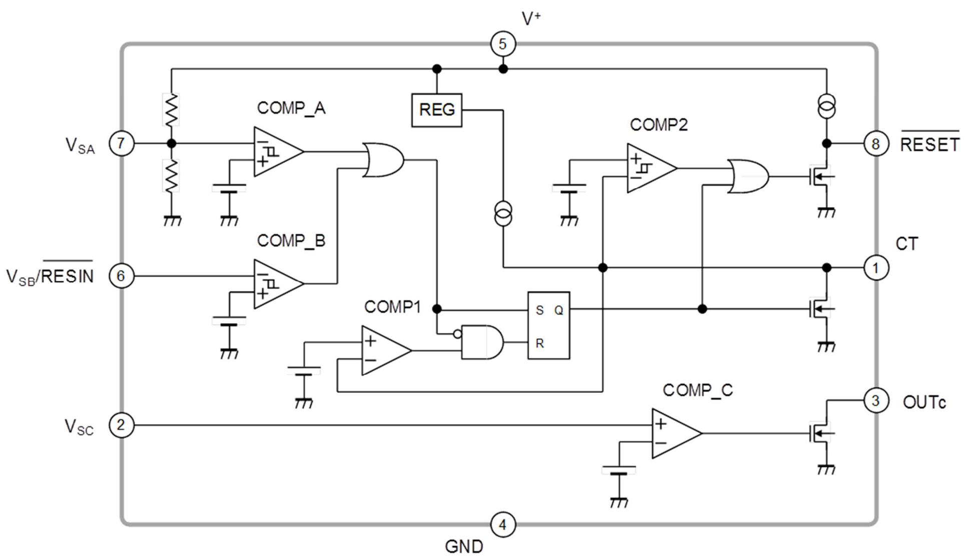
■APPLICATION

- Industrial equipment
- Housing and facility equipment
- OA equipment
- Amusement equipment

■TYPICAL APPLICATION

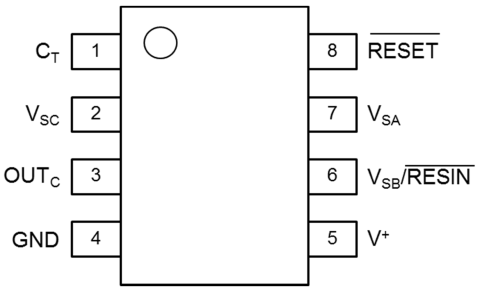


■BLOCK DIAGRAM



■PIN CONFIGURATION

(Top View)



EMP8

PIN No.	PIN NAME	FUNCTION
1	C_T	Connects Capacitor pin for setting $\overline{RESET}$ Output Pulse Width
2	V_{SC}	Comparator C input pin
3	OUT_C	Comparator C output pin
4	GND	GND pin
5	V^+	Power Supply pin
6	$V_{SB}/\overline{RESIN}$	Comparator B input pin
7	V_{SA}	Comparator A input pin
8	$\overline{RESET}$	RESET output pin (Active Low)

■PRODUCT NAME INFORMATION

NJU2103B E (TE1)

- NJU2103B: Device Name
- E: Package E:EMP8
- (TE1): Taping form

■ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	RoHS	Halogen-Free	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU2103BE(TE1)	EMP8	yes	yes	Sn-2Bi	2103B	76	2000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	-0.3 to 20	V
Input Voltage	V_{SA}	-0.3 to V^++0.3 (<20)	V
	V_{SB}	-0.3 to 20	V
	V_{SC}	-0.3 to 20	V
C_T Pin Voltage	V_{CT}	-0.3 to V^++0.3 (<20)	V
$\overline{RESET}$ Output Voltage	$V_{\overline{RESET}}$	-0.3 to V^++0.3 (<20)	V
OUT_C Output Voltage	V_{OUTC}	-0.3 to 20	V
Power Dissipation(Ta=25°C) EMP8	P_D	(2-layer / 4-layer) 700(1)/ 1000(2)	mW
Junction Temperature	T_J	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-50 to +150	°C

(1): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 2 Layers)

(2): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 4 Layers) internal Cu area: 74.2 x 74.2mm

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	2.5 to 18	V
Input Voltage	V_{SA}	0 to V^+	V
	V_{SB}	0 to 18	V
	V_{SC}	0 to 18	V
Output Current	$I_{\overline{RESET}}$	0 to 20	mA
	I_{OUTC}	0 to 6	mA
$\overline{RESET}$ Output Pulse Width	t_{PO}	0.10 to 1000	ms
C_T Capacitor	C_T	0.001 to 10	μF

■ELECTRICAL CHARACTERISTICS

(DC Characteristics) Unless other noted, V^{+}=5V, V_{SB}=0V, V_{SC}=0V, C_T=0.01µF, T_a=25°C

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I_{CC1}	V_{SB}=5V	-	280	390	µA
Operating Current 2	I_{CC2}		-	300	410	µA
V_{SA} Detecting Voltage 1	V_{SAL}	V^{+} sweep down, V_{SB}=V^{+}	4.158	4.200	4.242	V
		V^{+} sweep down, V_{SB}=V^{+}, Ta=-40 °C to 125°C	4.050	-	4.350	
V_{SA} Detecting Voltage 2	V_{SAH}	V^{+} sweep up, V_{SB}=V^{+}	4.210	4.300	4.390	V
		V^{+} sweep up, V_{SB}=V^{+}, Ta=-40 °C to 125°C	4.150	-	4.450	
V_{SA} Hysteresis Width	V_{HRSA}		50	100	150	mV
V_{SB} Detecting Voltage	V_{SBL}	V_{SB} sweep down	1.218	1.230	1.242	V
		V_{SB} sweep down, Ta=-40 °C to 125°C	1.200	-	1.260	
V_{SB} Detecting Supply Voltage Fluctuation	ΔV_{SBL}	V^{+}=2.5 to 18V	-	3	10	mV
V_{SB} Hysteresis Width	V_{HRSB}		14	28	42	mV
V_{SB} Input Current 1	I_{IHB}	V_{SB}=5V	-	0	250	nA
V_{SB} Input Current 2	I_{ILB}		-	0	250	nA
High Level $\overline{RESET}$ Output Voltage	V_{OHR}	$I_{\overline{RESET}}$=-5µA, V_{SB}=5V	4.5	4.9	-	V
$\overline{RESET}$ Output Saturation Voltage 1	V_{OLR1}	$I_{\overline{RESET}}$=3mA	-	0.05	0.40	V
$\overline{RESET}$ Output Saturation Voltage 2	V_{OLR2}	$I_{\overline{RESET}}$=10mA	-	0.15	0.50	V
$\overline{RESET}$ Output Sink Current	$I_{\overline{RESET}}$	V_{OLR}=1V	20	60	-	mA
C_T Charge Current	I_{CT}	V_{SB}=5V, V_{CT}=0.5V	9	12	16	µA
V_{SC} Input Current1	I_{IHC}	V_{SC}=5V	-	0	500	nA
V_{SC} Input Current 2	I_{ILC}		-	0	500	nA
V_{SC} Detecting Voltage	V_{SC}		1.233	1.245	1.257	V
		Ta=-40 °C to 125°C	1.205	-	1.285	
V_{SC} Detecting Supply Voltage Fluctuation	ΔV_{SC}	V^{+}=2.5 to 18V	-	3	10	mV
OUT_C Output Leak Current	I_{OHC}	V_{OHC}=18V	-	0	1	µA
OUT_C Output Saturation Voltage	V_{OLC}	I_{OUTC}=4mA, V_{SC}=5V	-	0.15	0.40	V
OUT_C Output Sink Current	I_{OUTC}	V_{OLC}=1V, V_{SC}=5V	6	20	-	mA
$\overline{RESET}$ Minimum Operating Voltage	V^{+}_{L}	V_{OLR}=0.4V, $I_{\overline{RESET}}$=200µA	-	0.8	1.2	V

■ELECTRICAL CHARACTERISTICS

(AC Characteristics) Unless other noted, V^+=5V, V_{SB}=5V, V_{SC}=0V, C_T=0.01µF, T_a=25°C

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{SA} Input Pulse Width	t_{PIA}		5	-	-	µs
V_{SB} Input Pulse Width	t_{PIB}		5	-	-	µs
$\overline{RESET}$ Output Pulse Width	t_{PO}	$V_{SB}=V^+$	0.5	1.0	1.5	ms
$\overline{RESET}$ Rise Time	t_r	$V_{SB}=V^+$, R_L=2.2kΩ, C_L=100pF $\overline{RESET}$=10% to 90%	-	1.0	1.5	µs
$\overline{RESET}$ Fall Time	t_f	$V_{SB}=V^+$, R_L=2.2kΩ, C_L=100pF $\overline{RESET}$=90% to 10%	-	0.1	0.5	µs
Output Delay Time	t_{PD}	V_{SB} sweep down	-	2	10	µs
	t_{PHL}	V_{SC} sweep up, R_L=2.2kΩ, C_L=100pF	-	0.5	-	µs
	t_{PLH}	V_{SC} sweep down, R_L=2.2kΩ, C_L=100pF	-	1.0	-	µs

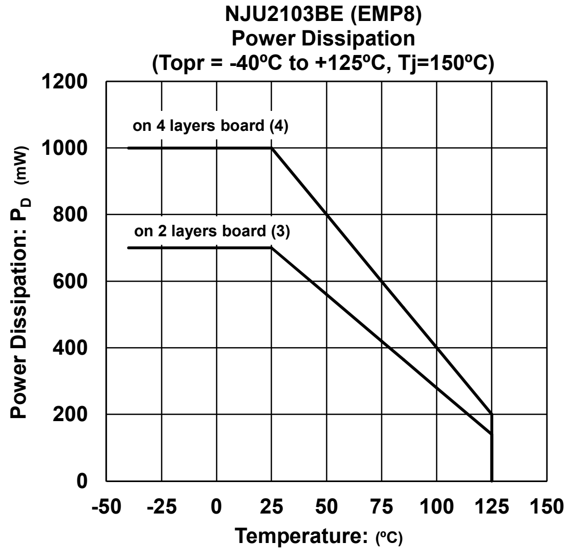
■THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-ambient thermal resistance	θja	EMP8	178(3) 121(4)	°C/W
Junction-to-Top of package characterization parameter	ψjt	EMP8	31(3) 27(4)	°C/W

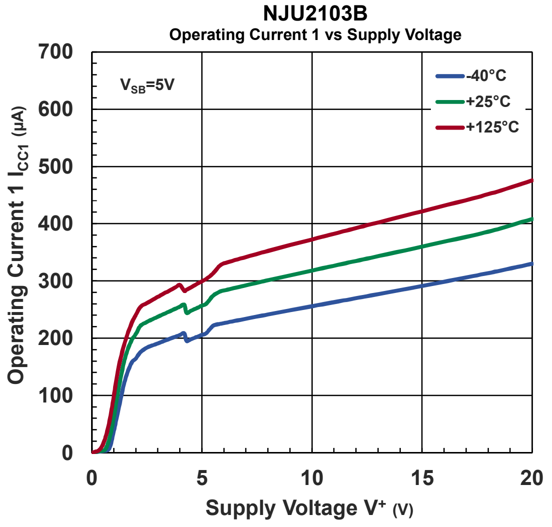
(3): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 2 Layers)

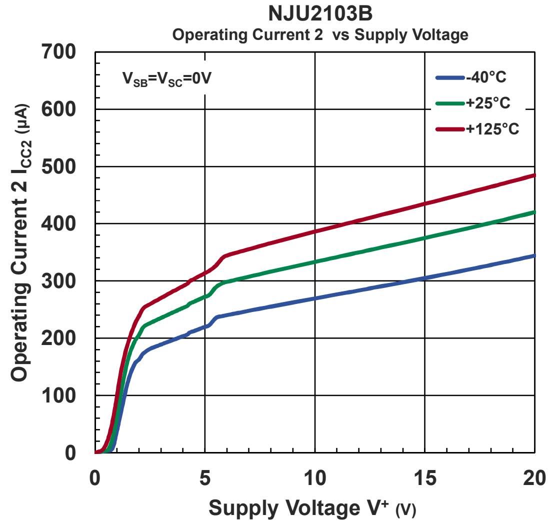
(4): Mounted on glass epoxy board.(76.2 x 114.3 x 1.6 :based on EIA/JEDEC standard, 4 Layers) internal Cu area: 74.2 x 74.2mm

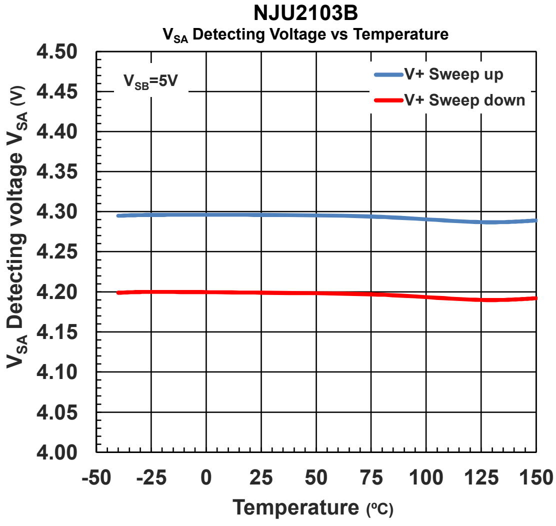
■POWER DISSIPATION vs. AMBIENT TEMPERATURE

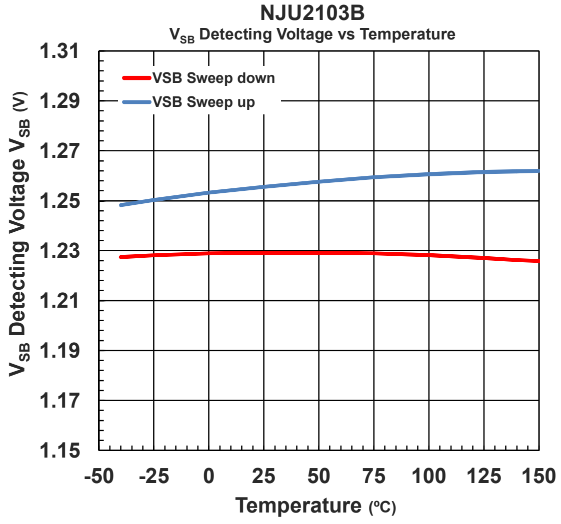


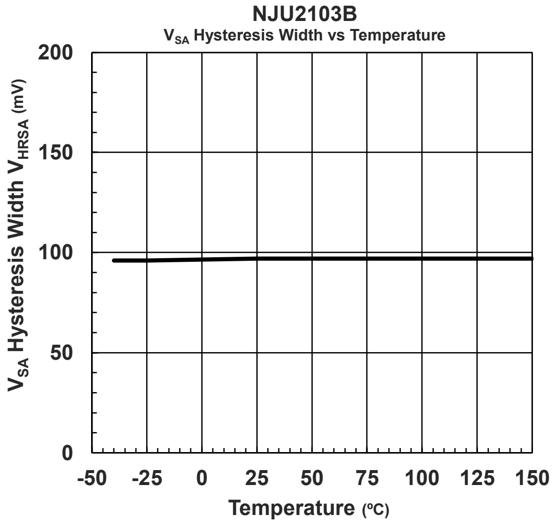
■TYPICAL CHARACTERISTICS

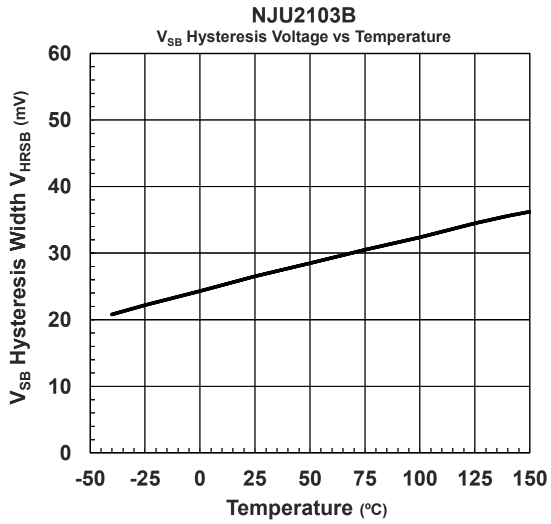


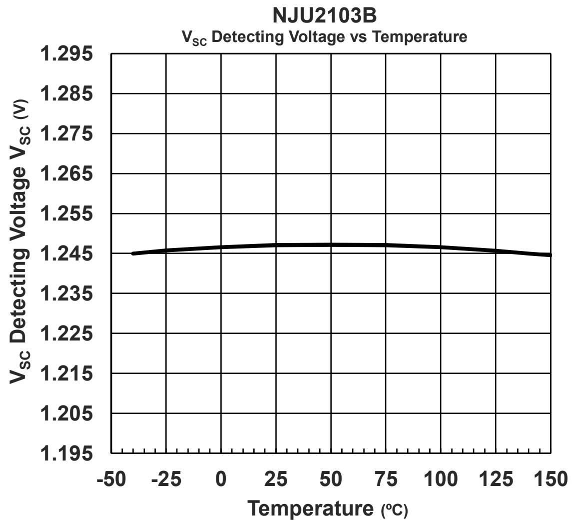


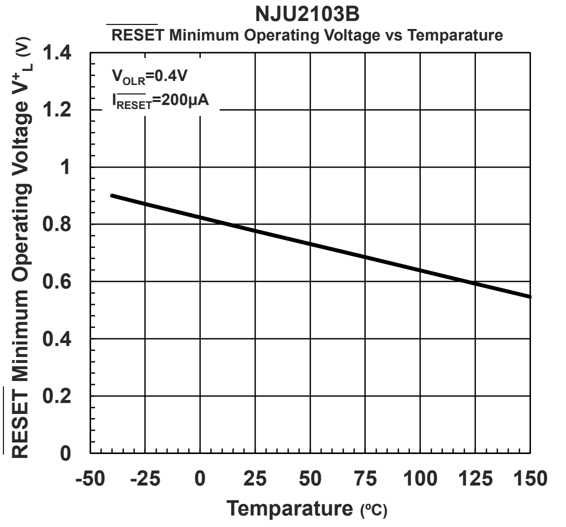


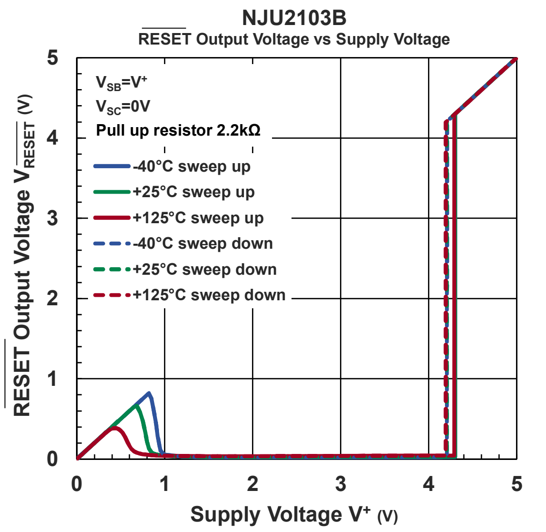


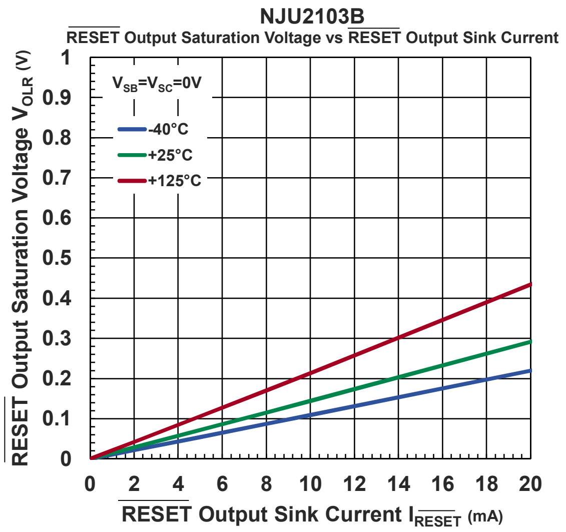


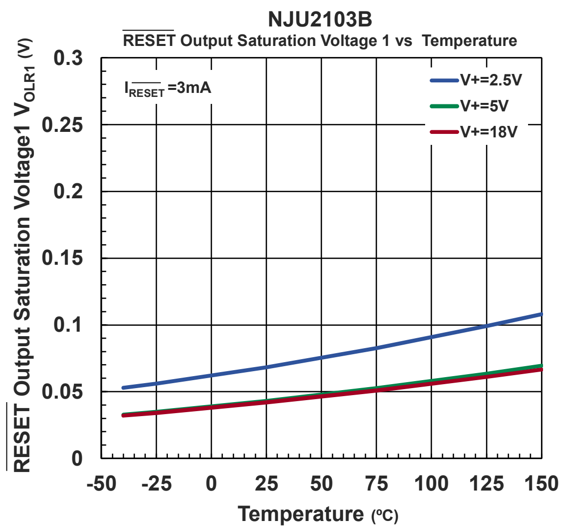


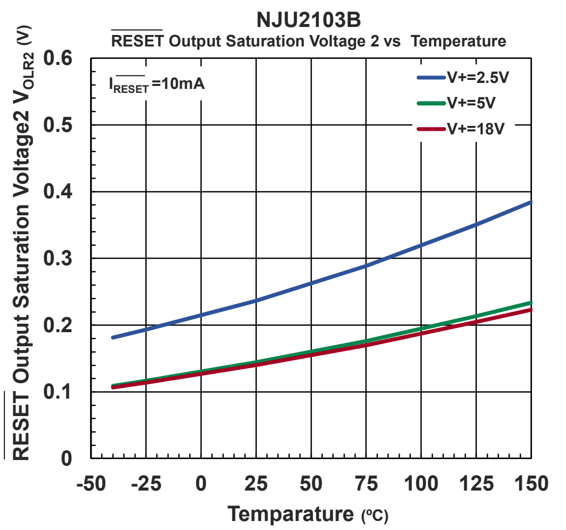

NJU2103B
VSC Detecting Voltage vs Temperature
VSC Detecting Voltage VSC (V)
Temperature (ºC)

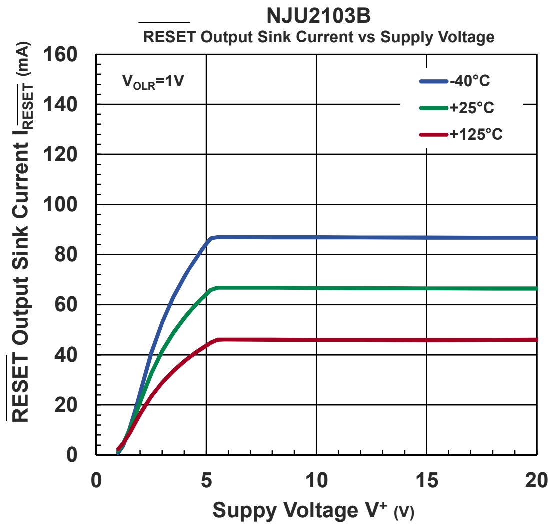

NJU2103B
RESET Minimum Operating Voltage vs Temparature
VOLR=0.4V
IRESET=200μA
RESET Minimum Operating Voltage V+L (V)
Temparature (ºC)

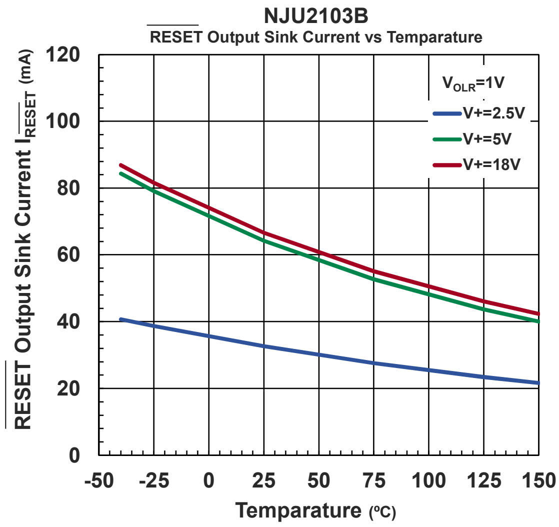

NJU2103B
RESET Output Voltage vs Supply Voltage
VSB=V+
VSC=0V
Pull up resistor 2.2kΩ
-40°C sweep up
+25°C sweep up
+125°C sweep up
-40°C sweep down
+25°C sweep down
+125°C sweep down
RESET Output Voltage VRESET (V)
Supply Voltage V+ (V)

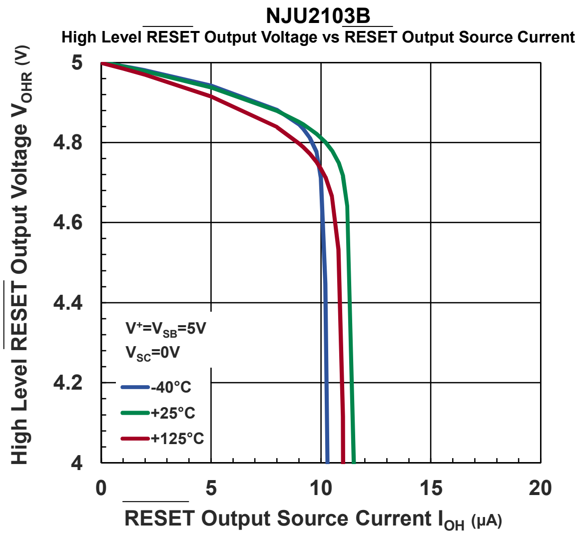

NJU2103B
RESET Output Saturation Voltage vs RESET Output Sink Current
VSB=VSC=0V
-40°C
+25°C
+125°C
RESET Output Saturation Voltage VOLR (V)
RESET Output Sink Current IRESET (mA)

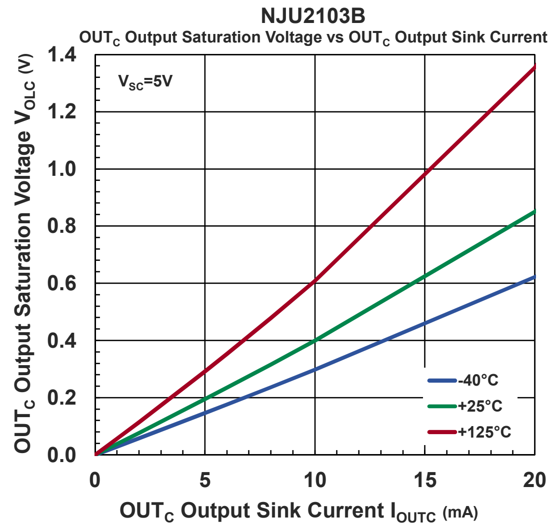

NJU2103B
RESET Output Saturation Voltage 1 vs Temperature
IRESET =3mA
V+=2.5V
V+=5V
V+=18V
RESET Output Saturation Voltage1 VOLR1 (V)
Temperature (ºC)

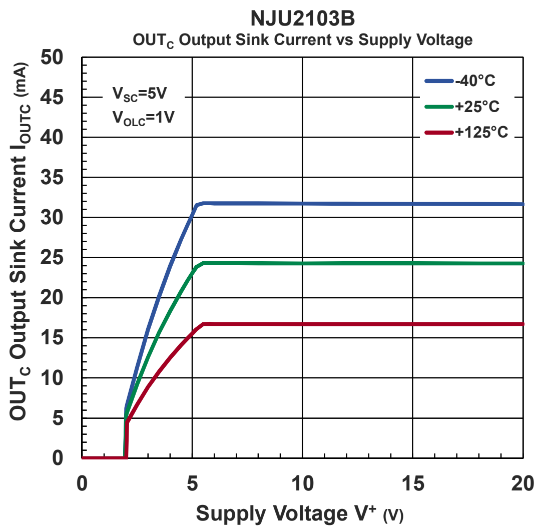

NJU2103B
RESET Output Saturation Voltage 2 vs Temperature
IRESET =10mA
V+=2.5V
V+=5V
V+=18V
RESET Output Saturation Voltage2 VOLR2 (V)
Temparature (ºC)

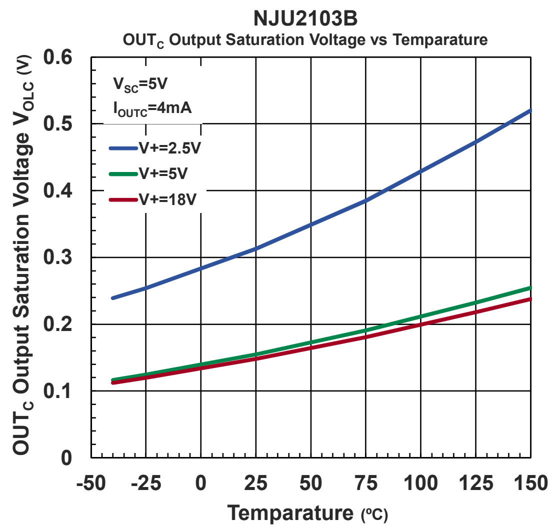

NJU2103B
RESET Output Sink Current vs Supply Voltage
V_OLR=1V
-40°C
+25°C
+125°C
RESET Output Sink Current I_RESET (mA)
0
20
40
60
80
100
120
140
160
0
5
10
15
20
Suppy Voltage V+ (V)

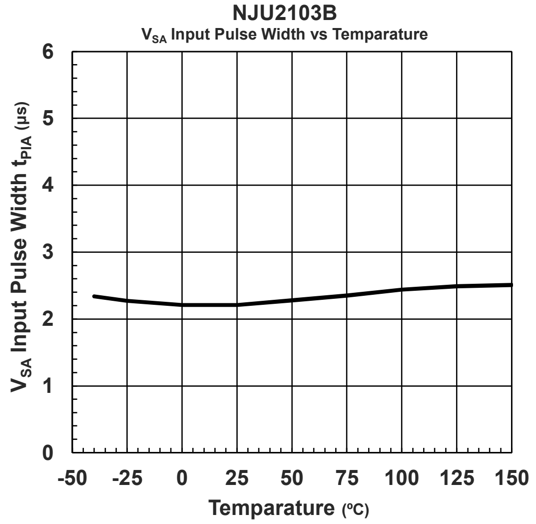

NJU2103B
RESET Output Sink Current vs Temparature
V_OLR=1V
V+=2.5V
V+=5V
V+=18V
RESET Output Sink Current I_RESET (mA)
0
20
40
60
80
100
120
-50
-25
0
25
50
75
100
125
150
Temparature (ºC)

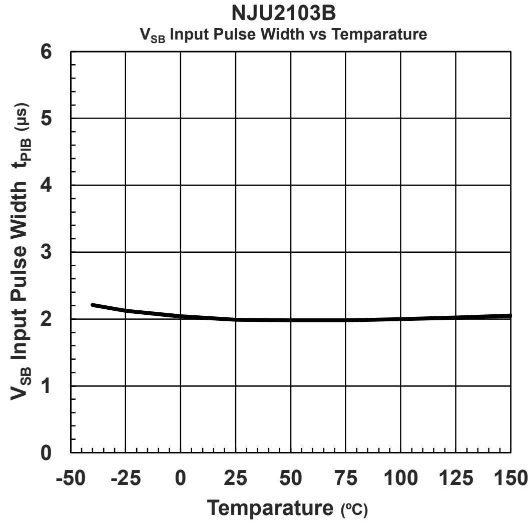

NJU2103B
High Level RESET Output Voltage vs RESET Output Source Current
V+=V_SB=5V
V_SC=0V
-40°C
+25°C
+125°C
High Level RESET Output Voltage V_OHR (V)
4
4.2
4.4
4.6
4.8
5
0
5
10
15
20
RESET Output Source Current I_OH (μA)

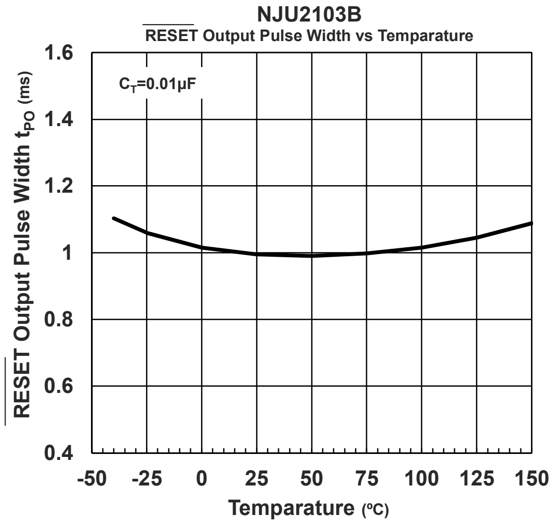

NJU2103B
OUT_C Output Saturation Voltage vs OUT_C Output Sink Current
V_SC=5V
-40°C
+25°C
+125°C
OUT_C Output Saturation Voltage V_OLC (V)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
0
5
10
15
20
OUT_C Output Sink Current I_OUTC (mA)

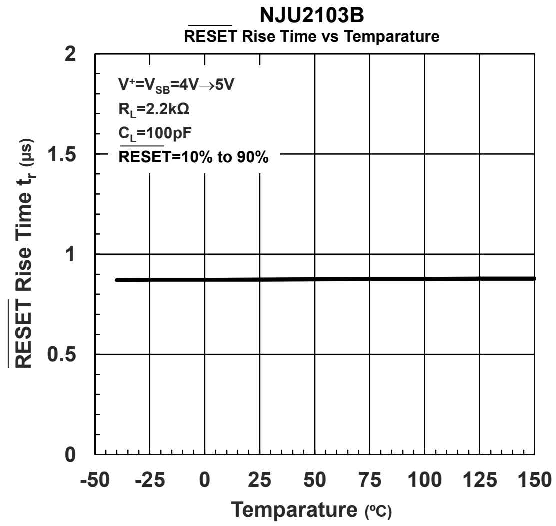

NJU2103B
OUT_C Output Sink Current vs Supply Voltage
V_SC=5V
V_OLC=1V
-40°C
+25°C
+125°C
OUT_C Output Sink Current I_OUTC (mA)
0
5
10
15
20
25
30
35
40
45
50
0
5
10
15
20
Supply Voltage V+ (V)

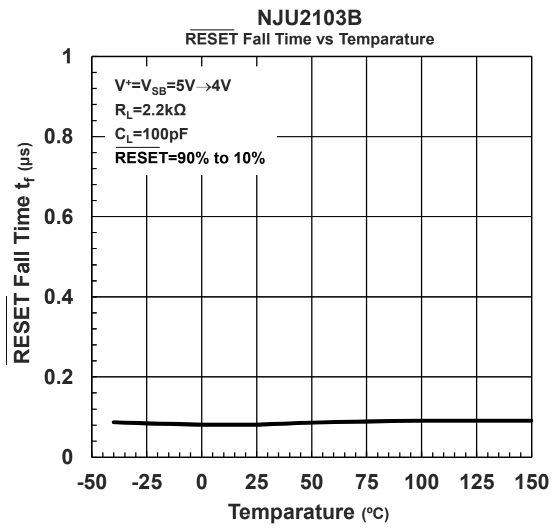

NJU2103B
OUT_C Output Saturation Voltage vs Temparature
V_SC=5V
I_OUTC=4mA
V+=2.5V
V+=5V
V+=18V
OUT_C Output Saturation Voltage V_OLC (V)
0
0.1
0.2
0.3
0.4
0.5
0.6
-50
-25
0
25
50
75
100
125
150
Temparature (ºC)

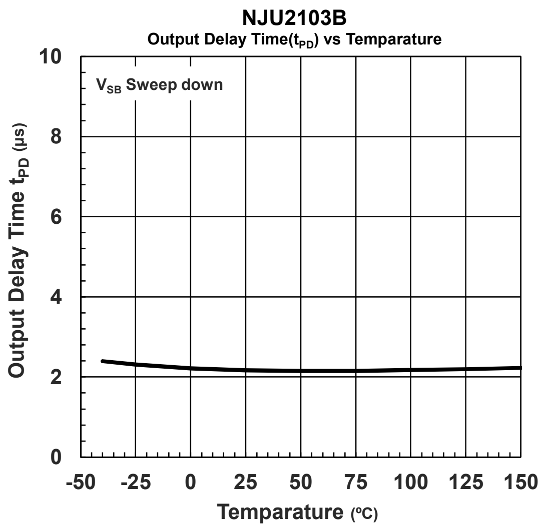

NJU2103B
VSA Input Pulse Width vs Temparature
VSA Input Pulse Width tPIA (μs)
6
5
4
3
2
1
0
-50 -25 0 25 50 75 100 125 150
Temparature (°C)

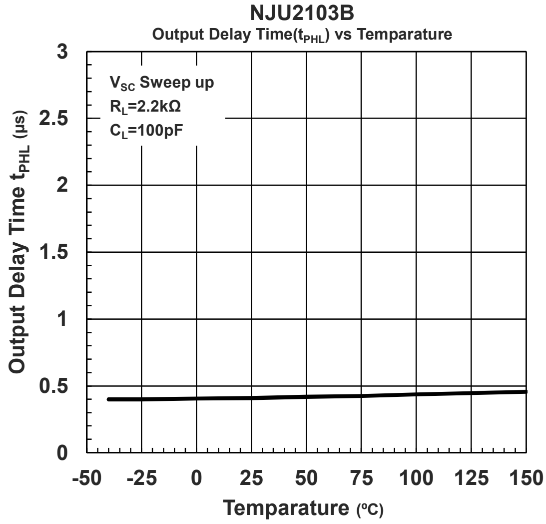

NJU2103B
VSB Input Pulse Width vs Temparature
VSB Input Pulse Width tPIB (μs)
6
5
4
3
2
1
0
-50 -25 0 25 50 75 100 125 150
Temparature (°C)

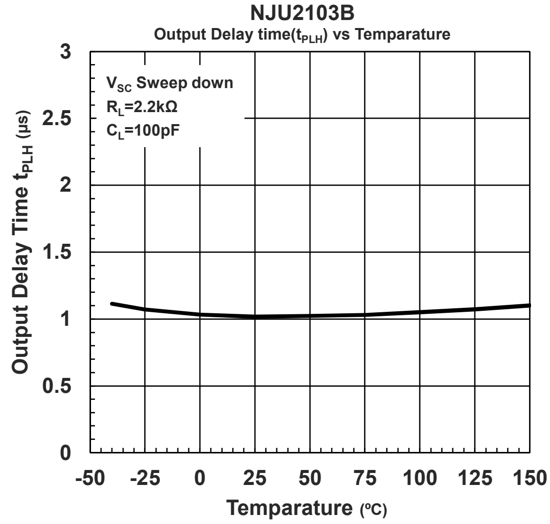

NJU2103B
RESET Output Pulse Width vs Temparature
CT=0.01μF
RESET Output Pulse Width tPO (ms)
1.6
1.4
1.2
1
0.8
0.6
0.4
-50 -25 0 25 50 75 100 125 150
Temparature (°C)

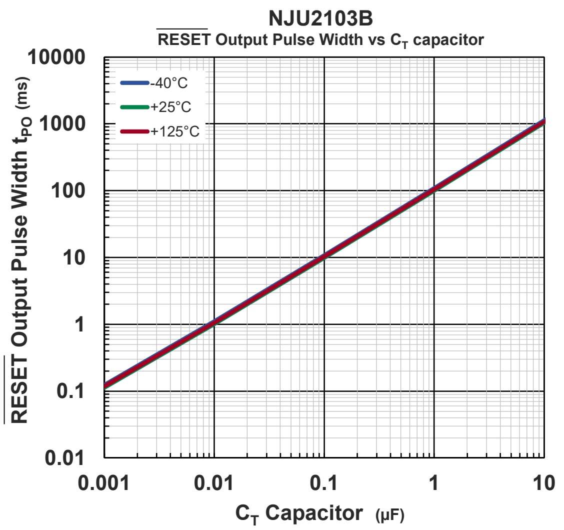

NJU2103B
RESET Rise Time vs Temparature
V+=VSB=4V→5V
RL=2.2kΩ
CL=100pF
RESET=10% to 90%
RESET Rise Time tr (μs)
2
1.5
1
0.5
0
-50 -25 0 25 50 75 100 125 150
Temparature (°C)

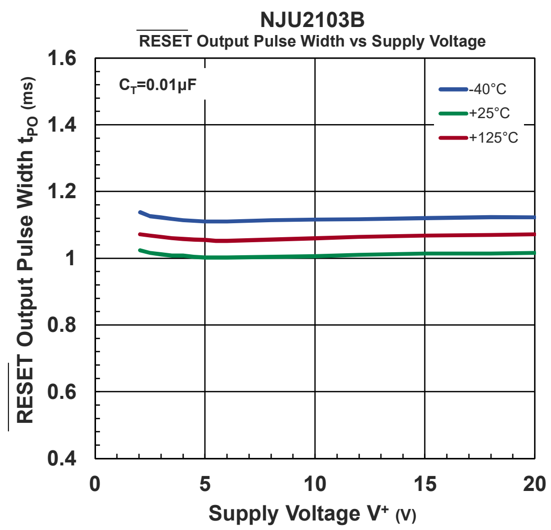

NJU2103B
RESET Fall Time vs Temparature
V+=VSB=5V→4V
RL=2.2kΩ
CL=100pF
RESET=90% to 10%
RESET Fall Time tf (μs)
1
0.8
0.6
0.4
0.2
0
-50 -25 0 25 50 75 100 125 150
Temparature (°C)


NJU2103B
Output Delay Time(tPD) vs Temparature
VSB Sweep down
Output Delay Time tPD (μs)
10
8
6
4
2
0
-50 -25 0 25 50 75 100 125 150
Temparature (°C)


NJU2103B
Output Delay Time(tPHL) vs Temparature
VSC Sweep up
RL=2.2kΩ
CL=100pF
Output Delay Time tPHL (μs)
3
2.5
2
1.5
1
0.5
0
-50
-25
0
25
50
75
100
125
150
Temparature (ºC)


NJU2103B
Output Delay time(tPLH) vs Temparature
VSC Sweep down
RL=2.2kΩ
CL=100pF
Output Delay Time tPLH (μs)
3
2.5
2
1.5
1
0.5
0
-50
-25
0
25
50
75
100
125
150
Temparature (ºC)

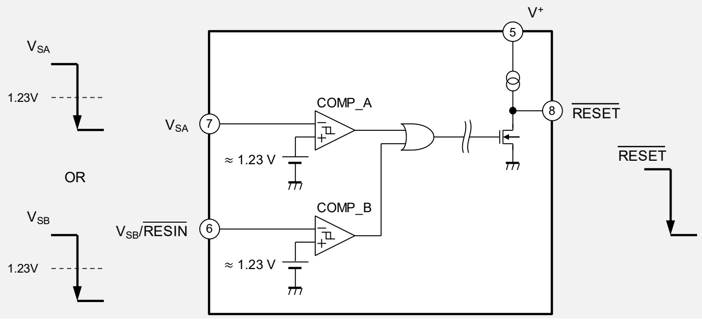

NJU2103B
RESET Output Pulse Width vs CT capacitor
-40°C
+25°C
+125°C
RESET Output Pulse Width tPO (ms)
10000
1000
100
10
1
0.1
0.01
0.001
0.01
0.1
1
10
CT Capacitor (μF)


NJU2103B
RESET Output Pulse Width vs Supply Voltage
CT=0.01μF
-40°C
+25°C
+125°C
RESET Output Pulse Width tPO (ms)
1.6
1.4
1.2
1
0.8
0.6
0.4
0
5
10
15
20
Supply Voltage V+ (V)

■FUNCTION EXPLAMATION

COMP_A and COMP_B are comparator with hysteresis in detection voltage.

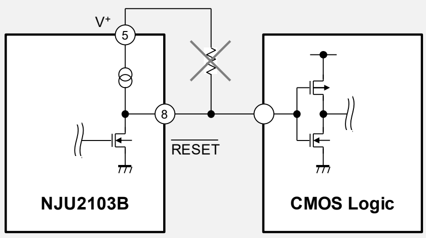
When either V_{SA} or V_{SB} pin voltage becomes about 1.23 V or less, the $\overline{\text{RESET}}$ output becomes " Low ".



COMP_B can be used for arbitrary voltage detection (refer to Fig.3 or Fig.4) and also can be used as a manual reset function with reset hold time by TTL signal input. (refer to Fig.7)

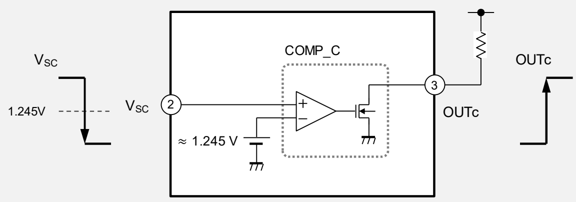
The NJU2103B can detect the instantaneous interruption and the instantaneous drop of the power line with a time of about 2 μs width. If this level of instantaneous interruption or drop is not a problem, it can have a delayed trigger function by connecting capacitor to the V_{SA} and V_{SB} pins (refer to Fig.9).

Since the $\overline{\text{RESET}}$pin is internally pulled up to V^+, an external pull-up resistor isn't required in case of high impedance load like a CMOS logic IC.



COMP_C is an open-drain output comparator without hysteresis which has anti-polarity input and output.

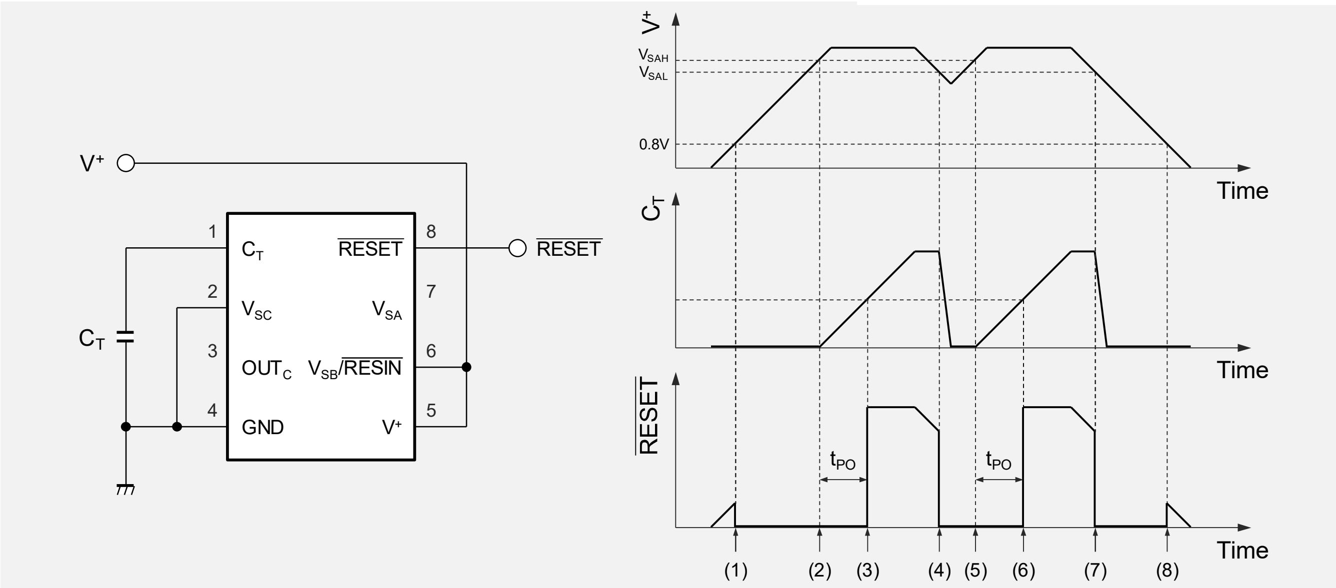
Therefore, it can be used for overvoltage detection (refer to Fig.14), positive logic reset output (refer to Fig.8) and generating a reference voltage source.(refer to Fig.11 to 13)



Unused Pin should be treated as shown in the table below.

Pin. No.	Pin Name	Treatment method of unused Pin
2	V_{SC}	Connect to GND
3	OUT_C	OPEN
6	$V_{SB}/\overline{RESIN}$	Connect to V^+
7	V_{SA}	OPEN
8	$\overline{RESET}$	OPEN

■**OPERATION EXPLAMATION**

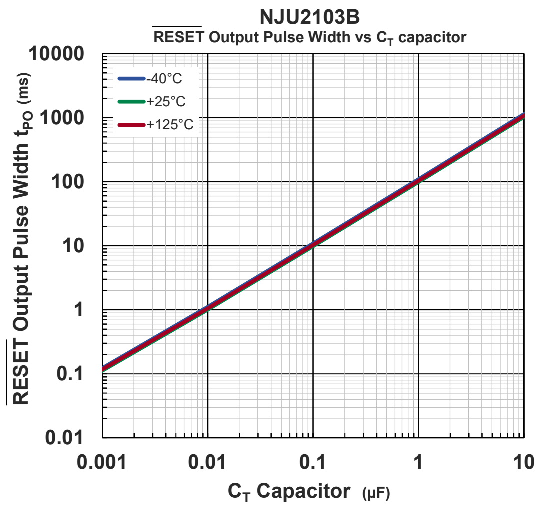


(1) When V^+ increases to about 0.8V, $\overline{\text{RESET}}$ becomes "Low"

(2) When V^+ increases to V_{SAH}, charging to capacitor C_T starts. At this time, $\overline{\text{RESET}}$ holds "Low".

(3) $\overline{\text{RESET}}$ switches from "Low" to "High" after the $\overline{\text{RESET}}$ Output Pulse Width t_{PO}.
Refer to "Output Pulse Width vs C_T capacitor " in TYPICAL CHARACTERISTICS and t_{PO} can be calculated as following formula.

$$\overline{\text{RESET}}\ Output\ Pulse\ Width\ t_{PO}\ [\text{ms}] \approx 100 \times C_T\ [\mu\text{F}]$$



(4) After $\overline{\text{RESET}}$ becomes "High", When V^+ decreases below V_{SAL} , $\overline{\text{RESET}}$ goes "Low" and discharges C_T.

(5) After V^+ decreases below V_{SAL} , it starts charging C_T when V^+ increase to V_{SAH}.
In case of instantaneous V^+ drop, if the time from V^+ decreases below V_{SAL} to increase to V_{SAH} is more than V_{SA} Input Pulse Width t_{PIA}, charging will start after discharging C_T.

(6) V^+ increase to V_{SAH} and .$\overline{\text{RESET}}$ switches from "Low" to "High" after .$\overline{\text{RESET}}$ Output Pulse Width t_{PO}

(7) When V^+ becomes less than V_{SAL}, repeat steps (4) - (6).

(8) When V^+ decreases to 0 V, $\overline{\text{RESET}}$ holds "Low" until V^+ reaches about 0.8 V.

■APPLICATION EXAMPLE

1. 5V Power supply monitor

Monitor the 5V power supply with V_{SA}(COMP_A). The detection voltage at falling is the V_{SA} detection voltage 1 V_{SAL} (4.2 V typ.), and the detection voltage at rising is the V_{SA} detection voltage 2 V_{SAH} (4.3Vtyp.).

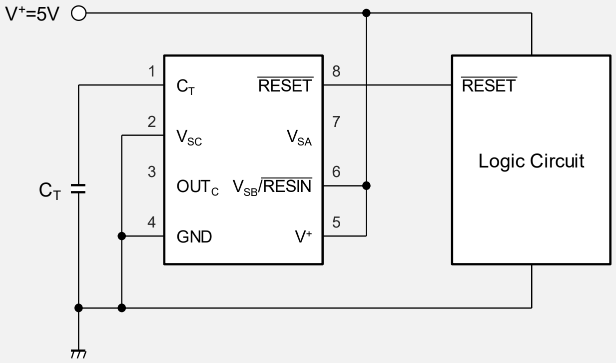


Fig. 1 5V Power supply monitor

2. Power supply monitor (adjust detection voltage by external resistor)

V_{SA} detection voltage1 can be adjusted with an external resistor.

- By selecting the external voltage-dividing resistors R_1 and R_2 to a sufficiently smaller value than internal voltage-dividing resistors R ', R "(99 kΩ, 41 kΩ), the detection voltage can be set by the resistance ratio of R_1 and R_2.

  The formula for calculating detection voltage is as follows and refer to Tab.1 for setting example.

Detection voltage calculate formula (R_1 << 100kΩ, R_2 << 41kΩ)

$$Detection\ Voltage(falling) = \frac{(R_1 \parallel R') + (R_2 \parallel R'')}{R_2 \parallel R''} \times \frac{R''}{R' + R''} \times V_{SAL} \approx \frac{R_1 + R_2}{R_2} \times 1.2300 \quad [\mathrm{V}]$$

$$Detection\ Voltage(rising) = \frac{(R_1 \parallel R') + (R_2 \parallel R'')}{R_2 \parallel R''} \times \frac{R''}{R' + R''} \times V_{SAH} \approx \frac{R_1 + R_2}{R_2} \times 1.2593 \quad [\mathrm{V}]$$

Tab. 1 Setting example

External resistor R_1 [kΩ]	External resistor R_2 [kΩ]	Detection Voltage(falling) [V]	Detection Voltage(rising) [V]
10	3.9	4.37	4.47
9.1	3.9	4.11	4.20

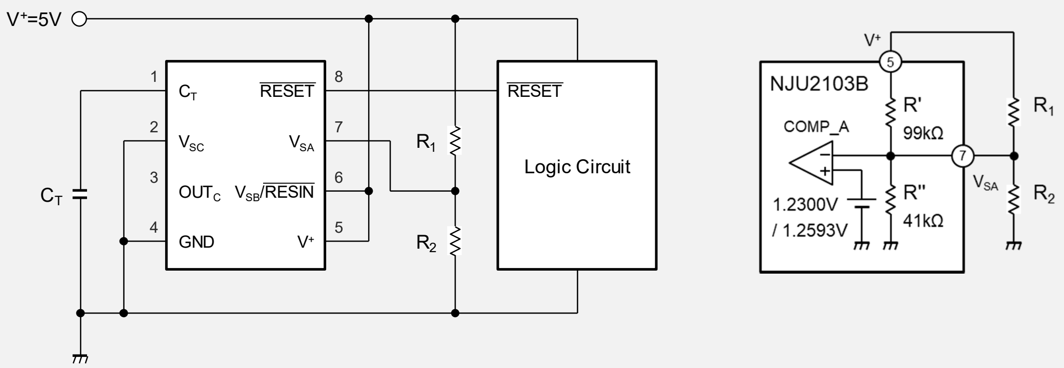


Fig. 2 Power supply monitor (adjust detection voltage by external resistor)

3. Arbitrary power supply monitor (monitoring $V^+ \leq 18V$)

Monitor the power supply of $V^+ \leq 18V$ with V_{SB} (COMP_B) and voltage-dividing resistors R_1 and R_2.

- The detection voltage can be set by resistors R_1 and R_2.

  The formula for calculating R_1 and R_2 is as follows and refer to Tab.2.

$$Detection\ Voltage(falling) = \frac{R_1 + R_2}{R_2} \times V_{SBL} \approx \frac{R_1 + R_2}{R_2} \times 1.230 \quad [V]$$

$$Detection\ Voltage(rising) = \frac{R_1 + R_2}{R_2} \times (V_{SBL} + V_{HRSB}) \approx \frac{R_1 + R_2}{R_2} \times 1.258 \quad [V]$$

- When V^+ is 4.45V or less, connects V_{SA} (pin 7) to V^+ to disable COMP_A
- When V^+ is greater than 4.45 V, V_{SA} (pin 7) should be opened. And in this case, current consumption decreases. (decrease value: $17.2 \times V^+$ [μA])

Tab. 2 setting example

External resistor R_1 [kΩ]	External resistor R_2 [kΩ]	Detection Voltage(falling) [V]	Detection Voltage(rising) [V]
20	7.5	4.51	4.61
39	27	3.01	3.08

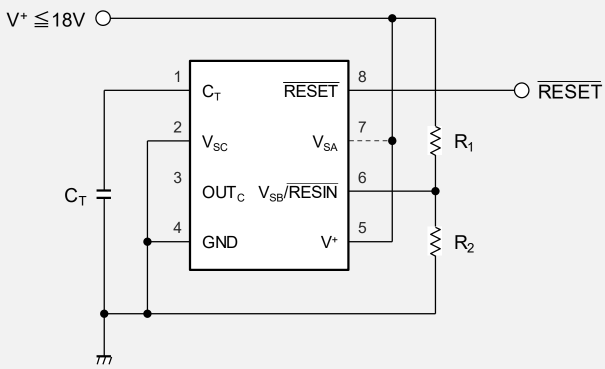


Fig. 3 Arbitrary power supply monitor (monitoring $V^+ \leq 18V$)

4. Arbitrary power supply monitor (monitoring V^+ > 18V)

Monitor the power supply of V^+ > 18V with V_{SB} (COMP_B) and voltage-dividing resistors R_1 and R_2.

The power supply of this IC (about 5V) is generated with V_{SC} (COMP_C) and feedback resistors R_4 and R_5.

- Set the detection voltage with resistors R_1 and R_2 according to the following formula.

Detection voltage calculate formula

$$Detection\ Voltage(V^+\ falling) = \frac{R_1 + R_2}{R_2} \times V_{SBL} \approx \frac{R_1 + R_2}{R_1} \times 1.230 \quad [\mathrm{V}]$$

$$Detection\ Voltage(V^+ rising) = \frac{R_1 + R_2}{R_2} \times (V_{SBL} + V_{HRSB}) \approx \frac{R_1 + R_2}{R_2} \times 1.258 \quad [\mathrm{V}]$$

- The $\overline{\text{RESET}}$ output is ≈ 0V (low level) and ≈ 5V (high level). Not outputs V^+ voltage.

  $\overline{\text{RESET}}$ should not be pulled up to V^+

- If the resistor ratio of R_4 and R_5 is adjusted, high level $\overline{\text{RESET}}$ voltage is changed according to constant voltage set by resistor ratio of R_4 and R_5. Constant voltage V_{OUT} is calculated as the following formula. However, shouldn't be exceed 18V.

$$\text{Constant Voltage } V_{OUT} = \frac{R_4 + R_5}{R_5} \times V_{SC} \approx \frac{R_4 + R_5}{R_5} \times 1.245 \quad [\mathrm{V}]$$

- The constant voltage (5V output) can be used as the power supply for the small current consumption circuit.
- When deciding the value of R_3, it is necessary to be careful about power consumption.

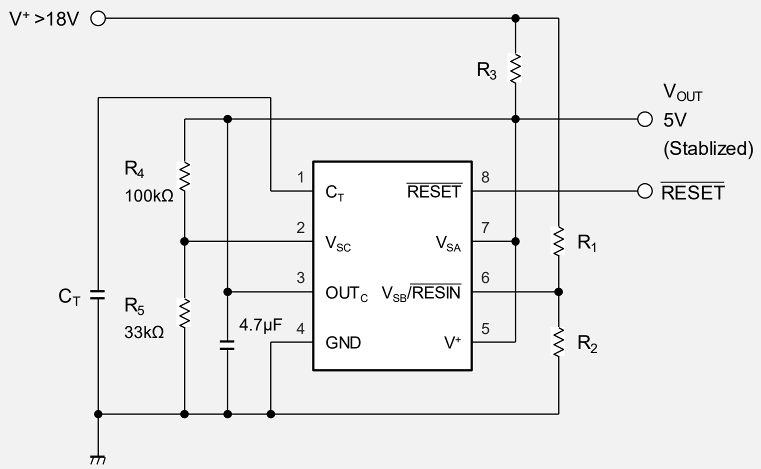


Fig. 4 Arbitrary power supply monitor (monitoring V^+ > 18V)

5. **5V, 12V power supply monitor (dual power supply monitor e.g. V^+_1 = 5V, V^+_2 = 12V)**

Monitor the V^+_1(5V) power supply with V_{SA}(COMP_A) and monitor the V^+_2 (12V) power supply with V_{SB} (COMP_B) and voltage-dividing resistors R_1 and R_2.

- V^+_1 detection voltage (falling) is 4.2V and detection voltage (rising) is 4.3V.
- V^+_2 detection voltage (falling, rising) is set by R_1 and R_2 according to following formula. In case of resistor value in Fig.5, the detection voltage (falling) is about 9.0 V and the detection voltage (rising) is about 9.2 V.

V^+_2 detection voltage calculate formula

$$\text{Detection Voltage}(V_2^+\text{falling}) = \frac{R_1 + R_2}{R_2} \times V_{SBL} \approx \frac{R_1 + R_2}{R_2} \times 1.230 \quad [\text{V}]$$

$$\text{Detection Voltage}(V_2^+\text{rising}) = \frac{R_1 + R_2}{R_2} \times (V_{SBL} + V_{HRSB}) \approx \frac{R_1 + R_2}{R_2} \times 1.258 \quad [\text{V}]$$

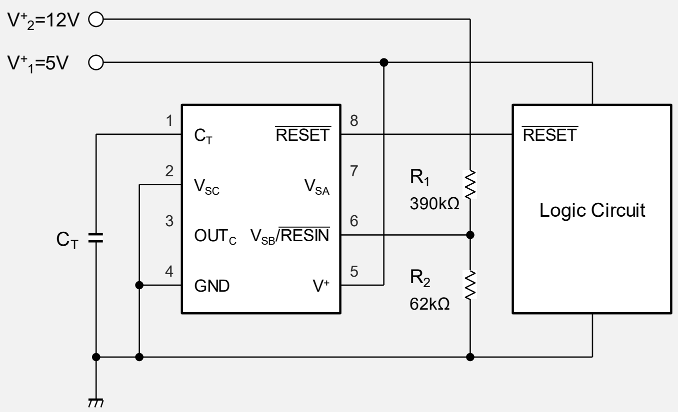


Fig. 5 5V, 12V power supply monitor (dual power supply monitor : V^+_1 = 5V, V^+_2 = 12V)

Technical Information

6. 5V, 12V power supply monitor (e.g. V^+_1 = 5V, V^+_2 = 12V, $\overline{RESET}$ output is only V^+_1 detection result)

Monitor the V^+_1(5V) power supply with V_{SA}(COMP_A) and output signal from $\overline{RESET}$.
In addition, monitor the V^+_2(12V) power supply with V_{SC}(COMP_C) and voltage-dividing resistors R_1, R_2, R_3, R_4, NPN transistor., base current limiting resistor R_5, and output signal from OUT_C.

- V^+_1 detection voltage (falling) is 4.2V and detection voltage (rising) is 4.3V.
- V^+_2 detection voltage (falling) and hysteresis width at rising are calculated as following formula. In case of resistor value in Fig.6, the detection voltage (falling) is about 9.0 V and the hysteresis width at rising is about 0.2 V

V^+_2 detection voltage and hysteresis width at rising calculate formula

$$\text{Detection Voltage}(V_2^+\text{falling}) = \frac{R_1+R_2+R_3}{R_2+R_3}\times V_{SC} \approx \frac{R_1+R_2+R_3}{R_2+R_3}\times 1.245 \quad [\text{V}]$$

$$\text{Hysteresis width at rising} = \frac{R_1(R_3 - R_3 \parallel R_4)}{(R_2+R_3)(R_2+R_3\parallel R_4)}\times V_{SC} \approx \frac{R_1(R_3 - R_3 \parallel R_4)}{(R_2+R_3)(R_2+R_3\parallel R_4)}\times 1.245 \quad [\text{V}]$$

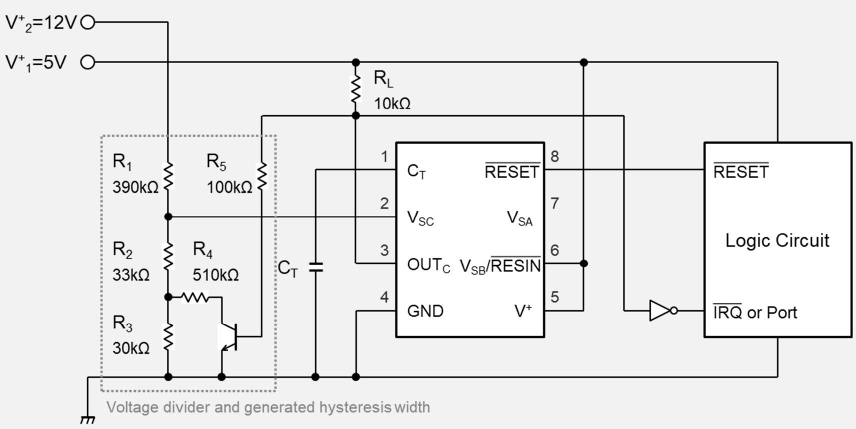


Fig. 6 5V, 12V power supply monitor (V^+_1 = 5V, V^+_2 = 12V, $\overline{RESET}$ output is only V^+_1 detection result)

7. Manual Reset function (V^+ = 5V)

By inputting the TTL signal to $V_{SB}/\overline{RESIN}$, it realizes manual reset output signal regardless of the state of V^+.

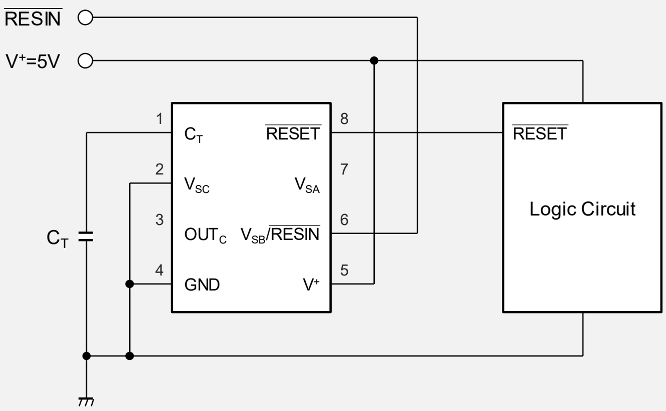


Fig. 7 Manual Reset function (V^+ = 5V)

8. Non-inverting reset output

If a positive output is required for reset signal, invert the $\overline{\text{RESET}}$ output with COMP_C and output from OUT_C.
Since OUT_C is an open drain output, It is required the pull-up resistor.(shown as R_L in Fig.8)

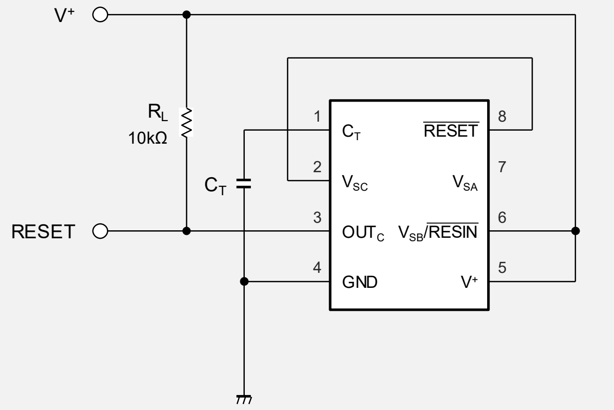


Fig. 8 Non-inverting reset output

9. Power supply voltage monitoring by delayed trigger

An arbitrary delay is added to the COMP_A operation by connecting capacitor C_1 between V_{SA} and GND.

When C_1 is connected minimum input pulse width becomes longer. e.g. t_{PI} = 40μs (C1=1000pF)

Minimum input pulse width t_{PI} is calculated as following formula.

Minimum input pulse width calculate formula

$$t_{PI}\,[\mu s] \approx (R' \parallel R'') \times \ln\left(\frac{5-4}{V_{SAL}-4}\right) \times 10^{-6} \times C_1\,[\text{pF}] \approx 4.7 \times 10^{-2} \times C_1\,[\text{pF}]$$

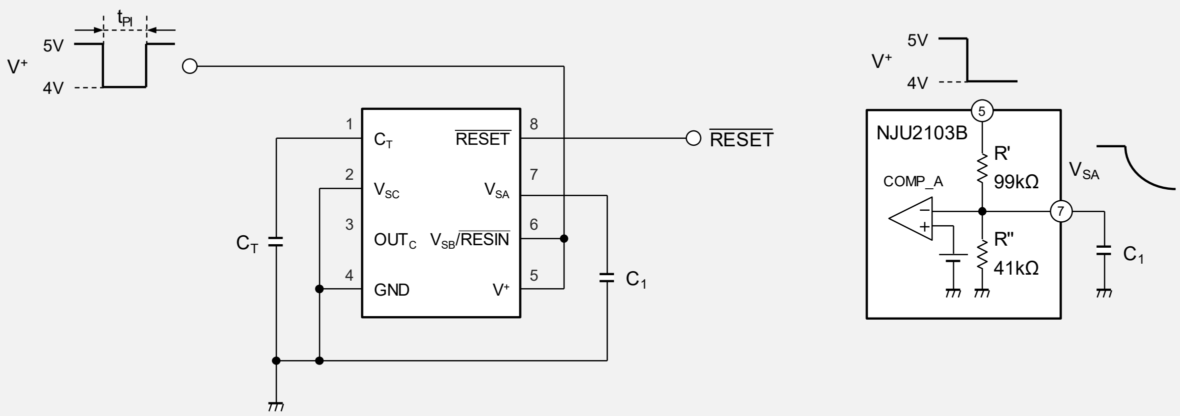


Fig. 9 Power supply voltage monitoring by delayed trigger

10. Positive and negative dual power supply monitoring (e.g. V^+ = 5V、V^-=negative voltage)

Monitor the positive power supply with V_{SA} (COMP_A) and monitor the negative voltage with V_{SB} (COMP_B)

V_{SC} (COMP_C) is used to shift negative voltage to positive voltage.

- R_1、R_2、R_3 should have the same resistance value
- V^+ detection voltage (falling) is 4.2V and detection voltage (rising) is 4.3V.
- V^- detection voltage is calculated as following formula. In case of resistor value in Fig.10, the detection voltage (falling) is about -4.4V and the detection voltage (rising) is about -4.5V.

V^- detection voltage calculate formula

$$\text{Detection voltage } (V^-\text{falling}) = \frac{R_3 + R_4}{R_3} \times V_{SC} - \frac{2R_4}{R_3} \times V_{SBL} \approx \frac{R_3 - R_4}{R_3} \times 1.230 \quad [\text{V}]$$

$$\text{Detection voltage}(V^-\text{rising}) = \frac{R_3 + R_4}{R_3} \times V_{SC} - \frac{2R_4}{R_3} \times (V_{SBL} + V_{HRSB}) \approx \frac{R_3 - R_4}{R_3} \times 1.258 \quad [\text{V}]$$

- When using a power supply that outputs V- without V+ output, it is necessary to connect a Schottky barrier diode (SBD) between the V_{SC} and GND to prevent being applied negative voltage to this IC.

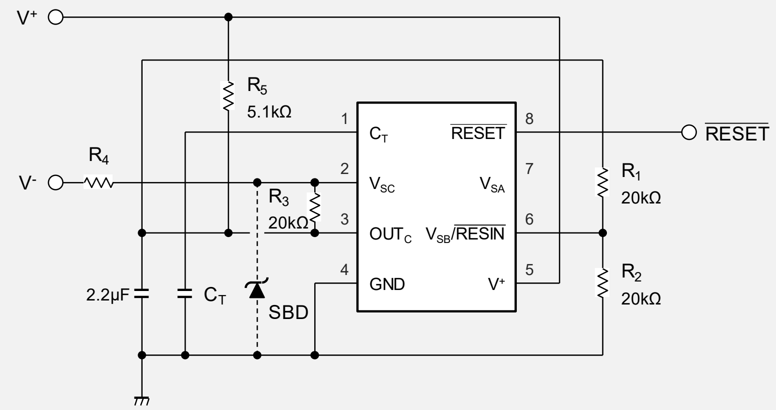


Fig. 10　Positive and negative dual power supply monitoring (V^+ = 5V、V^-=negative voltage)

Technical Information

11. Reference voltage output and voltage drop monitoring (e.g. 9V reference output, 5V, 9V monitoring)

Monitor the V^+(5V) power supply with V_{SA}(COMP_A).

9V Reference voltage V_{OUT} is generated by V_{SC}(COMP_C), feedback resistors R_3, R_4 and NPN transistor, and its 9V is monitored by V_{SB}(COMP_B) and voltage-dividing resistors R_1 and R_2.

- V^+ detection voltage (falling) is 4.2V and detection voltage (rising) is 4.3V.
- The reference voltage V_{OUT} and its detection voltage are calculated as the following formula. In case of resistor value In Fig.11, the reference voltage V_{OUT} is about 9.0V, the detection voltage (V_{OUT} falling) is about 7.2V and the detection voltage (V_{OUT} rising) is about 7.3V

Reference Voltage and detection voltage calculate formula

$$\text{Reference voltage } V_{OUT} = \frac{R_3 + R_4}{R_4} \times V_{SC} \approx \frac{R_3 + R_4}{R_4} \times 1.245 \quad [\text{V}]$$

$$\text{Detection Voltage}(V_{OUT} \text{ falling}) = \frac{R_1 + R_2}{R_2} \times V_{SBL} \approx \frac{R_1 + R_2}{R_2} \times 1.230 \quad [\text{V}]$$

$$\text{Detection Voltage}(V_{OUT} \text{ rising}) = \frac{R_1 + R_2}{R_2} \times (V_{SBL} + V_{HRSB}) \approx \frac{R_1 + R_2}{R_2} \times 1.258 \quad [\text{V}]$$

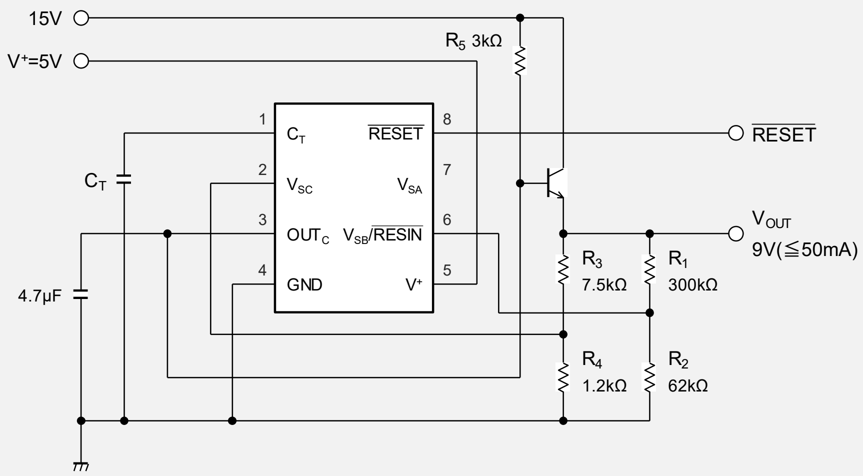


Fig. 11 Reference voltage output and voltage drop monitoring (e.g. 9V reference output, 5V, 9V monitoring)

Technical Information

12-1. Reference Voltage output and Voltage drop monitoring (e.g. 5V output, 5V monitoring)

5V Reference voltage V_{OUT} is generated by V_{SC}(COMP_C), feedback resistors R_3, R_4, NPN transistor and drive resistor R_5, and its 5V is monitored by V_{SA}(COMP_A).

- The reference voltage V_{OUT} is calculated as following formula. In case of resistor value In Fig.12-1, the reference voltage V_{OUT} is about 5.0V

Reference Voltage calculate formula

$$\text{Reference voltage } V_{OUT} = \frac{R_3 + R_4}{R_3} \times V_{SC} \approx \frac{R_3 + R_4}{R_3} \times 1.245 \quad [\text{V}]$$

- The detection voltage (falling) is 4.2V and detection voltage (rising) is 4.3V.

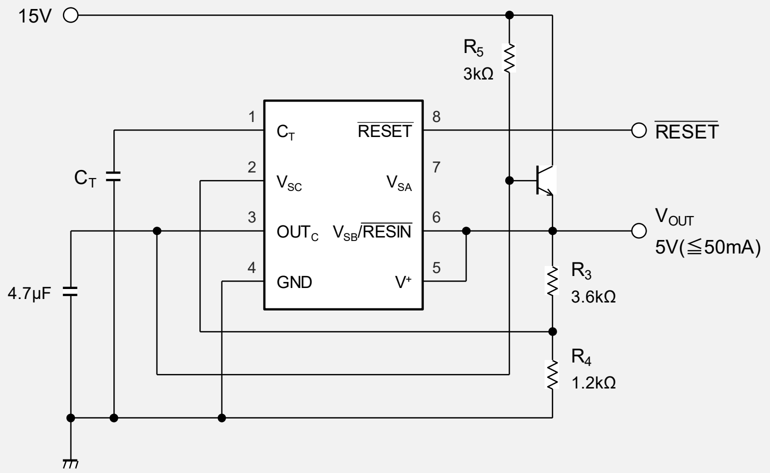


Fig. 12-1 Reference Voltage output and Voltage drop monitoring (e.g. 5V output, 5V monitoring)

12-2. Reference Voltage output and Voltage drop monitoring (e.g. 5V output, 5V monitoring)

5V Reference voltage V_{OUT} is generated by V_{SC}(COMP_C) and feedback resistors R_2, R_3, and its 5V is monitored by V_{SA}(COMP_A). Unlike Fig.12-1, 5V output cannot supply large current.

- The reference voltage V_{OUT} is calculated as following formula.

  In case of resistor value In Fig.12-2, the reference voltage V_{OUT} is about 5.0V

$$\text{Reference voltage } V_{OUT} = \frac{R_2 + R_3}{R_3} \times V_{SC} \approx \frac{R_2 + R_3}{R_3} \times 1.245 \quad [\text{V}]$$

- The detection voltage (falling) is 4.2V and detection voltage (rising) is 4.3V.
- R_1 value should be calculated from current consumption of NJU2103B, the current flowing through R_2 and R_3, and 5V output current. .

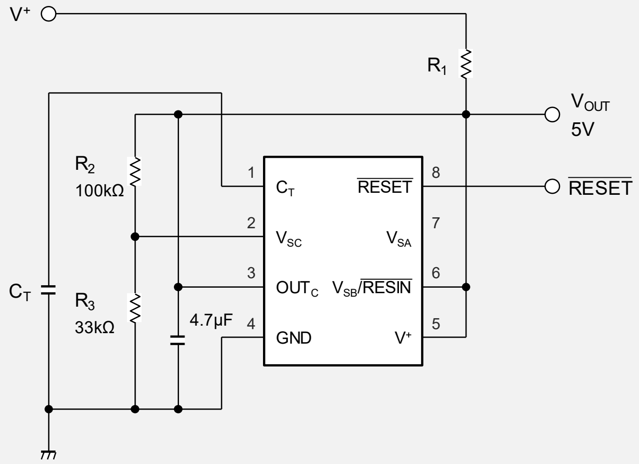


Fig. 12-2 Reference Voltage output and Voltage drop monitoring (e.g. 5V output, 5V monitoring)

13. Reference Voltage output and Voltage drop monitoring (e.g. 1.245V output, 5V monitoring)

Buffer-connect the V_{SC}(COMP_C) and output the reference voltage of COMP_C.
The output current of the reference voltage output is limited by R_1. If R_1 is 1.2 kΩ, it can output about 2 mA

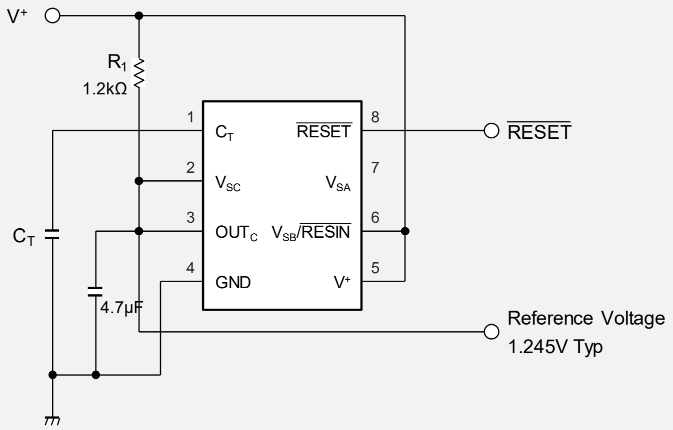


Fig. 13 Reference Voltage output and Voltage drop monitoring (e.g. 1.245V output, 5V monitoring)

14. Low voltage and over voltage detection ($V^+ = 5V$)

V_{SB} (COMP_B) for low voltage detection and V_{SC} (COMP_C) for overvoltage detection.

Logically synthesizes low voltage and over voltage detection by connecting OUT_C to V_{SA}, and output from $\overline{RESET}$.

- Low voltage detection and over voltage detection are calculated as following formula.

$$\text{Low voltage detection (falling) } V_{SL1} = \frac{R_1 + R_2}{R_2} \times V_{SBL} \approx \frac{R_1 + R_2}{R_2} \times 1.230 \quad [V]$$

$$\text{Low voltage detection (rising) } V_{SL2} = \frac{R_1 + R_2}{R_2} \times (V_{SBL} + V_{HRSB}) \approx \frac{R_1 + R_2}{R_2} \times 1.258 \quad [V]$$

$$\text{Over voltage detection } V_{SH} = \frac{R_3 + R_4}{R_4} \times V_{SC} \approx \frac{R_3 + R_4}{R_4} \times 1.245 \quad [V]$$

- There is no hysteresis characteristic for over voltage detection.
- "$\overline{RESET}$Output Pulse Width t_{PO}" is valid even when overvoltage is detected

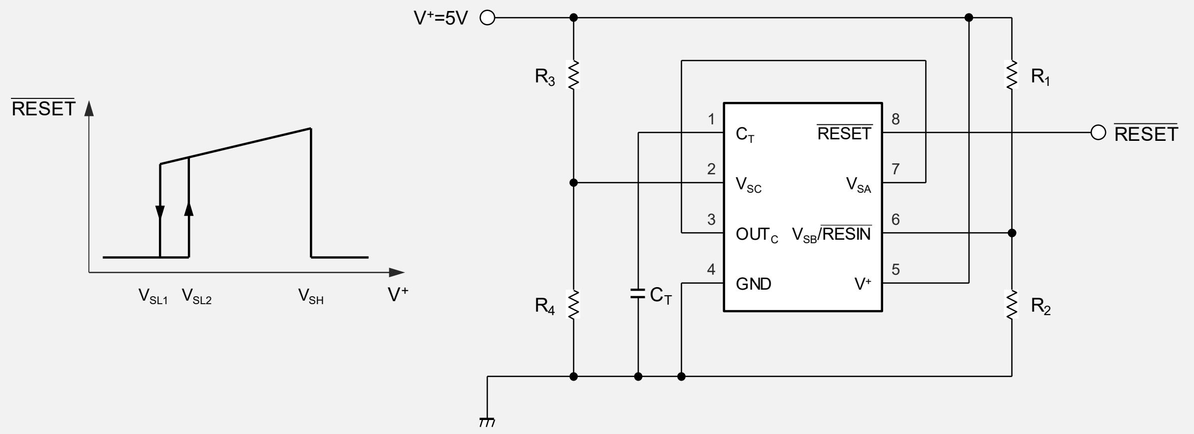
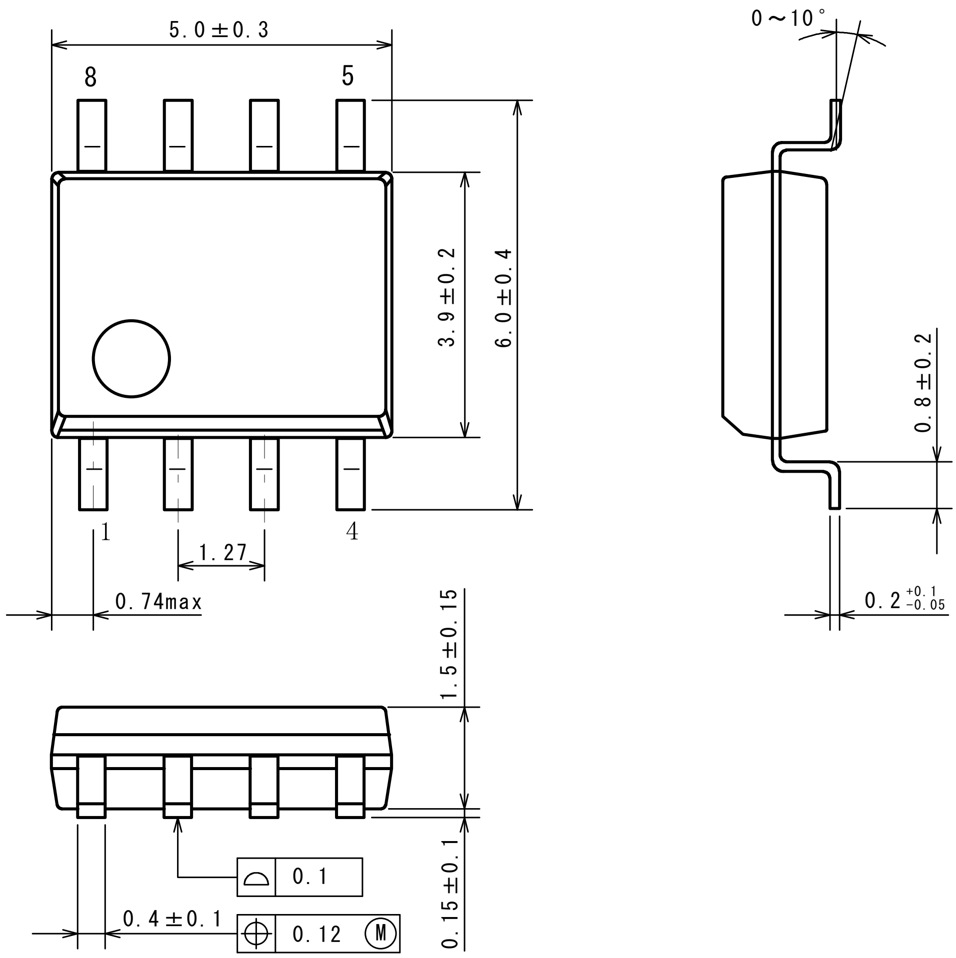


Fig. 14 Low voltage and over voltage detection ($V^+ = 5V$)

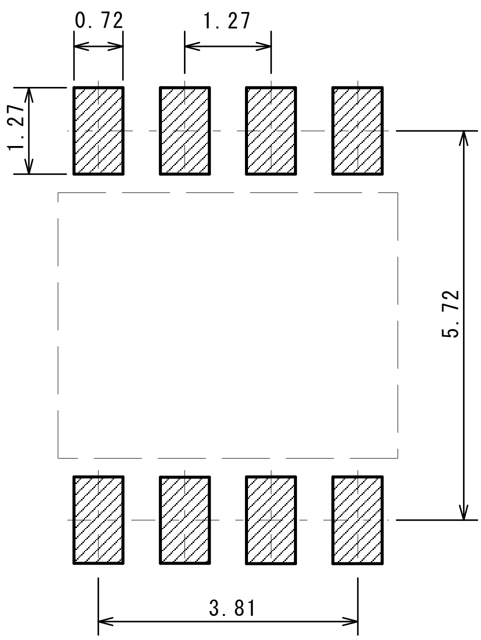
EMP8(SOP8 JEDEC 150mil)

■PACKAGE DIMENSIONS

Unit: mm



■EXAMPLE OF SOLDER PADS DIMENSION

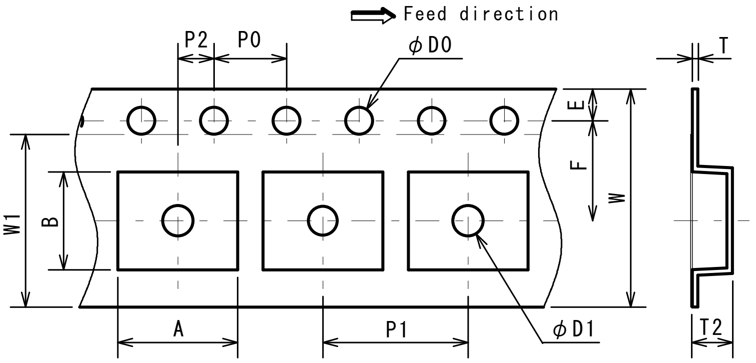


EMP8(SOP8 JEDEC 150mil)

■PACKING SPEC

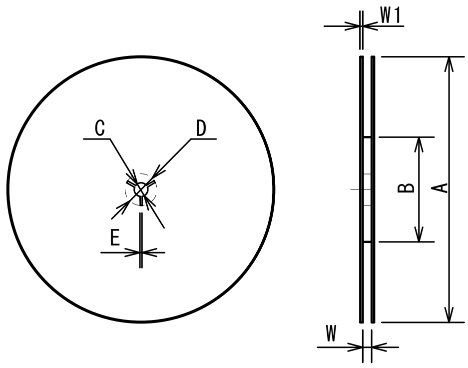
Unit: mm

TAPING DIMENSIONS



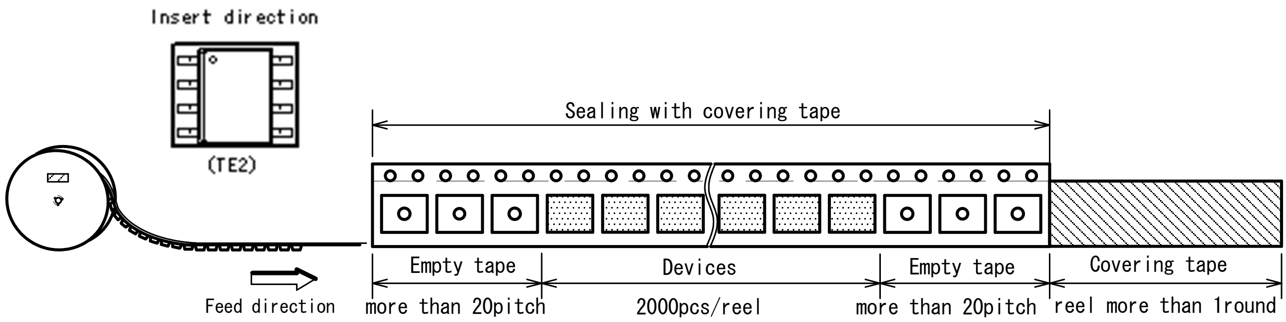
SYMBOL	DIMENSION	REMARKS
A	6.6	BOTTOM DIMENSION
B	5.4	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	1.7±0.1	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.30±0.05	
T2	2.2	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

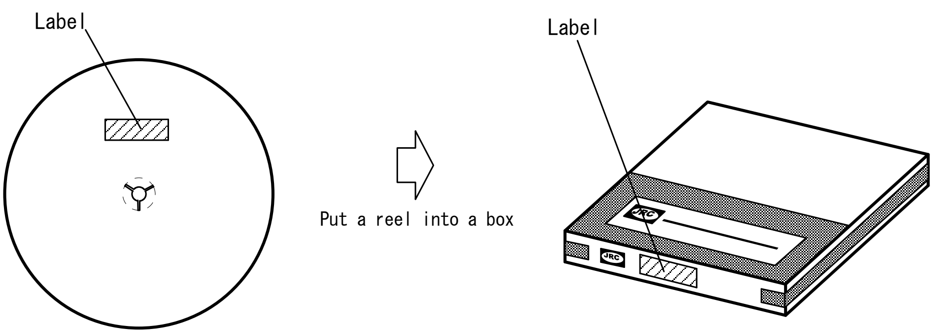


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE



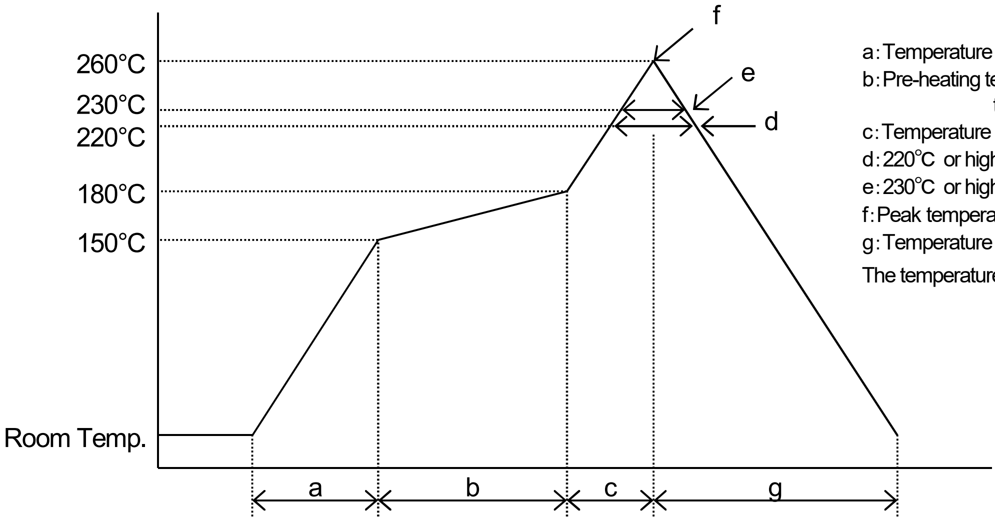
PACKING STATE



■RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

Recommended reflow soldering procedure



a : Temperature ramping rate	: 1 to 4°C /s
b : Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c : Temperature ramp rate	: 1 to 4°C /s
d : 220°C or higher time	: Shorter than 60s
e : 230°C or higher time	: Shorter than 40s
f : Peak temperature	: Lower than 260°C
g : Temperature ramping rate	: 1 to 6°C /s

The temperature indicates at the surface of mold package.

■REVISION HISTORY

Date	Revision	Changes
12.Nov.2018.	1.0	New Release
07.Feb.2019	1.1	Correction of error

[CAUTION]

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   ・Vehicle Control Equipment (Airplane, railroad, ship, etc.)
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