

A Complete Development Environment

What's in the Box

- Arria® 10 SoC development board
- 2 x USB cable mini
- 1 x USB cable micro
- 1 x USB host micro adapter
- Ethernet cable
- MicroSD daughtercard
- Quad SPI daughtercard
- NAND daughtercard
- 2 x DDR4 HILO memory cards
- Quick Start Guide

Arria 10 SoC Board Features

- Arria 10 SoC
- Embedded USB-Blaster[™] II for hard processor system (HPS) or FPGA programming/debugging
- PCI Express® (PCIe®) Gen3 x8
- Dual FPGA mezzanine card (FMC) expansion headers
- Two 10/100/1000 SGMII Ethernet ports, one 10/100/1000 RGMII Ethernet port and two 10GbE small form factor pluggable (SFP) cages
- USB On-The-Go (USB OTG) port
- Character LCD
- Display port and SDI port

Available Resources

The following software and tools are available for download:

- Documentation
 - Schematics and design files
 - Arria 10 SoC Development Kit User Guide
 - SoC Embedded Design Suite (EDS) User's Guide
 - Golden System Reference Design User Manual
- Design and development tools
 - Altera® SoC EDS, including ARM® Development Studio 5™ (DS-5™) Altera Edition Toolkit
 - Quartus® Prime design software
- Design examples
 - Golden System Reference Design

For documentation download and other resources, view the online Quick Start Guide at **altera.com/socqs**





Verify Basic Operation

- a. Attach the Ethernet cable from the board's HPS Ethernet jack (J5) to your network.
- b. Ensure that the MicroSD daughtercard is mounted in the J23 socket and the MicroSD boot card is inserted.
- c. Connect the power adapter from an A/C outlet to J36 on the board, then turn on the board using the Power Switch SW5.
- d. The HPS begins booting the Golden System Reference Design Linux image. After the image is booted, the system's LCD screen displays an IP address and "ALTERA.COM/SOCQS". If you do not have an available network port, or your network does not have a DHCP server, or if the system is unable to get an IP address, the LCD screen displays "No IP obtained". Proceed to step g.
- e. To see the Board Update Portal web server, open a browser, and type the IP address from the board into the URI field.

	Arria 10 SoC Development Kit
Overview	Developer Resources
	Hardware Developers
No Board update Detail web page is being served by the web server applicable numbers to the Net Phonese Staten (MSI) of use development beam. This web page services last to useful information on Altern ² website, Rease refer to the ode bar for the fifterence links. You can use this web page to interact with your based by binking the EDs and writing text messages to LCD on the board.	Software Developers
touse over the board photo to view features.	

Figure 1. Board Update Portal

- f. The Board Update Portal web server allows you to verify operation of the board and FPGA by: Blinking LEDs on the board
 - Writing text messages to the LCD display
- g. For a more detailed Quick Start Guide including information on FPGA design tools, software development tools, and documentation, browse to altera.com/socgs.
- h. For additional Linux resources, browse to the **rocketboards.org** community portal and select the "Start" button.



Electromagnetic interference caused by any modification made to the kit contents is the sole responsibility of the user. This equipment is designated for use only in an industrial research environment.

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.



FCC NOTICE: This kit is designed to allow:





Software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under FCC Part 5 of CFR Title 47.

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