

32K x 16 HIGH-SPEED CMOS STATIC RAM

JANUARY 2020

FEATURES

- High-speed access time: 12 ns
- Low Active Power: 175 mW (typical)
- Low Standby Power: 1 mW (typical) CMOS standby
- TTL compatible interface levels
- Single 5V \pm 10% power supply
- Fully static operation: no clock or refresh required
- Available in 44-pin SOJ package and 44-pin TSOP (Type II)
- Commercial and Industrial temperature ranges available
- Lead-free available

DESCRIPTION

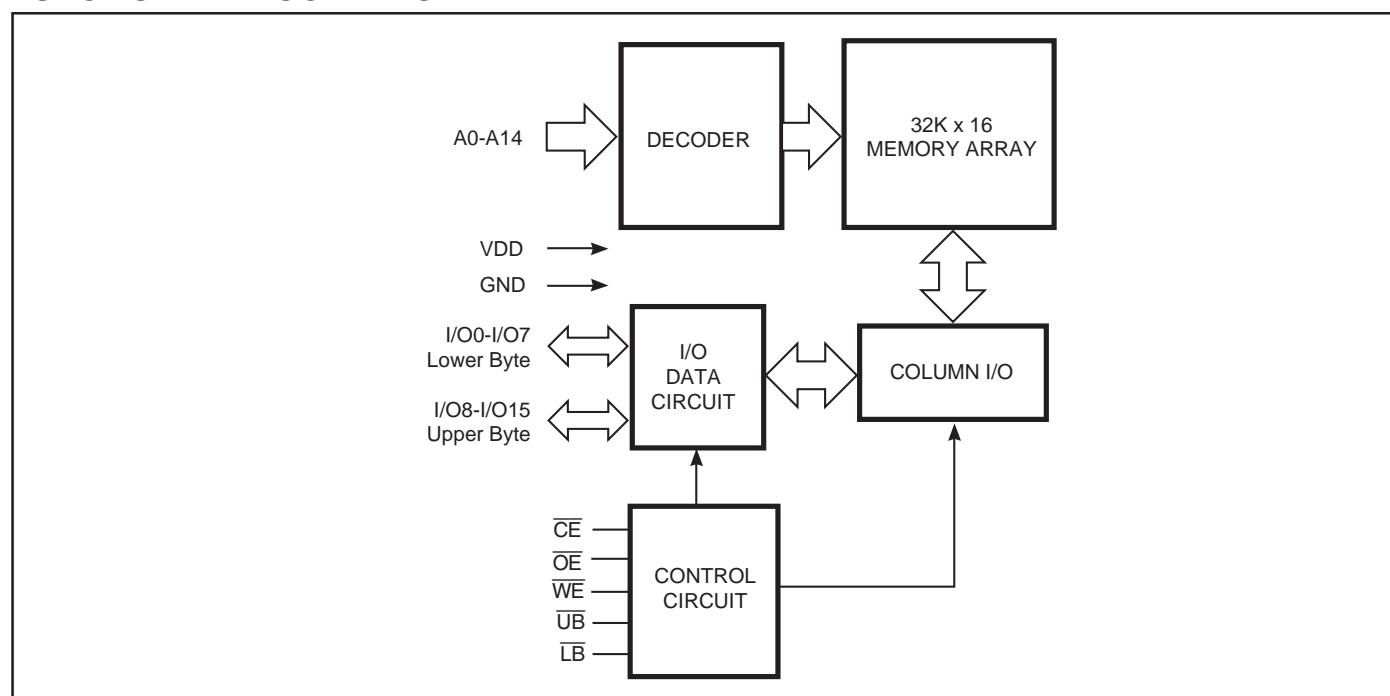
The *ISSI* IS61C3216AL is high-speed, 512Kb static RAMs organized as 32,768 words by 16 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS61C3216AL is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type II).

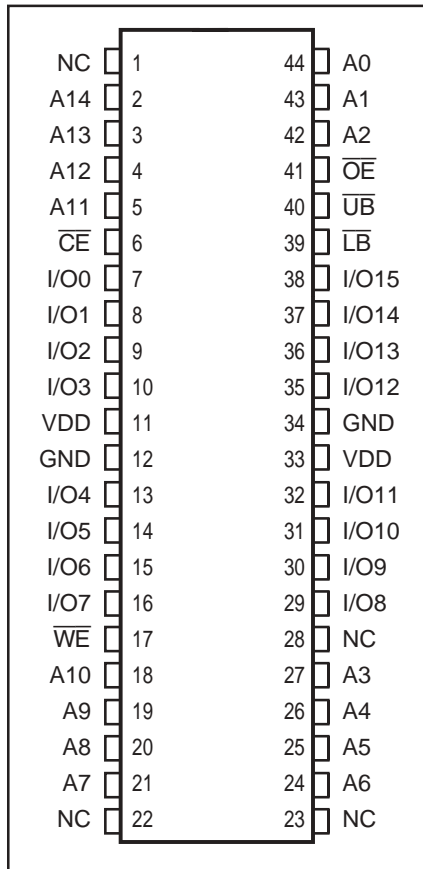
FUNCTIONAL BLOCK DIAGRAM



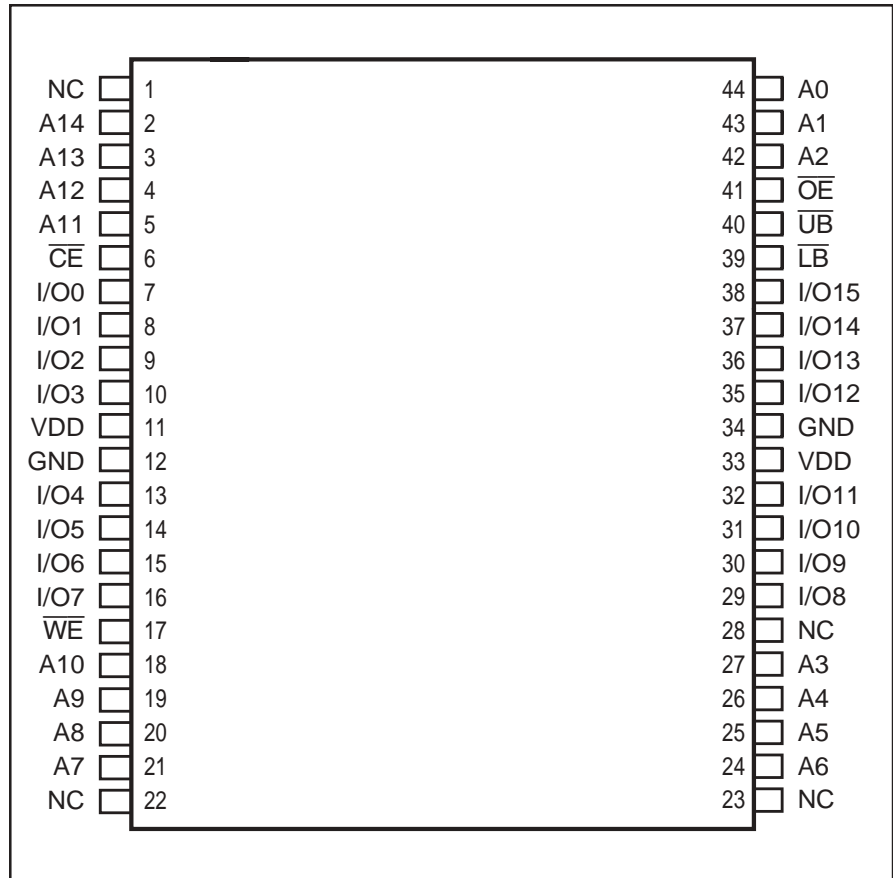
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PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A14	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input

LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	\overline{WE}	\overline{CE}	\overline{OE}	\overline{LB}	\overline{UB}	I/O PIN		V_{DD} Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1} , I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC1} , I_{CC2}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	Dout	High-Z	I_{CC1} , I_{CC2}
	H	L	L	H	L	High-Z	Dout	
	H	L	L	L	L	Dout	Dout	
Write	L	L	X	L	H	Din	High-Z	I_{CC1} , I_{CC2}
	L	L	X	H	L	High-Z	Din	
	L	L	X	L	L	Din	Din	

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS61C3216AL)

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -4.0 mA	2.4	—	V	
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA	—	0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{DD} + 0.5	V	
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V	
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com.	-1	1	μA
			Ind.	-2	2	
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} Outputs Disabled	Com.	-1	1	μA
			Ind.	-2	2	

Note:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

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POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-12 ns		Unit
				Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = V _{DD MAX.} , $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = 0	Com.	—	40	mA
			Ind.	—	45	
I _{CC2}	V _{DD} Dynamic Operating Supply Current	V _{DD} = V _{DD MAX.} , $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	50	mA
			Ind.	—	55	
			typ. ⁽²⁾		35	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = V _{DD MAX.} , V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1	mA
			Ind.	—	1	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = V _{DD MAX.} , $\overline{CE} \leq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	350	μA
			Ind.	—	400	
			typ. ⁽²⁾		200	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-12		Unit
		Min.	Max.	
t _{RC}	Read Cycle Time	12	—	ns
t _{AA}	Address Access Time	—	12	ns
t _{OH}	Output Hold Time	3	—	ns
t _{ACE}	\overline{CE} Access Time	—	12	ns
t _{DOE}	\overline{OE} Access Time	—	6	ns
t _{HZOE⁽²⁾}	\overline{OE} to High-Z Output	0	6	ns
t _{LZOE⁽²⁾}	\overline{OE} to Low-Z Output	0	—	ns
t _{HZCE⁽²⁾}	\overline{CE} to High-Z Output	0	7	ns
t _{LZCE⁽²⁾}	\overline{CE} to Low-Z Output	2	—	ns
t _{BA}	$\overline{LB}, \overline{UB}$ Access Time	—	6	ns
t _{HZB}	$\overline{LB}, \overline{UB}$ to High-Z Output	0	6	ns
t _{LZB}	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

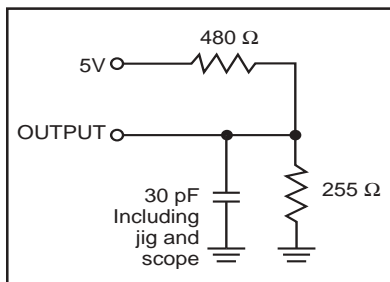


Figure 1

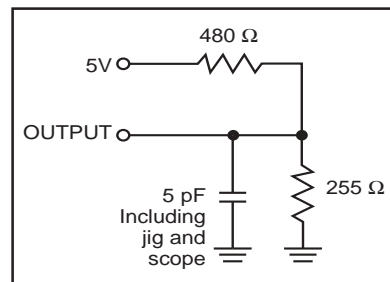
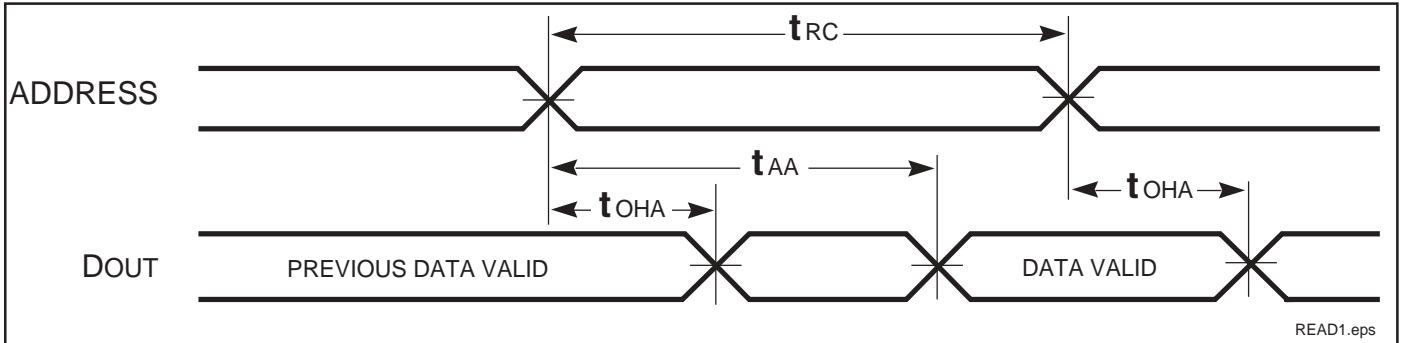


Figure 2

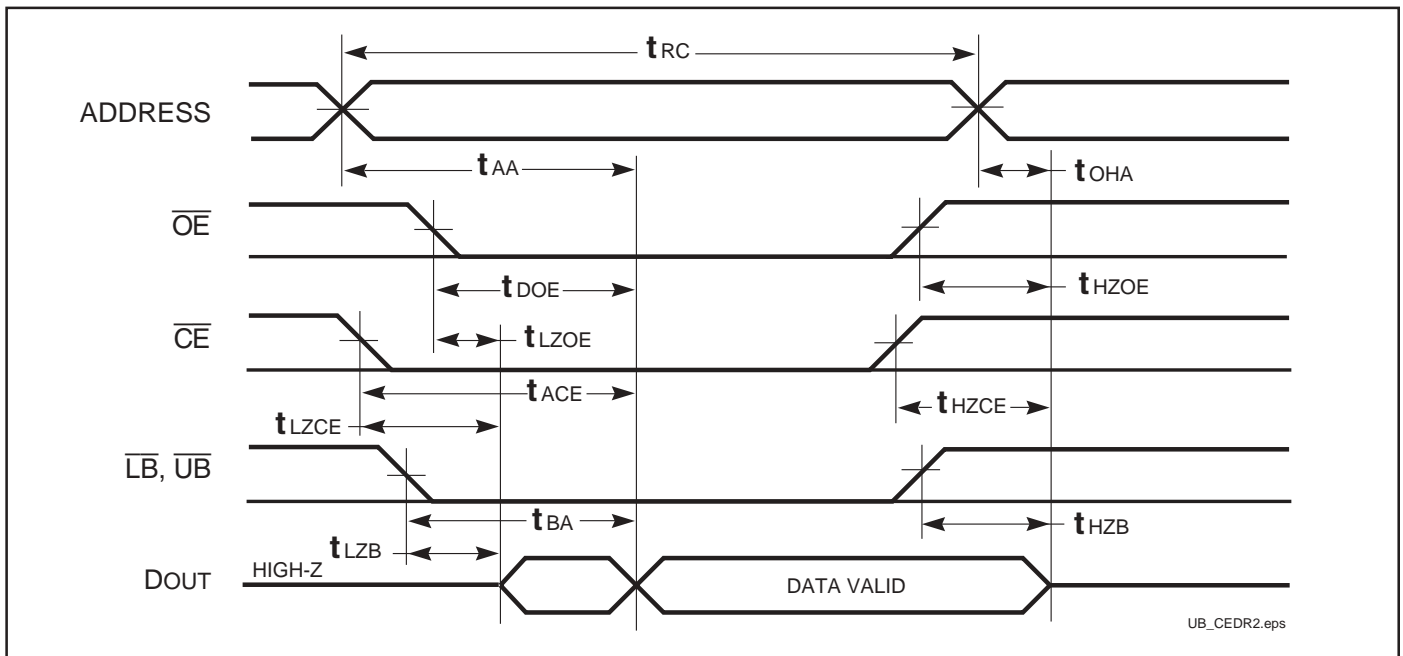
AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ1.eps

READ CYCLE NO. 2^(1,3)



UB_CEDR2.eps

Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

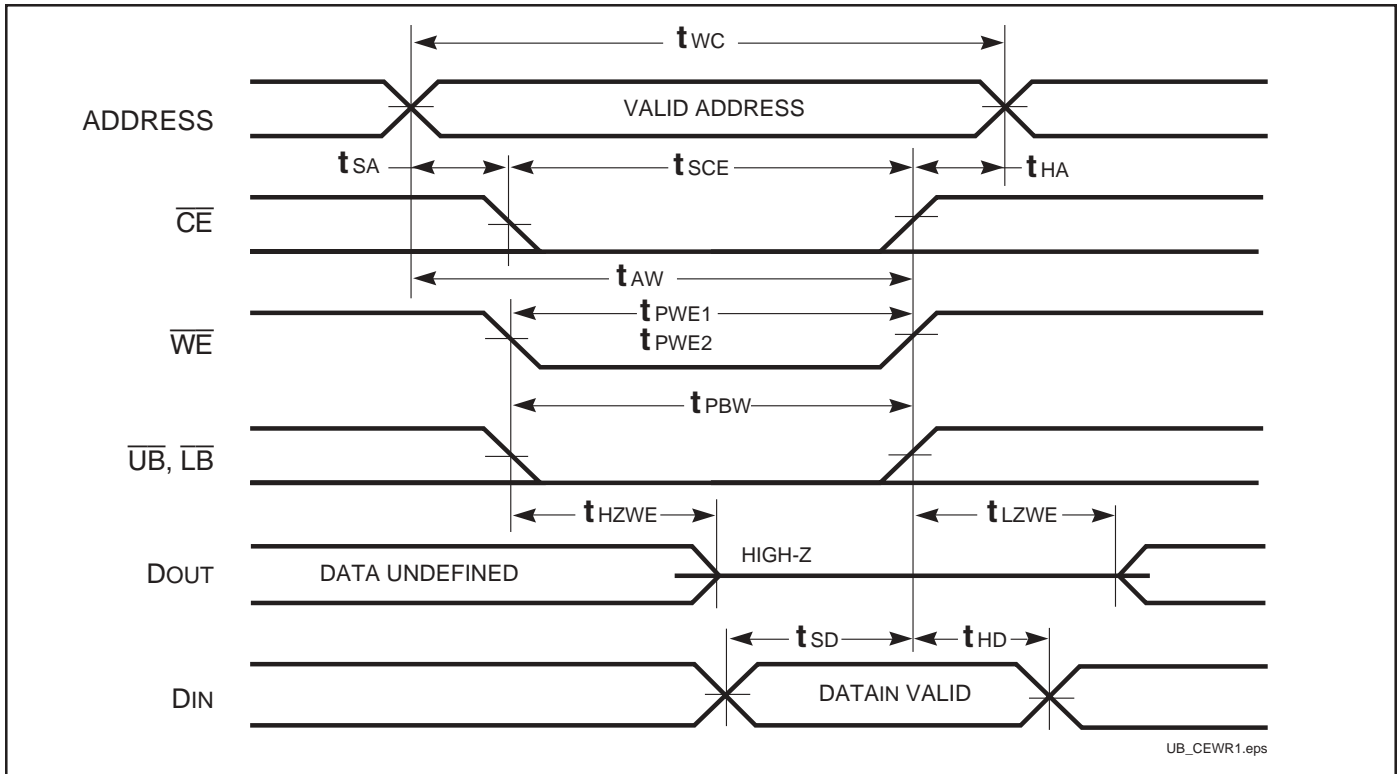
Symbol	Parameter	-12		Unit
		Min.	Max.	
t _{WC}	Write Cycle Time	12	—	ns
t _{SCE}	$\overline{\text{CE}}$ to Write End	9	—	ns
t _{AW}	Address Setup Time to Write End	9	—	ns
t _{HA}	Address Hold from Write End	0	—	ns
t _{SA}	Address Setup Time	0	—	ns
t _{PWB}	$\overline{\text{LB}}, \overline{\text{UB}}$ Valid to End of Write	9	—	ns
t _{PWE1}	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ =High)	9	—	ns
t _{PWE2}	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ =Low)	9	—	ns
t _{SD}	Data Setup to Write End	6	—	ns
t _{HD}	Data Hold from Write End	0	—	ns
t _{HZWE⁽²⁾}	$\overline{\text{WE}}$ LOW to High-Z Output	—	6	ns
t _{LZWE⁽²⁾}	$\overline{\text{WE}}$ HIGH to Low-Z Output	3	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{UB}}$ or $\overline{\text{LB}}$, and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

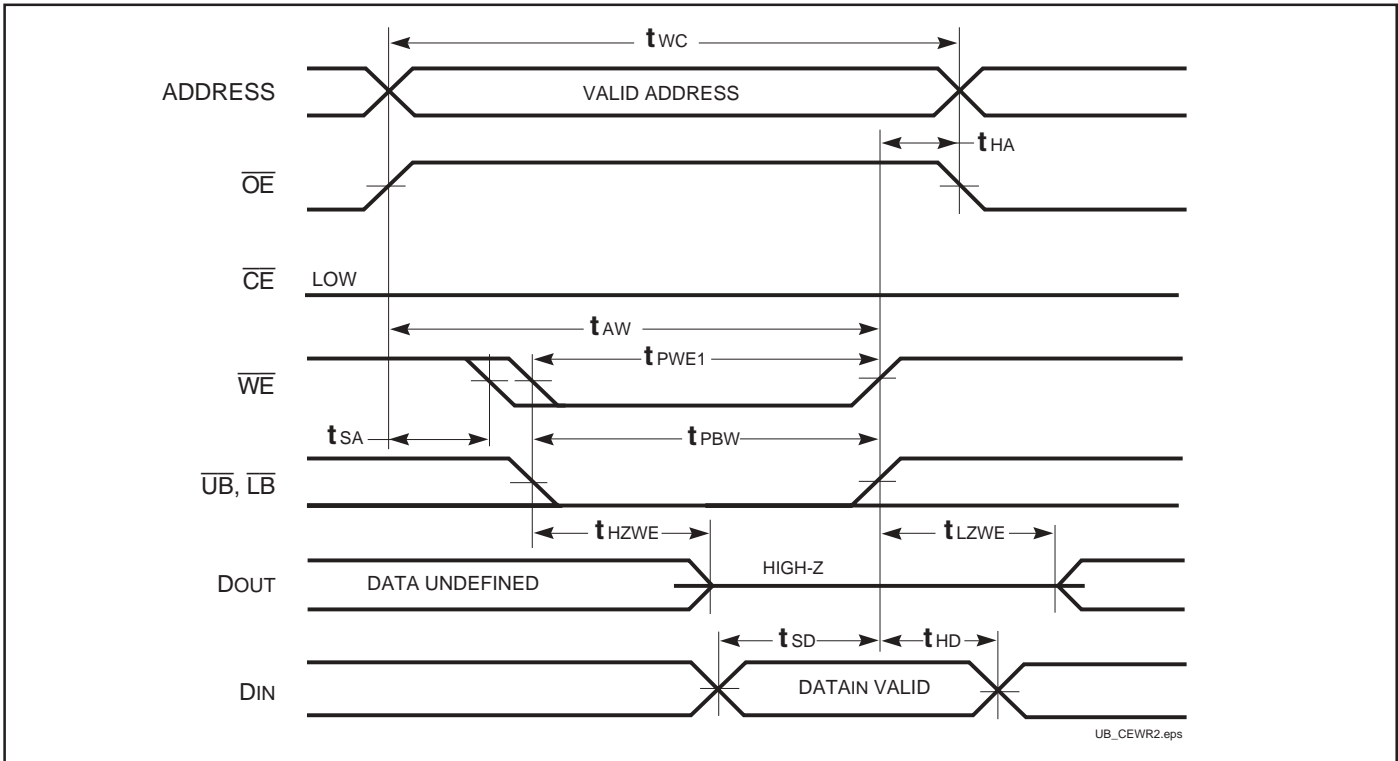
WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)



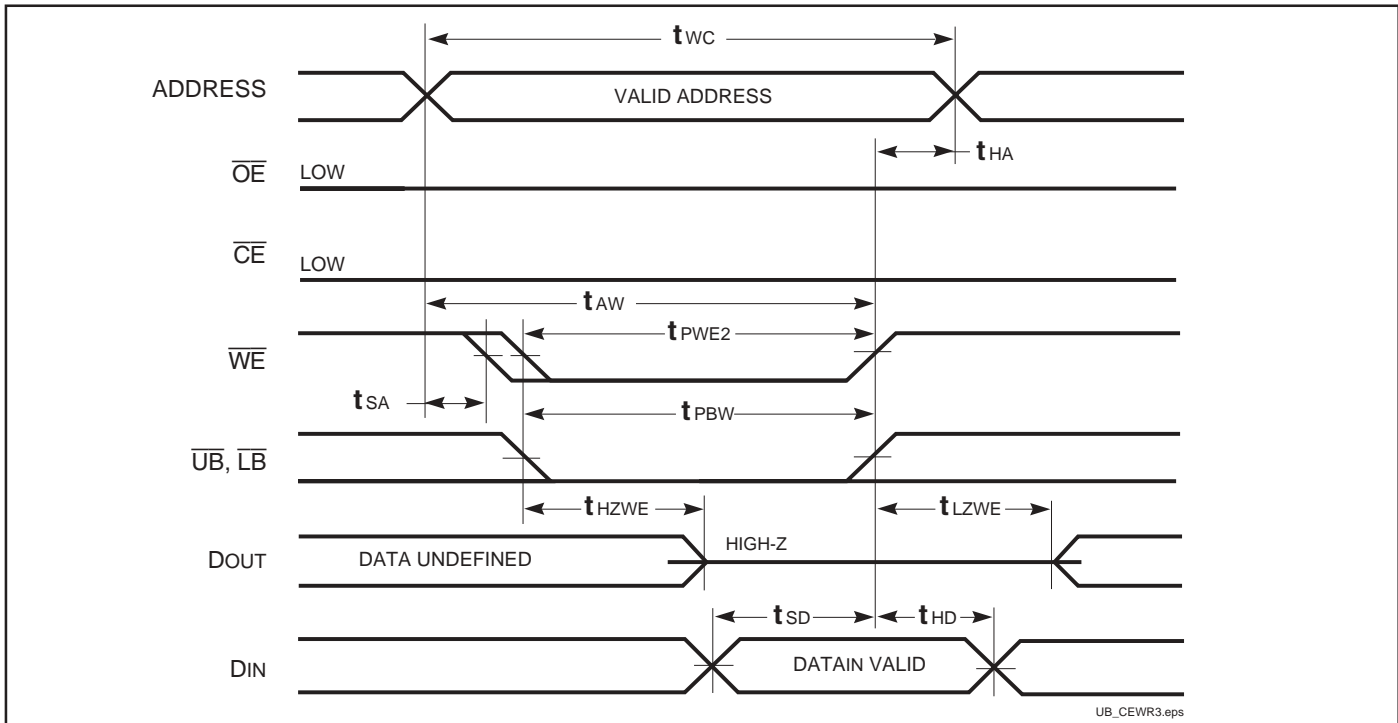
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. WRITE = (\overline{CE}) [(\overline{LB}) = (\overline{UB})] (\overline{WE}).

WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)



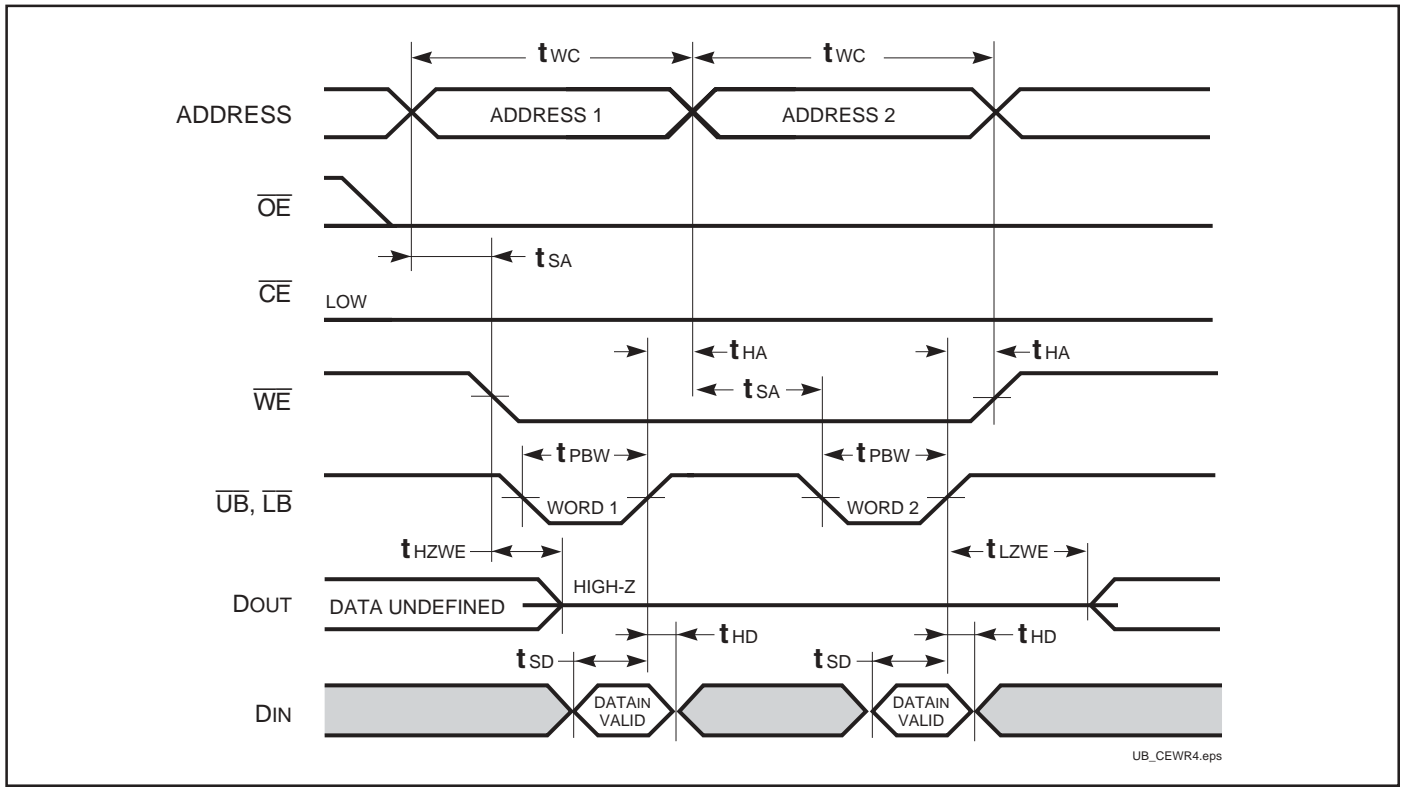
WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾



Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Back to Back Write)



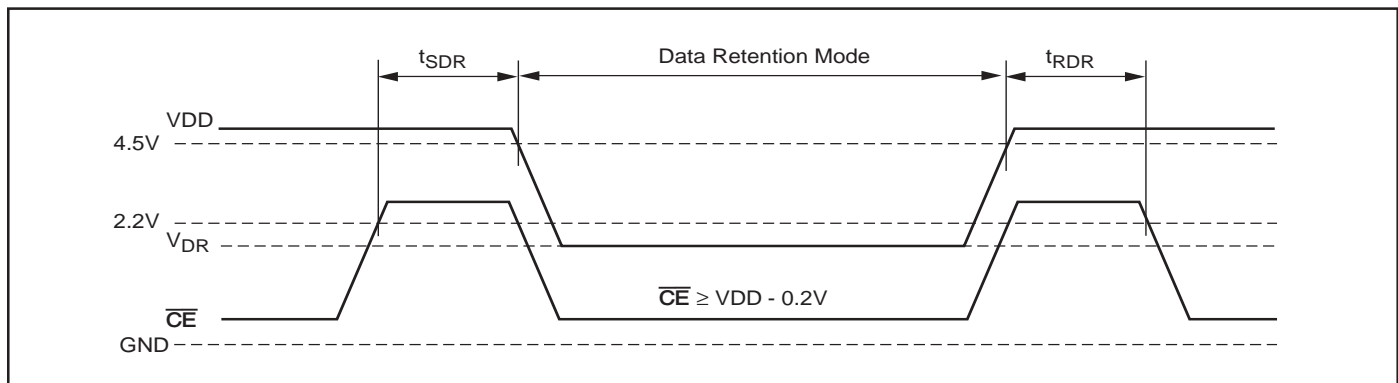
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0		5.5	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V, \text{ or } V_{IN} \leq V_{SS} + 0.2V$	—	—	350	μA
			—	200	400	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}		—	ns

Note:

1. Typical Values are measured at $V_{DD} = 5V, T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)

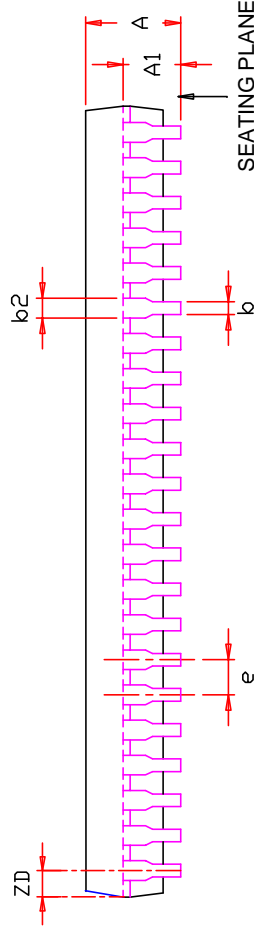
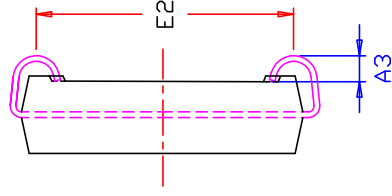
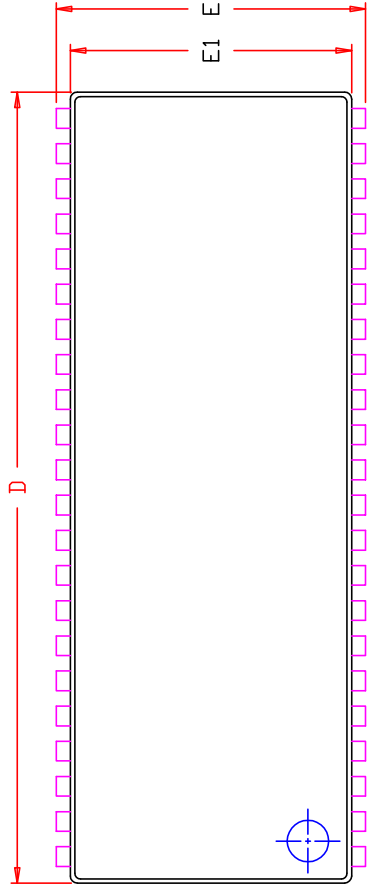


IS61C3216AL

ORDERING INFORMATION: IS61C3216AL

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C3216AL-12KLI	400-mil Plastic SOJ, Lead-free
	IS61C3216AL-12TLI	44-pin TSOP-II, Lead-free



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	NOM. MAX.	MIN.	NOM. MAX.
A	3.25	3.76	0.128	0.148
A1	2.08		0.082	
A3	0.635		0.025	
k	0.38	0.51	0.015	0.020
b2	0.66	0.71	0.026	0.028
D	28.45	28.58	1.120	1.125
E	11.05	11.18	0.435	0.440
E1	10.03	10.16	0.395	0.400
E2	9.40	BSC.	0.370	BSC.
e	1.27	BSC.	0.050	BSC.
ZD	0.95	REF.	0.037	REF.

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.



TITLE

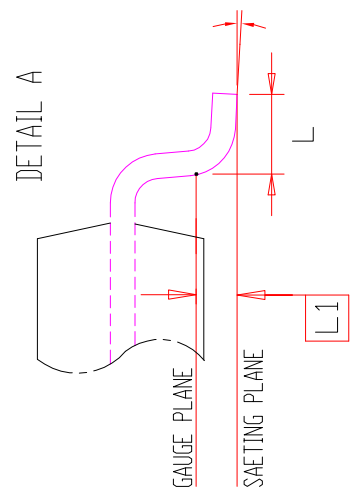
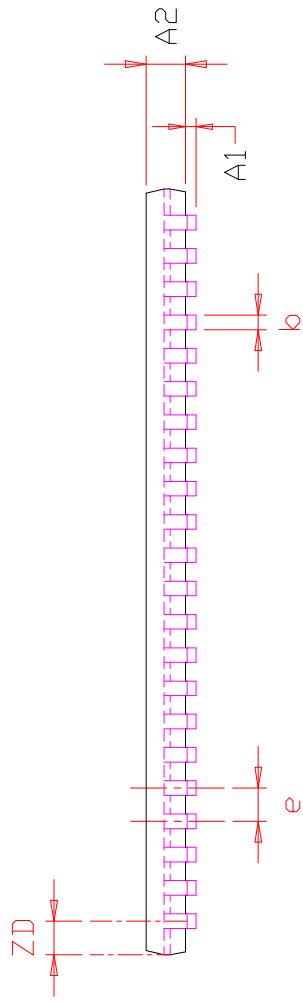
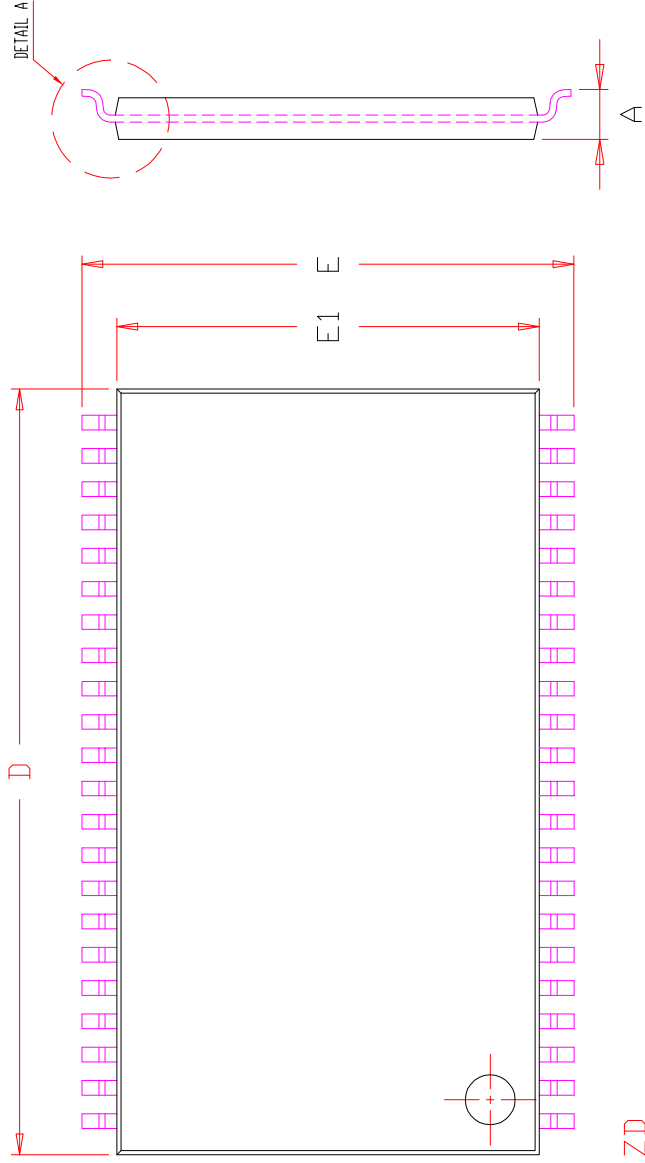
44L 400mil SOJ
Package Outline

REV.

E

DATE

12/21/2007



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	NOM. MAX.	MIN.	NOM. MAX.
A	1.00	1.20	0.039	0.047
A1	0.05	0.15	0.002	0.006
A2	0.95	1.05	0.037	0.041
b	0.30	0.45	0.012	0.018
D	18.28	18.41	0.720	0.730
E	11.56	11.76	0.455	0.471
E1	10.03	10.16	0.395	0.405
e	0.80	BSC.	0.031	BSC.
L	0.40	0.69	0.016	0.027
L1	0.25	BSC.	0.010	BSC.
ZD	0.805	REF.	0.032	REF.
	0	8°	0	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



TITLE

44L 400mil TSOP-2
Package Outline

REV.

F

DATE

06/04/2008