Integrated Transceiver Modules for WLAN 802.11 b/g/n, Bluetooth, and ANT

FEATURES

- IEEE 802.11 b,g,n,d,e,i, compliant
- Typical WLAN Transmit Power:
  - 18.3dBm, 11 Mbps, CCK (b)
  - 12.6 dBm, 54 Mbps, OFDM (g)
  - 9.5 dBm, 65 Mbps, OFDM (n)
- Typical WLAN Sensitivity:
  - -89 dBm, 8% PER, 11 Mbps
  - -76 dBm, 10% PER, 54 Mbps
  - -73 dBm, 10% PER, 65 Mbps
- Bluetooth 2.1+EDR, Power Class 1.5
- Full support for ANT
- Miniature footprint: 18 mm x 13 mm
- Low height profile: 1.9 mm
- U.FL connector for external antenna
- Terminal for PCB/Chip antenna feeds
- Integrated band-pass filter
- Worldwide acceptance: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan)
- Modular certification allows reuse of LSR FCC ID and ETSI certification without repeating the expensive testing on your end product
- Compact design based on Texas Instruments WL1271 Transceiver
- Seamless integration with TI OMAP™ application processors
- SDIO Host data path interfaces
- Bluetooth Advanced Audio Interfaces
- Low power operation mode
- RoHS compliant

APPLICATIONS

- Security
- HVAC Control, Smart Energy
- Sensor Networks
- Medical

DESCRIPTION

The TiWi-R2 module is a high performance 2.4 GHz IEEE 802.11 b/g/n and Bluetooth 2.1+EDR radio in a cost effective, pre-certified footprint.

The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.

The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Need to get to market quickly? Not an expert in 802.11 or Bluetooth? Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? LSR Design Services will be happy to develop custom hardware or software, integrate the design, or license the design so you can manufacture yourself. Contact us at sales@lsr.com or call us at 262-375-4400.

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ORDERING INFORMATION

Order Number	Description
450-0037	TiWi-R2 Module with U.FL connector for external antenna (Tray, SPQ = 100)
450-0037R	TiWi-R2 Module with U.FL connector for external antenna (Tape and Reel, SPQ = 1000)

Table 1 Orderable TiWi-R2 Part Numbers

MODULE ACCESSORIES

	Order Number	Description
	001-0001	2.4 GHz Dipole Antenna with Reverse Polarity SMA Connector
	080-0001	U.FL to Reverse Polarity SMA Bulkhead Cable 105mm

Table 2 Module Accessories

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BLOCK DIAGRAM
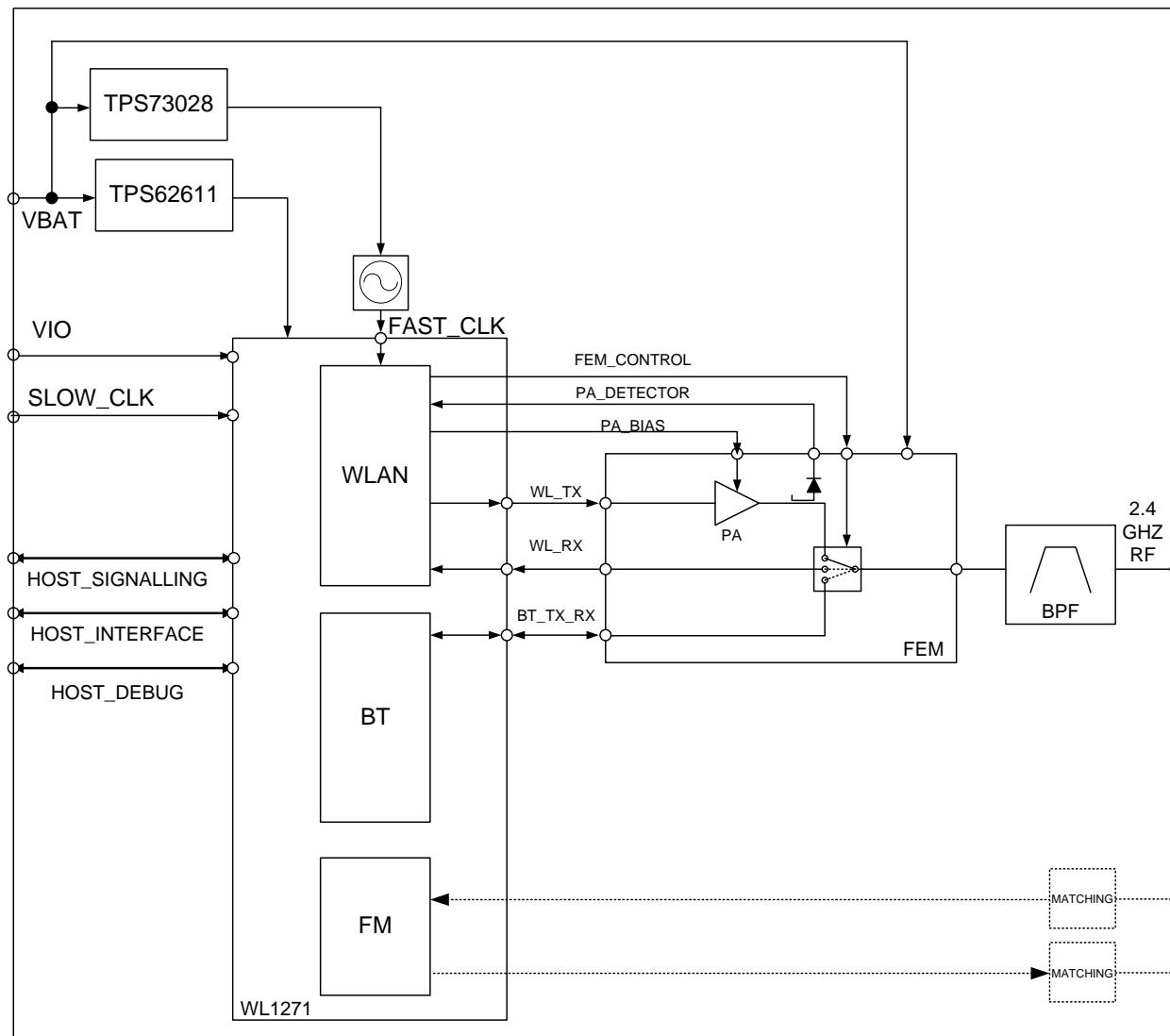
Figure 1 TiWi-R2 Module Block Diagram – Top-Level

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TIWI-R2 MODULE FOOTPRINT AND PIN DEFINITIONS

To apply the TiWi-R2 module, it is important to use the module pins in your application as they are designated in below and in the corresponding pin definition table found on pages 8 and 9. Not all the pins on the TiWi-R2 module may be used, as some are reserved for future functionality.
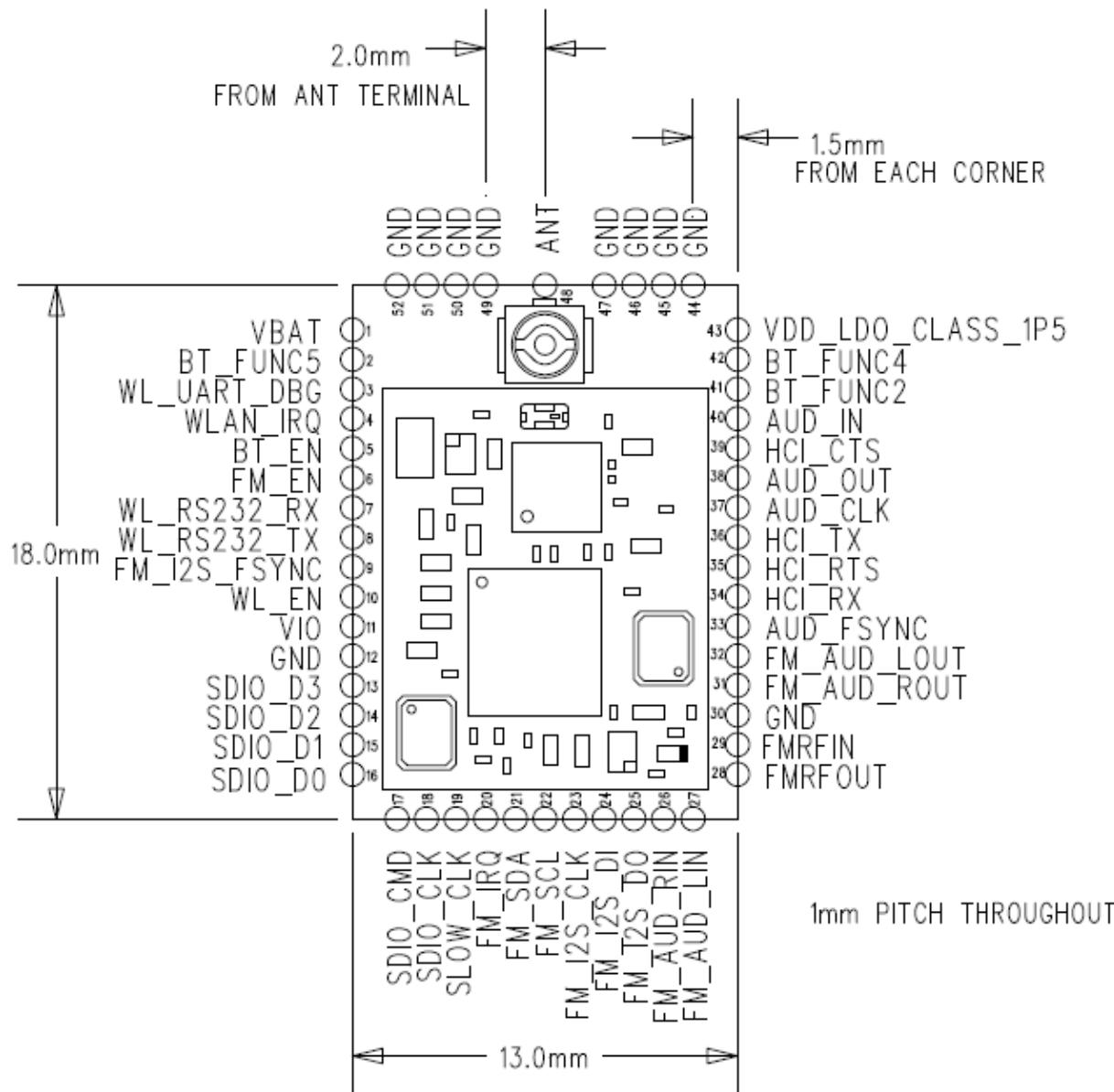

Figure 2 TiWi-R2 Pinout (Top View)

PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Buffer Type	Logic Level	Description
1	VBAT	PI	-	-	Battery Voltage 3.6 VDC Nominal (3.0-4.8 VDC)
2	BT_FUNC5	DO	4 mA	1.8 VDC	HOST_WU (*)
3	WL_UART_DBG	DIO	4 mA	1.8 VDC	WL_UART_DBG
4	WLAN_IRQ	DO	4 mA	1.8 VDC	WLAN Interrupt Request
5	BT_EN	DI	-	1.8 VDC	Bluetooth Enable
6	FM_EN	DI	-	1.8 VDC	NOT SUPPORTED, CONNECT TO GND
7	WL_RS232_RX	DI	-	1.8 VDC	WLAN TEST UART RX (*)
8	WL_RS232_TX	DO	4 mA	1.8 VDC	WLAN TEST UART TX (*)
9	FM_I2S_FSYNC	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
10	WL_EN	DI	-	1.8 VDC	WLAN Enable
11	VIO	PI	-	-	POWER SUPPLY FOR 1.8 VDC DIGITAL DOMAIN
12	GND	GND	-	-	Ground
13	SDIO_D3	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
14	SDIO_D2	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
15	SDIO_D1	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
16	SDIO_D0	DIO	8 mA	1.8 VDC	SDIO INTERFACE, HOST PULL UP
17	SDIO_CMD	DIO	8 mA	1.8 VDC	HOST PULL UP
18	SDIO_CLK	DI	-	1.8 VDC	HOST PULL UP
19	SLOW_CLK	DI	-	1.8 VDC	SLEEP CLOCK (32 kHz)
20	FM_IRQ	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
21	FM_SDA	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
22	FM_SCL	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
23	FM_I2S_CLK	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
24	FM_I2S_DI	DI	4 mA	1.8 VDC	NOT SUPPORTED, CONNECT TO GND
25	FM_I2S_DO	DO	4 mA	1.8 VDC	NOT SUPPORTED, NO CONNECT
26	FM_AUD_RIN	AI	-	-	NOT SUPPORTED, CONNECT TO GND
27	FM_AUD_LIN	AI	-	-	NOT SUPPORTED, CONNECT TO GND
28	FMRFOUT	AO	-	-	NOT SUPPORTED, NO CONNECT
29	FMRFIN	AI	-	-	NOT SUPPORTED, CONNECT TO GND
30	GND	GND	-	-	Ground

The information in this document is subject to change without notice.

Module Pin	Name	I/O Type	Buffer Type	Logic Level	Description
31	FM_AUD_ROUT	AO	-	-	NOT SUPPORTED, NO CONNECT
32	FM_AUD_LOUT	AO	-	-	NOT SUPPORTED, NO CONNECT
33	AUD_FSYNC	DIO	4 mA	1.8 VDC	PCM I/F
34	HCI_RX	DI	8 mA	1.8 VDC	Bluetooth HCI UART RX (*)
35	HCI_RTS	DO	4 mA	1.8 VDC	Bluetooth HCI UART RTS (*)
36	HCI_TX	DIO	8 mA	1.8 VDC	Bluetooth HCI UART TX
37	AUD_CLK	DO	4 mA	1.8 VDC	PCM I/F (*)
38	AUD_OUT	DO	4 mA	1.8 VDC	PCM I/F (*)
39	HCI_CTS	DI	4 mA	1.8 VDC	Bluetooth HCI UART CTS (*)
40	AUD_IN	DI	4 mA	1.8 VDC	PCM I/F (*)
41	BT_FUNC2	DI	4 mA	1.8 VDC	Bluetooth Wakeup[DI] / DC2DC mode[DO](*)
42	BT_FUNC4	DO	4 mA	1.8 VDC	BT_UARTD (DEBUG) (*)
43	VDD_LDO_CLASS_1P5	NC	-	-	VBAT VOLTAGE PRESENT, NO CONNECT
44	GND	GND	-	-	Ground
45	GND	GND	-	-	Ground
46	GND	GND	-	-	Ground
47	GND	GND	-	-	Ground
48	ANT	RF		-	Antenna terminal for WLAN and Bluetooth (Note [1])
49	GND	GND	-	-	Ground
50	GND	GND	-	-	Ground
51	GND	GND	-	-	Ground
52	GND	GND	-	-	Ground

PI = Power Input   PO = Power Output   DI = Digital Input (1.8 VDC Logic Level)   DO=Digital Output (1.8 VDC Logic Level)

AI = Analog Input   AO = Analog Output   AIO = Analog Input/Output   RF = RF Port   GND = Ground

Note[1]: Antenna terminal presents d.c. short circuit to ground.

(*) indicates that pin is capable of bidirectional operation, but is used as the type shown.

Table 3 TiWi-R2 Module Pin Descriptions

All digital I/O signals use 1.8V logic. If the host microcontroller does not support 1.8V logic, then level shifters MUST be used.

The information in this document is subject to change without notice.

BT_FUNC2 and BT_FUNC5 Pins

When BT is awake and active, BT_WU (BT_FUNC2) is high (from host to module). This is an active high signal. The host puts the BT section to sleep by de-asserting (logic low level) the BT_WU signal (input to the module). The module then drives HOST_WU (BT_FUNC5) low to acknowledge to the host that it is has been put into sleep mode.

Using these pins is optional.

BT_FUNC4 Pin

The BT_FUNC4 (BT_UARTD) pin is a debug pin. It is a 1.8V logic UART TX line. This pin should never need to be used in normal operation. It may be useful to terminate this pin to a test point or header in case it is needed.

WL_UART_DBG Pin

The WL_UART_DBG pin is a debug pin. It is a 1.8V logic UART TX line. This pin should never need to be used in normal operation. It may be useful to terminate this pin to a test point or header in case it is needed.

WL_RS232_RX and WL_RS232_TX Pins

These pins are used for a WLAN test mode interface. Both pins are 1.8V logic level UART pins. These pins should be brought out to a header on the host PCB. The WLAN test interface can be used to place the module into constant packet transmit and constant packet receive modes. These modes can be useful for antenna and sensitivity testing.

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INI FILE RADIO PARAMETERS AND BLUETOOTH PATCH FILES

There are ini files that contains WLAN radio parameters which are critical to both the RF performance and EMC compliance of the module in various antenna configurations.

The ini files available on the LSR wiki website are only intended to be used with the LSR WLAN Eval Tool. Note that the ini file will not work when using the TiWi-R2 module in normal operation which typically involves an operating system. To use the TiWi-R2 module in normal operation, refer to specifics contained in the TiWi Family INI File Radio Parameter User Guide which is also available for download on the LSR wiki website, http://wiki.lsr.com/ .

The settings specified in the appropriate ini file must be used to operate the module in compliance with the modular certification for FCC or ETSI. There are two ini files for operating the module in compliance with FCC regulations that corresponds to different antenna configuration, and a different ini file for operating the module in compliance with the ETSI regulations.

The Bluetooth patch files are available on the LSR wiki website. The appropriate patch file must be selected to operate the module in compliance with the modular certification for FCC or ETSI.

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ELECTRICAL SPECIFICATIONS

The majority of these characteristics are based on controlling and conditioning the tests using the TiWi-R2 control software application. Other control conditions may require these values to be re-characterized by the customer.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage (VBAT)[4][5]	-0.5	+5.5	V
Digital supply voltage (VIO)	-0.5	2.1	V
Voltage on any GPIO	-0.5	VIO + 0.5	V
Voltage on any Analog Pins[3]	-0.5	2.1	V
RF input power, antenna port		+10	dBm
Operating temperature[6]	-40	+85	ºC
Storage temperature	-55	+125	ºC

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device and are not covered by the warranty. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All parameters are measured as follows unless stated otherwise: VDD_IN=1.8V, VDDIO_1.8V=1.8V, VDD_LDO_CLASS1P5=3.6V
3. Analog pins: XTALP, XTALM, RFIOBT, DRPWRXBM, DRPWRXBP, DRPWTXB, and also FMRFINP, FMRFINM, FMRFINM, FMAUDLIN, FMAUDRIN, FMAUDLOUT, FMAUDROUT
4. The following signals are from the VBAT group, PMS_VBAT and VDD_LDO_CLASS1P5 (if BT class 1.5 direct VBAT is used).
5. Maximum allowed depends on accumulated time at that voltage; 4.8V for 7 years lifetime, 5.5V for 6 hours cumulative.
6. The device can be reliably operated for 5,000 active-WLAN cumulative hours at T_A of 85ºC.

Table 4 Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{BAT}	3.0	3.6	4.8	V
VIO	1.62	1.8	1.92	V
V_{IH}	0.65 x VIO	-	VIO	V
V_{IL}	0	-	0.35 x VIO	V
V_{OH} @ 4, 8 mA	VIO - 0.45	-	VIO	V
V_{OL} @ 4, 8 mA	0	-	0.45	V
Ambient temperature range	-40	25	85	ºC

Table 5 Recommended Operating Conditions

The information in this document is subject to change without notice.

General Characteristics

Parameter	Min	Typ	Max	Unit
WLAN RF frequency range	2412		2472	MHz
WLAN RF data rate	1	802.11 b/g/n rates supported	65	Mbps
BT RF frequency Range	2402		2480	MHz

Table 6 General Characteristics

Power Consumption - WLAN

Parameter	Test Conditions	Min	Typ	Max	Unit
CCK (802.11b) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=18.3 dBm, 11 Mbps CCK L=1200 bytes, t_{delay} (idle)=4 ⬚S	-	270	-	mA
OFDM (802.11g) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=12.6 dBm, 54 Mbps OFDM L=1200 bytes, t_{delay} (idle)=4 ⬚S	-	171	-	mA
OFDM (802.11n) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=9.5 dBm, 65 Mbps OFDM L=1200 bytes, t_{delay} (idle)=4 ⬚S	-	152	-	mA
CCK (802.11b) RX Current		-	100	-	mA
OFDM (802.11g) RX Current		-	100	-	mA
OFDM (802.11n) RX Current		-	100	-	mA
Dynamic Mode [1]		-	<1.2	-	mA

[1] Total Current from V_{BAT} for reception of Beacons with DTIM=1 TBTT=100 mS, Beacon duration 1.6ms, 1 Mbps beacon reception in Listen Mode.

Table 7 WLAN Power Consumption

Power Consumption - Bluetooth

Parameter	Test Conditions	Min	Typ	Max	Unit
GFSK TX Current	Constant Transmit, DH5, PRBS9	-	45	-	mA
EDR TX Current	Constant Transmit, 2DH5,3DH5, PRBS9	-	43	-	mA
GFSK RX Current	Constant Receive, DH1	-	35	-	mA
EDR RX Current	Constant Receive, 2DH5, 3DH5	-	41	-	mA
Deep Sleep Current	Deep Sleep Mode	-	70	-	µA

Table 8 Bluetooth Power Consumption

DC Characteristics – General Purpose I/O

Parameter	Test Conditions	Min	Typ	Max	Unit
VIO Current			-	16	mA
Logic input low, V_{IL}		0	-	0.35 x VIO	V
Logic input high, V_{IH}		0.65 x VIO	-	VIO	V
Logic output low, V_{OL} (Full Drive)	Iout = 8 mA	0	-	0.45	V
	Iout = 4 mA	0	-	0.45	V
Logic output low, V_{OL} (Reduced Drive)	Iout = 1 mA	0	-	0.112	V
	Iout = 0.09 mA	0	-	0.01	V
Logic output high, V_{OH} (Full Drive)	Iout = -8 mA	VIO - 0.45	-	VIO	V
	Iout = -4 mA	VIO - 0.45	-	VIO	V
Logic output high, V_{OH} (Reduced Drive)	Iout = -1 mA	VIO - 0.112	-	VIO	V
	Iout = -0.3 mA	VIO - 0.033	-	VIO	V

Table 9 DC Characteristics General Purpose I/O

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WLAN RF Characteristics

WLAN Transmitter Characteristics
(TA=25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
11 Mbps CCK (802.11b) TX Output Power	11 Mbps CCK , 802.11(b) Mask Compliance, 35% EVM RMS power over TX packet	-	18.3	-	dBm
9 Mbps OFDM (802.11g) TX Output Power	9 Mbps OFDM , 802.11(g) Mask Compliance, -8 dB EVM RMS power over TX packet	-	17.6	-	dBm
54 Mbps OFDM (802.11g) TX Output Power	54 Mbps OFDM, 802.11(g) Mask Compliance, -25 dB EVM RMS power over TX packet	-	12.6	-	dBm
6.5 Mbps OFDM (802.11n) TX Output Power	6.5 Mbps OFDM, 802.11(n) Mask Compliance, -5 dB EVM RMS power over TX packet	-	17.7	-	dBm
65 Mbps OFDM (802.11n) TX Output Power	65 Mbps OFDM, 802.11(n) Mask Compliance, -28 dB EVM RMS power over TX packet	-	9.5	-	dBm

Table 10 WLAN Transmitter RF Characteristics

The information in this document is subject to change without notice.

WLAN Receiver Characteristics
(TA=25°C, VBAT=3.6 V) [1]

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps CCK (802.11b) RX Sensitivity	8% PER	-	-97	-	dBm
11 Mbps CCK (802.11b) RX Sensitivity	8% PER	-	-89	-	dBm
9 Mbps OFDM (802.11g) RX Sensitivity	10% PER	-	-90	-	dBm
54 Mbps OFDM (802.11g) RX Sensitivity	10% PER	-	-76	-	dBm
6.5 Mbps OFDM (802.11n) RX Sensitivity	10% PER	-	-91	-	dBm
65 Mbps OFDM (802.11n) RX Sensitivity	10% PER	-	-73	--	dBm
11 Mbps CCK (802.11b) RX Overload Level	8% PER	-	-	-10	dBm
6 Mbps OFDM (802.11g) RX Overload Level	10% PER	-	-	-20	dBm
54 Mbps OFDM (802.11g) RX Overload Level	10% PER	-	-	-20	dBm
65 Mbps OFDM (802.11n) RX Overload Level	10% PER	-	-	-20	dBm

[1] Up to 2 dB degradation at Channel 13 for 11g/n modes and up to 2 dB degradation at Channel 14 for 11b/g/n modes.

Table 11 WLAN Receiver RF Characteristics

Bluetooth RF Characteristics

Bluetooth Transmitter GFSK and EDR Characteristics, Class 1.5
(TA=25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Bluetooth Spec	Unit
GFSK RF Output Power		-	9.5	-	-	dBm
EDR RF Output Power		-	7	-		dBm
Power Control Step Size		2	4	8	2-8	dB
EDR Relative Power		-2		1	-4/+1	dB

Table 12 Bluetooth Transmitter RF Characteristics

Bluetooth Receiver Characteristics
(TA=25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Bluetooth Spec	Unit
GFSK Sensitivity	BER=0.1%	-	-92	-	-70	dBm
EDR 2 Mbps Sensitivity	BER=0.01%	-	-91	-	-70	dBm
EDR 3 Mbps Sensitivity	BER=0.01%	-	-82	-	-70	dBm
GFSK Maximum Input Level	BER=0.1%	-	-5	-	-20	dBm
EDR 2 Maximum Input Level	BER=0.1%	-	-10	-	-	dBm
EDR 3 Maximum Input Level	BER=0.1%	-	-10	-	-	-

Table 13 Bluetooth Receiver RF Characteristics

WLAN POWER-UP SEQUENCE

The following sequence describes device power-up from shutdown. Only the WLAN Core is enabled; the Bluetooth and FM cores are disabled.
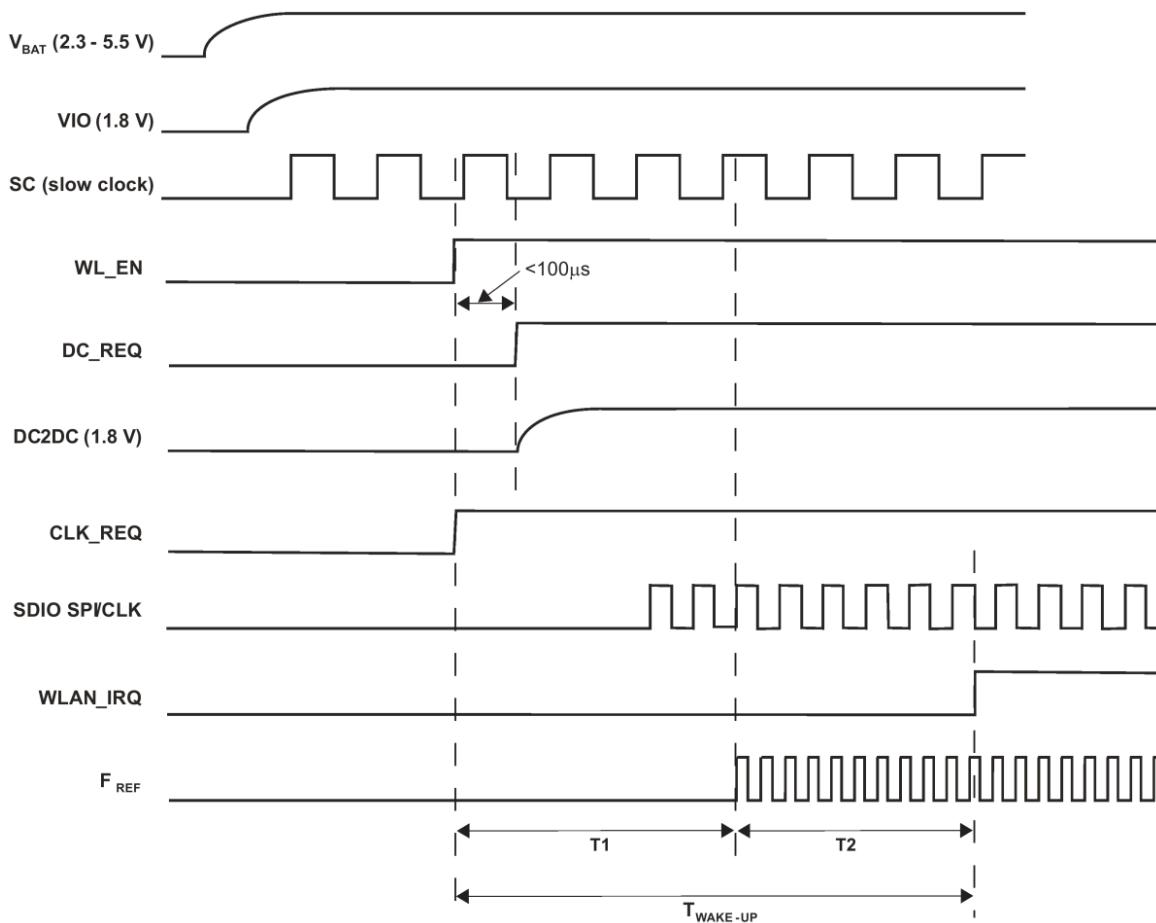

Figure 3 TiWi-R2 Power-up Sequence Requirements

1. No signals are allowed on the IO pins if no IO power is supplied, because the IOs are not 'fail safe'. Exceptions are CLK_REQ_OUT, SLOWCLK, XTALP, and AUD_xxx, which are failsafe and can tolerate external voltages with no VDDS and DC2DC".

2. VBAT, VIO, and SLOWCLK must be available before WL_EN.

3. Twakeup = T1 + T2

The duration of T1 is defined as the time from WL_EN=high until F_{REF} is valid for the SoC. T1=~55ms

The duration of T2 depends on:
– Operating system
– Host enumeration for the SDIO/WSPI
– PLL configuration
– Firmware download
– Releasing the core from reset
– Firmware initialization

WLAN POWER-DOWN SEQUENCE
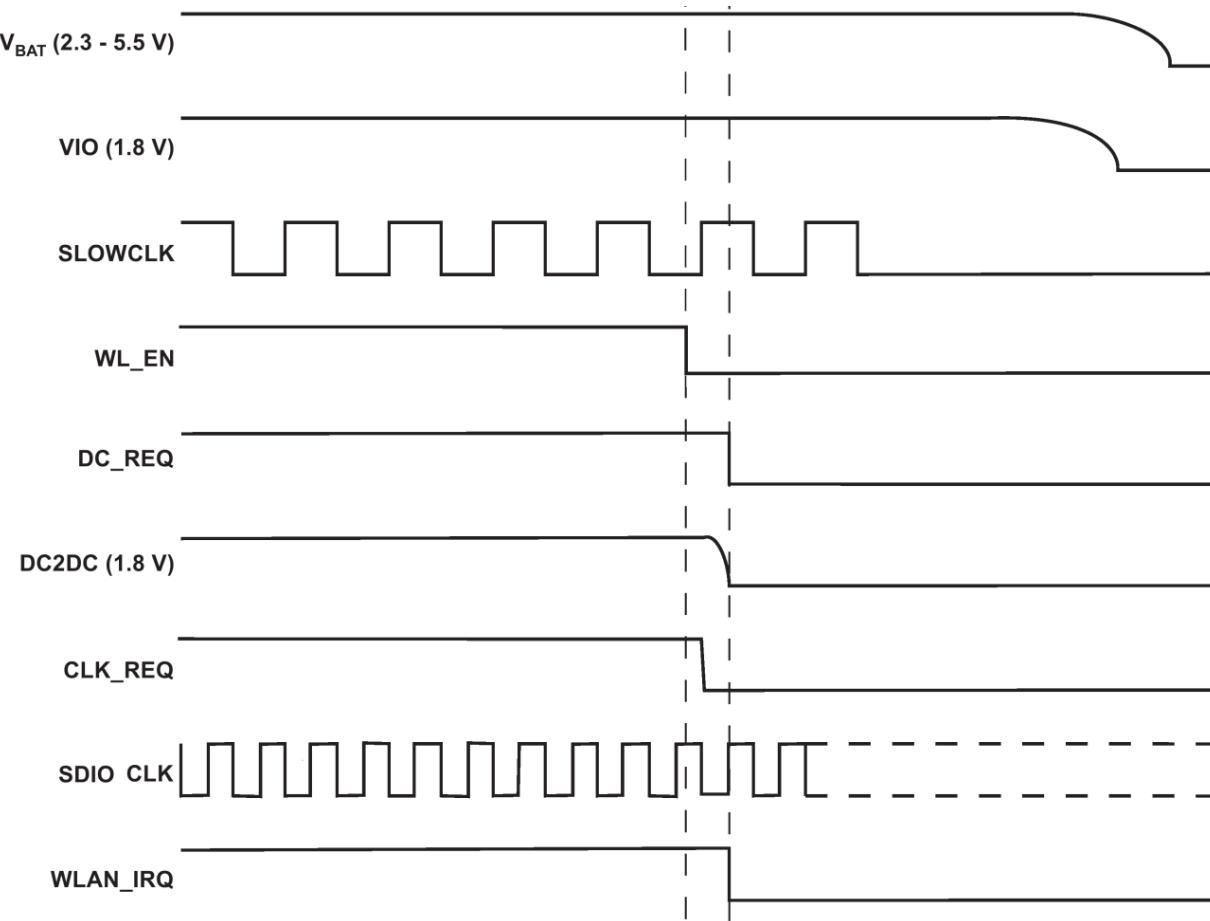
Notes:
1. The DC2DC(1.8V) signal can be monitored on BT_FUNC2 Module Pin (#41)
2. DC_REQ and CLK_REQ are internal signals shown for reference only

Figure 4 TiWi-R2 Module Power-down Sequence Requirements

1. DC_REQ will go low only if WLAN is the only core working. Otherwise if another core is working (e.g BT) it will stay high.

2. CLK_REQ will go low only if WLAN is the only core working. Otherwise if another core is working and using the F_{REF} (e.g BT) it will stay high.

3. If WLAN is the only core that is operating, WL_EN must remain de-asserted for at least 64 sec before it is re-asserted.

BLUETOOTH POWER-UP SEQUENCE

The following sequence describes device power up from shutdown. Only the Bluetooth core is enabled; the WLAN core is disabled.
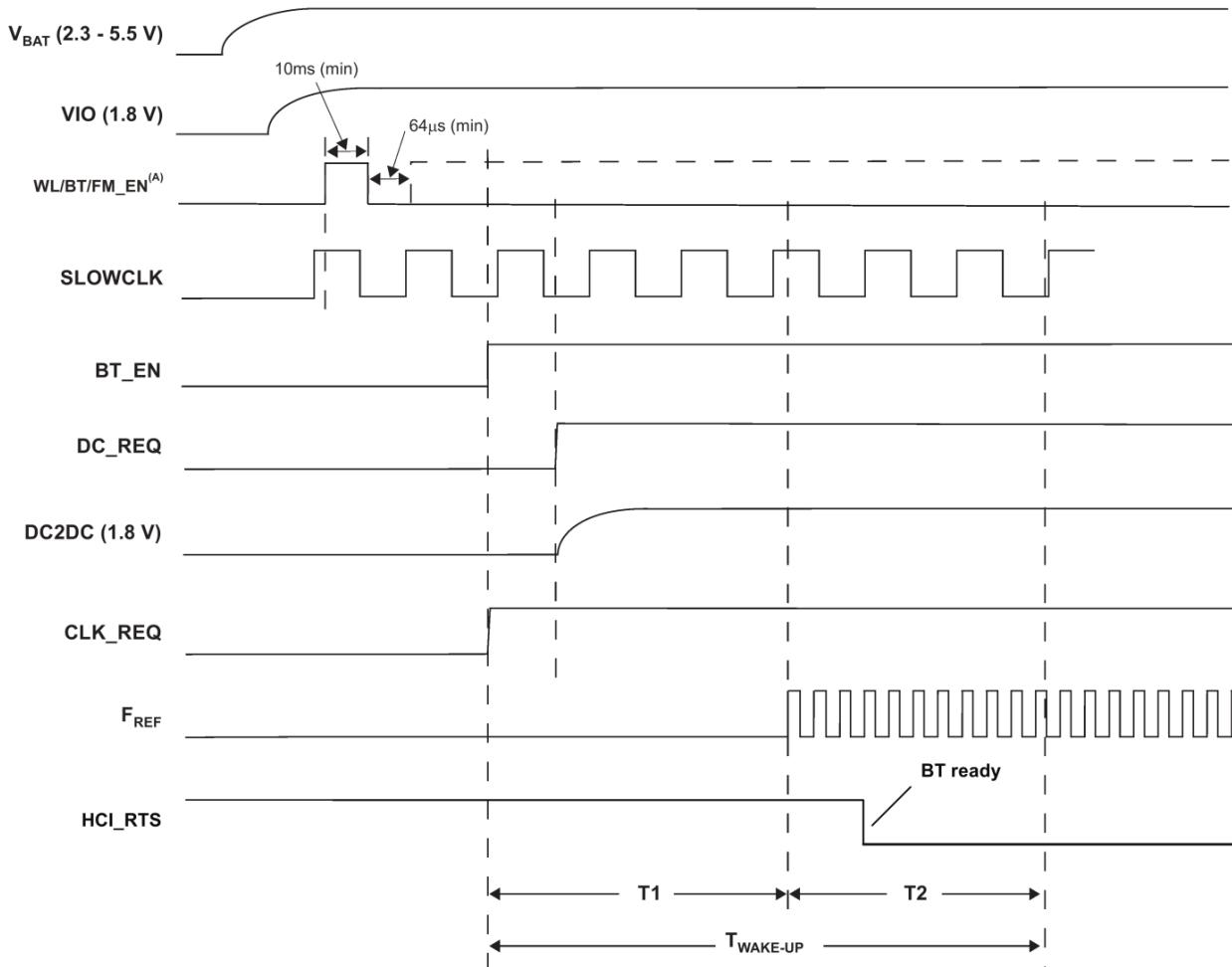

Notes:
1.   (A) After this sequence is completed, the device is in the low VIO-leakage state while in shutdown
2.   The DC2DC(1.8V) signal can be monitored on BT_FUNC2 Module Pin (#41)
3.   DC_REQ, CLK_REQ, and F_{REF} are internal signals shown for reference only

Figure 5 Bluetooth Power-up Sequence

Power up requirements:

1.   No signals are allowed on the IO pins if no IO power supplied, because the IOs are not 'failsafe'. Exceptions are CLK_REQ_OUT, SLOWCLK, XTALP, and AUD_xxx, which are failsafe and can tolerate external voltages with no VDDS and DC2DC.

2.   VDDS and SLOWCLK must be stable before releasing BT_EN.

3.   Fast clock must be stable maximum 55 ms after BT_EN goes HIGH.

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BLUETOOTH POWER-DOWN SEQUENCE
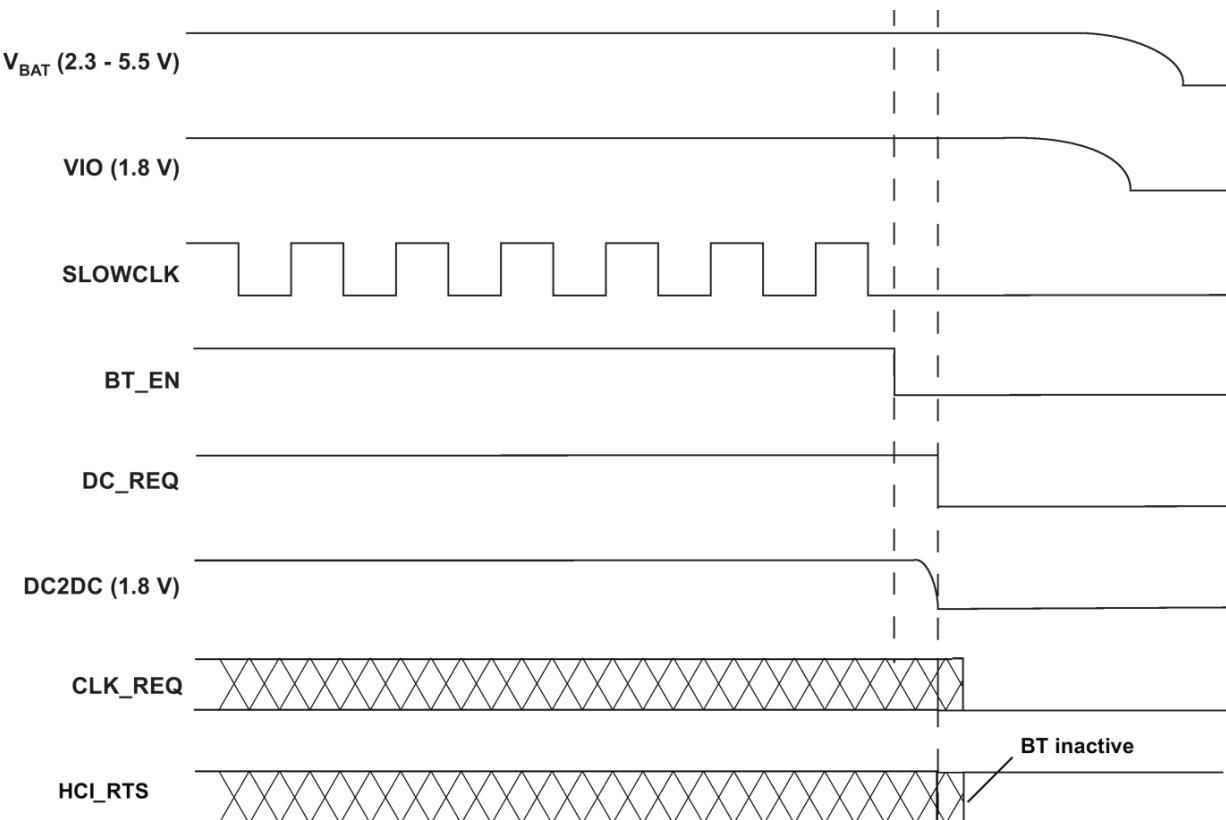
Notes:
1. The DC2DC(1.8V) signal can be monitored on BT_FUNC2 Module Pin (#41)
2. DC_REQ and CLK_REQ are internal signals shown for reference only

Figure 6 Bluetooth Power-down Sequence

The TiWi-R2 module indicates completion of Bluetooth power up sequence by asserting HCI_RTS low. This occurs up to 100 ms after BT_EN goes high.

ENABLE SCHEME

The module has 3 enable pins, one for each core: WL_EN, and BT_EN and FM_EN. Presently, there are 2 modes of active operation now supported: WLAN and Bluetooth. It is recommended that the FM_EN pin be grounded to disable the FM section. It is also recommended that the FM section be disabled by Bluetooth HCI commands.

1. Each core is operated independently by asserting each signal EN to Logic '1'. In this mode it is possible to control each core asynchronously and independently.

2. Bluetooth mode operation. WLAN will be operated through WL_EN asynchronously and independently of Bluetooth.

IRQ OPERATION

1. The default state of the WLAN_IRQ prior to firmware initialization is 0.

2. During firmware initialization, the WLAN_IRQ is configured by the SDIO module; a WLAN_IRQ changes its state to 1.

3. A WLAN firmware interrupt is handled as follows:

    a. The WLAN firmware creates an Interrupt-to-Host, indicated by a 1-to-0 transition on the WLAN_IRQ line (host must be configured as active-low or falling-edge detect).

    b. After the host is available, depending on the interrupt priority and other host tasks, it masks the firmware interrupt. The WLAN_IRQ line returns to 1 (0-to-1 transition on the WLAN_IRQ line).

    c. The host reads the internal register status to determine the interrupt sources - the register is cleared after the read.

    d. The host processes in sequence all the interrupts read from this register

    e. The host unmasks the firmware interrupts.

4. The host is ready to receive another interrupt from the WLAN device.

SLOW (32 KHZ) CLOCK SOURCE REQUIREMENTS

The slow clock is always supplied from an external source. It is input on the SLOW_CLK pin, and can be a digital signal in the range of VIO only. For slow clock frequency and accuracy refer to **Table 14**. The external slow clock must be stable before the system exits from shut down mode.

Parameter [1]	Condition	Symbol	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy	WLAN, BT				+/-250	ppm
Input transition time T_r/T_f – 10% to 90%		T_r/T_f			100	ns
Frequency input duty cycle			30	50	70	%
Input voltage limits	Square wave, DC coupled	VIH	0.65 x VIO		VIO	V_{peak}
		VIL	0		0.35 x VIO	
Input impedance			1			MΩ
Input capacitance					5	pF
Rise and fall time					100	ns
Phase noise	1 kHz				-125	dBc/Hz

Table 14 Slow Clock Source Requirements

[1] Slow clock is a fail safe input

BLUETOOTH HCI UART
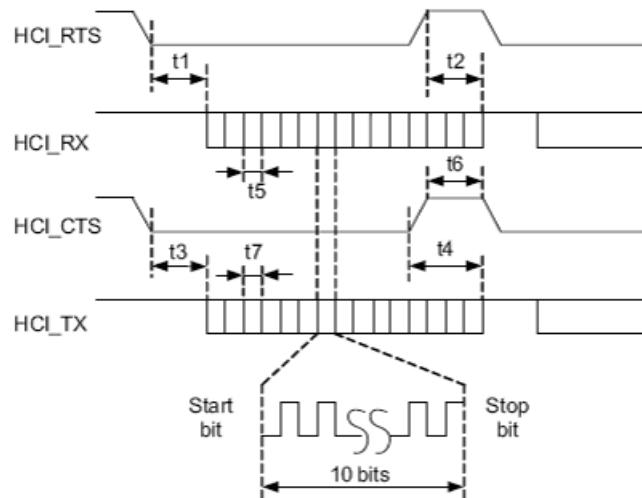
Figure 7 Bluetooth UART Timing

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate	Most rates[1]	37.5		4000	kbps
t5, t7	Baud rate accuracy	Receive/Transmit			−2.5 to 1.5	%
t3	CTS low to TX_DATA on		0	2		μs
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		μs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte
tb	Bit width (Jitter)		See application note[1]			% relative to ideal bit width

(1) Some exceptions: e.g. for 19.2-MHz max baud rate = 3.84 kbps.

Table 15 Bluetooth UART Timing
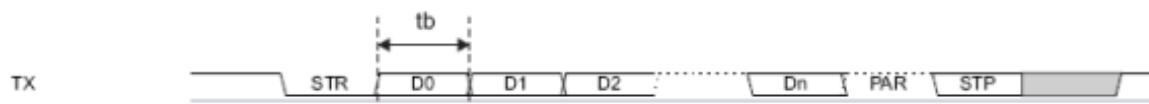
Figure 8 Bluetooth UART Data Frame

Symbol	Description
STR	Start bit
D0...Dn	Data bits (LSB first)
PAR	Parity bit (optional)
STP	Stop bit

Table 16 Bluetooth UART Data Frame

BLUETOOTH AUDIO CODEC INTERFACE

Overview

The CODEC interface is a fully dedicated programmable serial port that provides the logic to interface to several kinds of PCM or I2S codecs. The interface supports:
- Two voice channels
- Master / slave modes
- Coding schemes: μ-Law, A-Law, Linear, Transparent
- Long & short frames
- Different data sizes, order and positions
- UDI profile
- High rate PCM interface for EDR
- Enlarged interface options to support a wider variety of Codecs
- PCM bus sharing

PCM Hardware Interface

The PCM interface is one implementation of the codec interface. It contains the following four lines:
- Clock--configurable direction (input or output)
- Frame Sync--configurable direction (input or output)
- Data In--Input
- Data Out--Output/Hi-Z

The WL1271 device can be either the master of the interface where it generates the clock and the framesync signals, or slave where it receives these two signals. The PCM interface is fully configured by means of a VS command.

For slave mode, clock input frequencies of up to 16MHz are supported. At clock rates above 12MHz, the maximum data burst size is 32 bits.

For master mode, the WL1271 can generate any clock frequency between 64kHz and 4.096MHz.

Data Format

The data format is fully configurable:
- The data length can be from 8 to 320 bits, in 1-bit increments, when working with two channels, or up to 640 bits when using 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable with 1-clock (bit) resolution, and can be set independently (relative to the edge of the Frame Sync signal) for each channel.
- The Data_In and Data_Out bit order can be configured independently. For example; Data_In can start with MSB while Data_Out starts with LSB. Each channel is separately configurable. The inverse bit order (i.e. LSB first) is supported only for sample sizes up to 24 bits.
- The data in and data out size do not necessarily have to be the same length.
- The Data_Out line is configured as a 'high-Z' output between data words. Data_Out can also be set for permanent high-Z, irrespective of data out. This allows the WL1271 to be a bus slave in a multi-slave PCM environment. At power up, Data_Out is configured as high-Z.

The information in this document is subject to change without notice.

Frame-Idle Period

The CODEC interface has the capability for frame-idle periods, where the PCM clock can "take a break" and become '0' at the end of the PCM frame, after all data has been transferred.

The WL1271 supports frame-idle periods both as master and slave of the PCM bus.

When WL1271 is the master of the interface, the frame-idle period is configurable. There are 2 configurable parameters:
- Clk_Idle_Start - Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes '0'.
- Clk_Idle_End – Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

e.g. For PCM clock rate = 1MHz, frame sync period = 10kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90.

Between each two-frame sync there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts 90-60=30 clock cycles. This means that the idle period ends 100-90=10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.
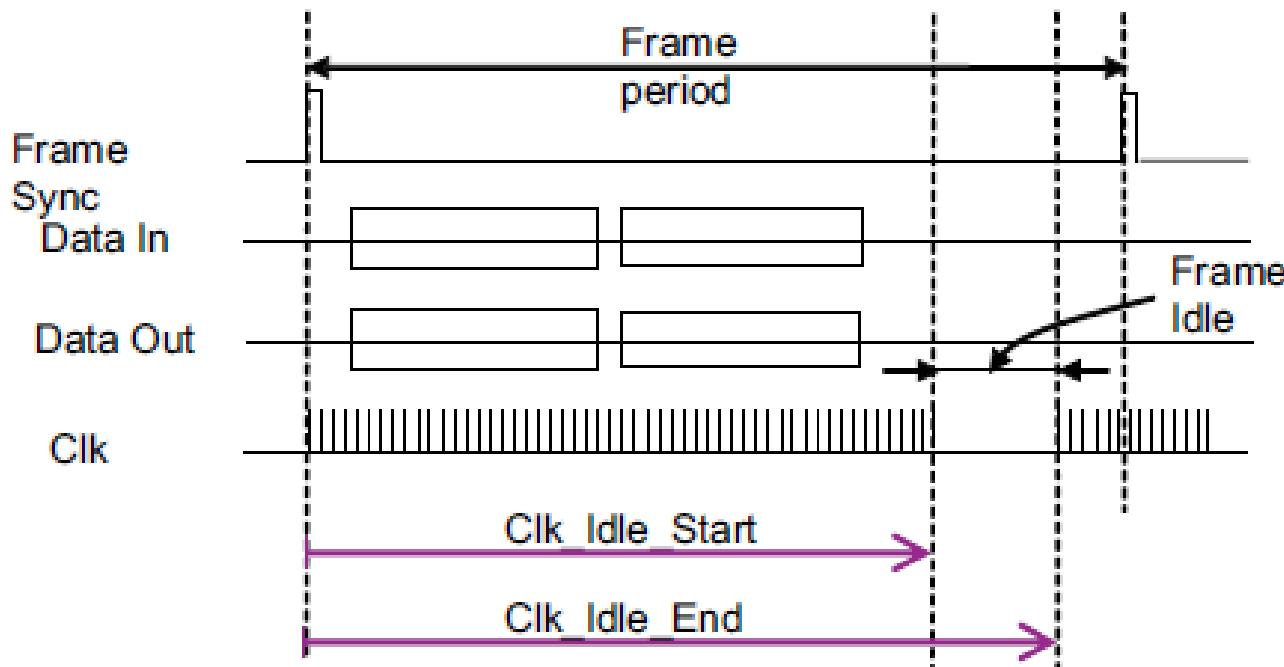

Figure 9 Frame Idle Period

Clock-Edge Operation

The CODEC interface of the WL1271 can work on the rising or the falling edge of the clock. It also has the ability to sample the frame sync and the data at inversed polarity.

The following diagram shows the operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame-sync signal is updated (by the codec) on the falling clock edge and therefore is sampled (by the WL1271) on the next rising clock. The data from the codec is sampled (by the WL1271) on the clock falling edge.
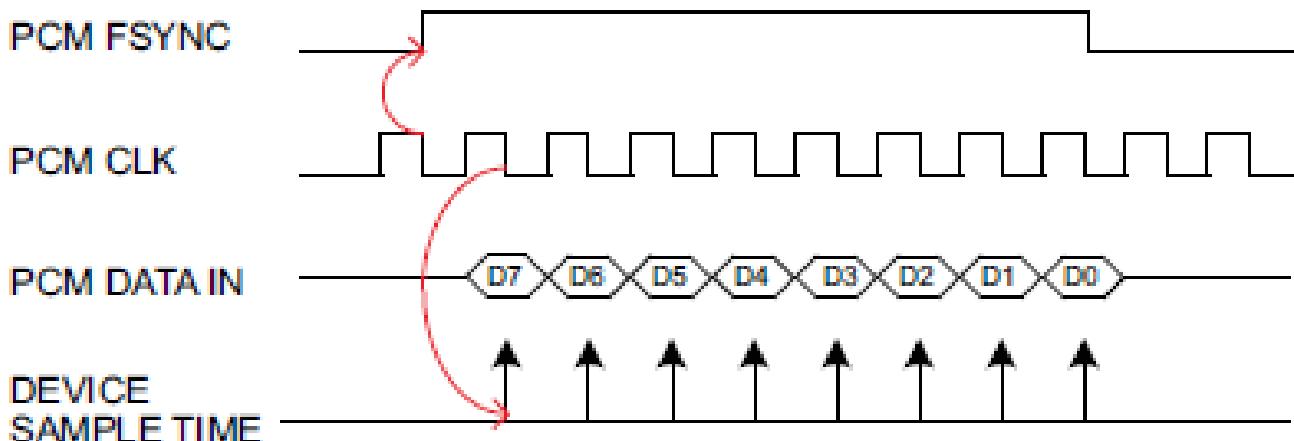
Figure 10 Negative Clock Edge PCM Operation

Two Channel PCM Bus Example

In the following figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame. (FT stands for Frame Timer)
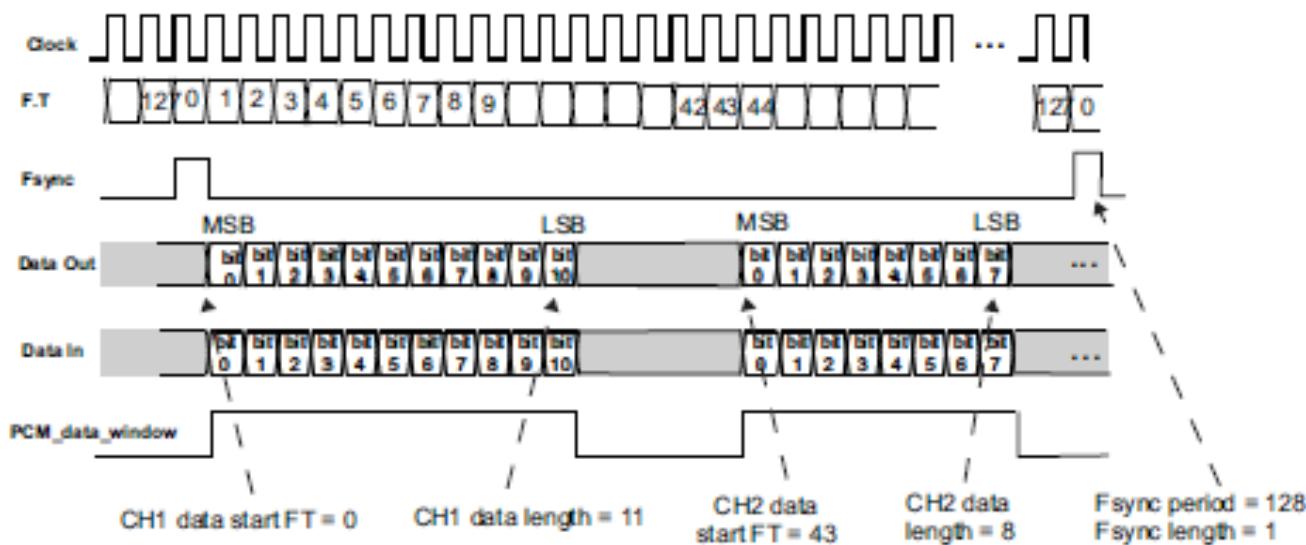

Figure 11 2 Channels PCM Bus Timing

The information in this document is subject to change without notice.

Audio Encoding

The WL1271 CODEC interface can use one of four audio coding patterns:
- A-Law (8-bit)
- µ-Law (8-bit)
- Linear (8 or 16-bit)
- Transparent

Improved Algorithm for Lost Packets

The WL1271 features an improved algorithm for improving voice quality when received voice data packets go missing. There are two options:
- Repeat the last sample – possible only for sample sizes up to 24 bits. For sample sizes >24 bits, the last byte is repeated.
- Repeat a configurable sample of 8-24 bits (depends on the real sample size), in order to simulate silence (or anything else) in the PCM bus. The configured sample is written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

BLUETOOTH PCM CLOCK MISMATCH HANDLING

In BT RX, the WL1271 receives RF voice packets and writes these to the CODEC I/F. If the WL1271 receives data faster than the CODEC I/F output allows, an overflow occurs. In this case, the WL1271 BT function has 2 possible behavior modes: 'allow overflow' and 'don't allow overflow'.

- If overflow is allowed, the WL1271 BT function continues receiving data and overwrites any data not yet sent to the CODEC.
- If overflow is not allowed, RF voice packets received when buffer is full, are discarded

The information in this document is subject to change without notice.

BLUETOOTH INTER-IC SOUND (I2S)

The WL1271 can be configured as an Inter-IC Sound (I2S) serial interface to an I2S CODEC device. In this mode, the WL1271 audio CODEC interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 is used for the left channel audio data and time slot 1 for the right channel audio data. Each time slot is configurable up to 40 serial clock cycles in length and the frame is configurable up to 80 serial clock cycles in length.

UDI SUPPORT

The UDI profile defines the protocols and procedures that are used by devices implementing UDI for the 3G mobile phone systems, such as devices with Bluetooth connections to a 3G Handset, communicating via video phone over a 3G network. Up to 2 channels of UDI data can be supported. The data is transferred via the CODEC interface using transparent mode, and is sent out using eSCO EV4 Bluetooth packets (EV5 is also selectable).

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SDIO INTERFACE TIMING

PARAMETER		MIN	MAX	UNIT
t_{CR}	Delay time, assign relative address or data transfer mode	Read-command CMD valid to card-response CMD valid	2	64	Clock cycles
t_{CC}	Delay time, CMD command valid to CMD command valid		58		Clock cycles
t_{RC}	Delay time, CMD response valid to CMD command valid		8		Clock cycles
t_{AC}	Access time, CMD command valid to SD3–SD0 read data valid		2		Clock cycles

Table 17 SDIO Interface Read (see Figure 12)
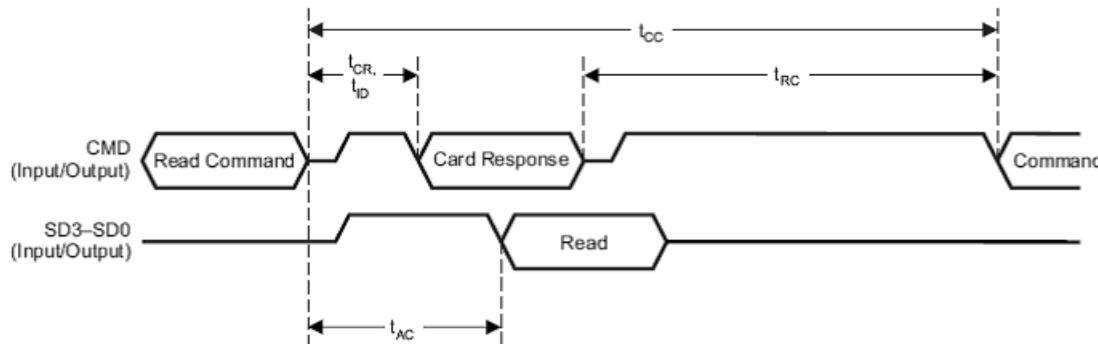
Figure 12 SDIO Single Block Read

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, CMD card response invalid to SD3–SD0 write data valid	2		Clock cycles
t_{d2}	Delay time, SD3–SD0 write data invalid end to CRC status valid	2	2	Clock cycles

Table 18 SDIO Interface Write (see Figure 13)
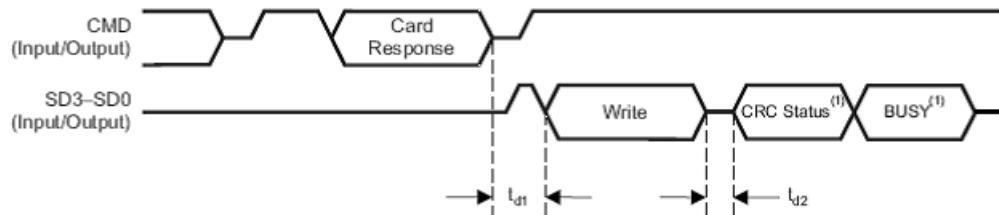
(1) CRC status and busy waveforms are only for data line 0. Data lines 1–3 are N/A. The busy waveform is optional, and may not be present.

Figure 13 SDIO Single Block Write

The information in this document is subject to change without notice.

SDIO CLOCK TIMING

Over Recommended Operating Conditions

Note: all timing parameters are indicated for the maximum Host-interface clock frequency.

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	$C_L \leq 30$ pF	0	26	MHz
DC	Low/high duty cycle	$C_L \leq 30$ pF	40	60	%
t_{TLH}	Rise time, CLK	$C_L \leq 30$ pF		4.3	ns
t_{THL}	Fall time, CLK	$C_L \leq 30$ pF		3.5	ns
t_{ISU}	Setup time, input valid before CLK $\uparrow$	$C_L \leq 30$ pF	4		ns
t_{IH}	Hold time, input valid after CLK $\uparrow$	$C_L \leq 30$ pF	5		ns
t_{ODLY}	Delay time, CLK$\downarrow$ to output valid	$C_L \leq 30$ pF	2	12	ns

Table 19 SDIO Clock Timing
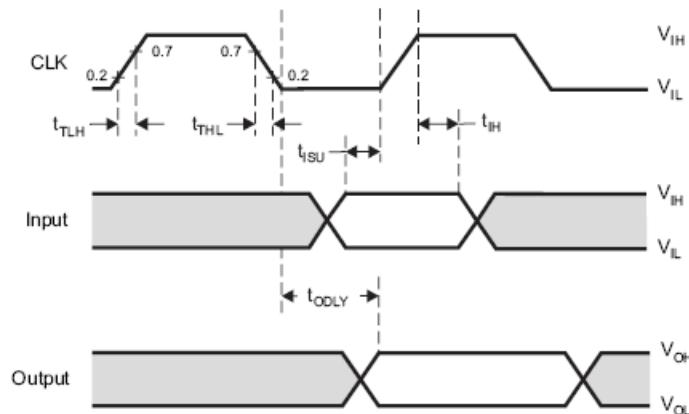
Figure 14 SDIO Clock Timing

SOLDERING RECOMMENDATIONS

Recommended Reflow Profile for Lead Free Solder
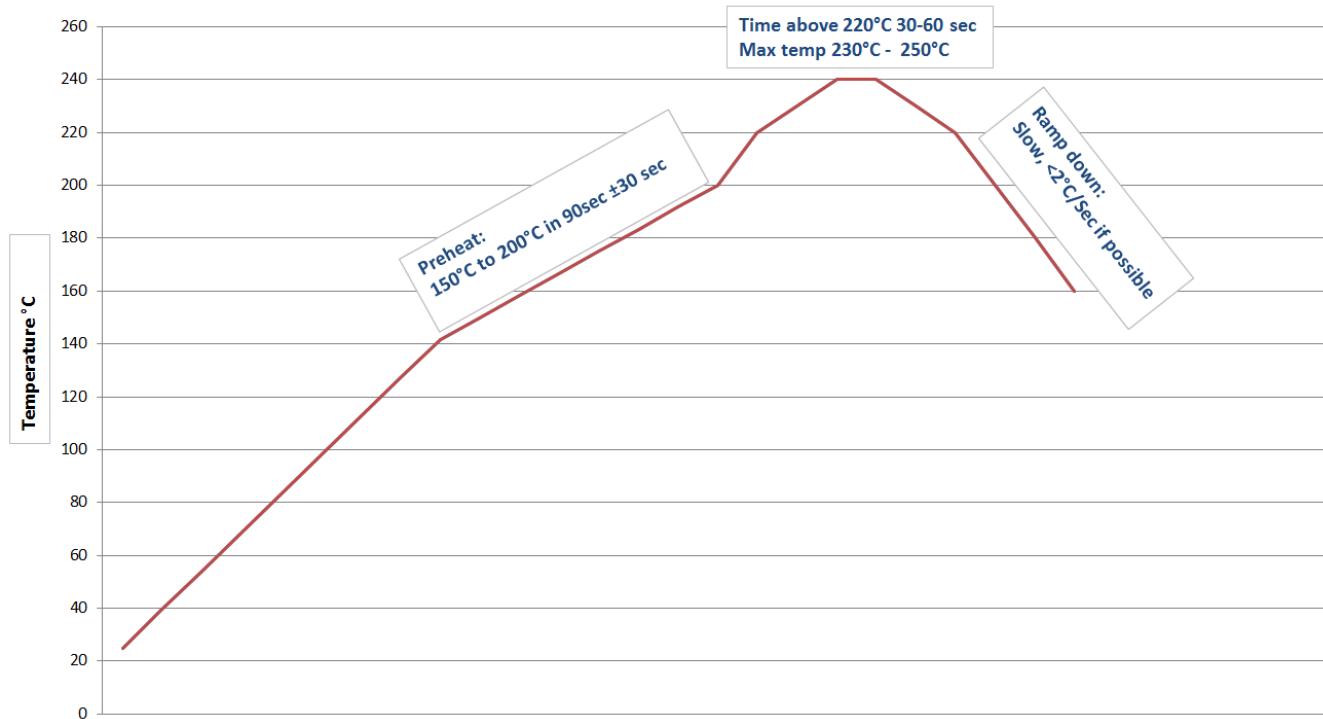
Note: The quality of solder joints on the castellations ('half vias') where they contact the host board should meet the appropriate IPC Specification. See IPC-A-610-D Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations."

Figure 15 Reflow Profile

The information in this document is subject to change without notice.

CLEANING

In general, cleaning populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

OPTICAL INSPECTION

After soldering the Module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads or vias.

REWORK

The module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

> **Never attempt rework on the module itself, e.g., replacing individual components. Such actions will terminate warranty coverage.**

SHIPPING, HANDLING, AND STORAGE

Shipping

TiWi-R2 modules are delivered in trays of 100 or reels of 1,000.

Handling

The TiWi-R2 modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40ºC and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX.

Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

The information in this document is subject to change without notice.

Repeating Reflow Soldering

> **Only a single reflow soldering process is recommended for host boards.**

AGENCY CERTIFICATIONS

FCC ID: TFB-TIWI1-01, 15.247

IC ID: 5969A-TIWI101, RSS 210

CE: Compliant to standards EN 60950-1, EN 300 328, and EN 301 489

Giteki: 209-J00157

SAR: This wireless mobile and/or portable device has been shown to be compliant for localized specific absorption rate (SAR) for uncontrolled environment/general exposure limits specified in ANSI/IEEE Std. C95.1-1999 and had been tested in accordance with the measurement procedures specified in IEEE 1528-2003, OET Bulletin 65 Supp. C, RSS-102 and Safety Code 6.

AGENCY STATEMENTS

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC CAUTION: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Industry Canada Statements

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

This device has been designed to operate with the antenna(s) listed below, and having a maximum gain of 4.3 dBi (LSR Dipole), -0.6dBi (Ethertronics Prestta), and 3.0dBi (Taoglas Flexible Dipole). Antennas not included in this list or having a gain greater than 4.3 dBi, -0.6dBi, and 3.0dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

List of all Antennas Acceptable for use with the Transmitter

1) LSR 001-0001 center-fed dipole antenna and LSR 080-0001 U.FL to Reverse Polarity SMA connector cable.
2) Ethertronics Prestta 1000423 and Johnson Emerson U.FL to U.FL coaxial cable 415-0088-150.
3) Taoglas FXP831.07.0100C flexible dipole antenna with integrated cable and U.FL connector.

L'opération est soumise aux deux conditions suivantes: (1) cet appareil ne peut pas provoquer d'interférences et (2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

Pour réduire le risque d'interférence aux autres utilisateurs, le type d'antenne et son gain doiventêtre choisis de manière que la puissance isotrope rayonnée équivalente (PIRE) ne dépasse pascelle permise pour une communication réussie.

Cet appareil a été conçu pour fonctionner avec l'antenne (s) ci-dessous, et ayant un gain maximum de 4,3 dBi (LSR dipôle),-0.6dBi (Ethertronics Prestta), et 3.0dBi (Taoglas Flexibles Dipôle). Antennes pas inclus dans cette liste ou ayant un gain supérieur à 4,3 dBi, 0.6dBi, et 3.0dBi sont strictement interdits pour une utilisation avec cet appareil. L'impédance d'antenne requise est de 50 ohms.

Liste de toutes les antennes acceptables pour une utilisation avec l'émetteur

1) LSR 001-0001 alimenté par le centre antenne dipôle et LSR 080-0001 U.FL d'inversion de polarité du câble connecteur SMA.
2) Ethertronics Prestta 1000423 et Johnson Emerson U.FL d'un câble coaxial U.FL 415-0088-150.
3) Taoglas FXP831.07.0100C antenne dipôle flexible avec câble intégré et un connecteur U.FL.

OEM RESPONSIBILITIES TO COMPLY WITH FCC AND INDUSTRY CANADA REGULATIONS

The TiWi-R2 Module has been certified for integration into products only by OEM integrators under the following conditions:

This device is granted for use in Mobile only configurations in which the antennas used for this transmitter must be installed to provide a separation distance of at least 20cm from all person and not be co-located with any other transmitters except in accordance with FCC and Industry Canada multi-transmitter product procedures.

As long as the two conditions above are met, further transmitter testing will not be required.
However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

> **IMPORTANT NOTE: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC and Industry Canada authorizations are no longer considered valid and the FCC ID and IC Certification Number cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC and Industry Canada authorization.**

Le module de TiWi-R2 a été certifié pour l'intégration dans des produits uniquement par des intégrateurs OEM dans les conditions suivantes:

Ce dispositif est accordé pour une utilisation dans des configurations mobiles seul dans lequel les antennes utilisées pour cet émetteur doit être installé pour fournir une distance de séparation d'au moins 20cm de toute personne et ne pas être colocalisés avec les autres émetteurs, sauf en conformité avec la FCC et de l'Industrie Canada, multi-émetteur procédures produit.

Tant que les deux conditions précitées sont réunies, les tests de transmetteurs supplémentaires ne seront pas tenus. Toutefois, l'intégrateur OEM est toujours responsable de tester leur produit final pour toutes les exigences de conformité supplémentaires requis avec ce module installé (par exemple, les émissions appareil numérique, les exigences de périphériques PC, etc.)

> **NOTE IMPORTANTE: Dans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou de co-implantation avec un autre émetteur), puis la FCC et Industrie autorisations Canada ne sont plus considérés comme valides et l'ID de la FCC et IC numéro de certification ne peut pas être utilisé sur la produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'un distincte de la FCC et Industrie Canada l'autorisation.**

The information in this document is subject to change without notice.

OEM LABELING REQUIREMENTS FOR END-PRODUCT

The TiWi-R2 module is labeled with its own FCC ID and IC Certification Number. The FCC ID and IC certification numbers are not visible when the module is installed inside another device, as such the end device into which the module is installed must display a label referring to the enclosed module. The final end product must be labeled in a visible area with the following:

"**Contains Transmitter Module FCC ID: TFB-TIWI1-01"**

"**Contains Transmitter Module IC: 5969A-TIWI101"**

or

"**Contains FCC ID: TFB-TIWI1-01"**

"**Contains IC: 5969A-TIWI101"**

The OEM of the TiWi-R2 Module must only use the approved antenna(s) listed above, which have been certified with this module.

Le module de TiWi-R2 est étiqueté avec son propre ID de la FCC et IC numéro de certification. L'ID de la FCC et IC numéros de certification ne sont pas visibles lorsque le module est installé à l'intérieur d'un autre appareil, comme par exemple le terminal dans lequel le module est installé doit afficher une etiquette faisant référence au module ci-joint. Le produit final doit être étiqueté dans un endroit visible par le suivant:

"**Contient Module émetteur FCC ID: TFB-TIWI1-01"**
"**Contient Module émetteur IC: 5969A-TIWI101"**

ou

"**Contient FCC ID: TFB-TIWI1-01"**
"**Contient IC: 5969A-TIWI101"**

L'OEM du module TiWi-R2 ne doit utiliser l'antenne approuvée (s) ci-dessus, qui ont été certifiés avec ce module.

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OEM END PRODUCT USER MANUAL STATEMENTS

The OEM integrator should not provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

The user manual for the end product must include the following information in a prominent location:

This device is granted for use in Mobile only configurations in which the antennas used for this transmitter must be installed to provide a separation distance of at least 20cm from all person and not be co-located with any other transmitters except in accordance with FCC and Industry Canada multi-transmitter product procedures.

Other user manual statements may apply.

L'intégrateur OEM ne devrait pas fournir des informations à l'utilisateur final en ce qui concerne la façon d'installer ou de retirer ce module RF ou modifier les paramètres RF connexes dans le manuel utilisateur du produit final.

Le manuel d'utilisation pour le produit final doit comporter les informations suivantes dans unendroit bien en vue:

Ce dispositif est accordé pour une utilisation dans des configurations mobiles seule dans laquelle les antennes utilisées pour cet émetteur doit être installé pour fournir une distance de séparation d'au moins 20cm de toute personne et ne pas être co-localisés avec les autres émetteurs, sauf en conformité avec FCC et Industrie Canada, multi-émetteur procédures produit.

Autres déclarations manuel de l'utilisateur peuvent s'appliquer.

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EUROPE

CE Notice

This device has been tested and certified for use in the European Union. See the Declaration of Conformity (DOC) for specifics.

If this device is used in a product, the OEM has responsibility to verify compliance of the final product to the EU standards. A Declaration of Conformity must be issued and kept on file as described in the Radio and Telecommunications Terminal Equipment (R&TTE) Directive.

The 'CE' mark must be placed on the OEM product per the labeling requirements of the Directive.

Declaration of Conformity (DOC)

This DOC can be downloaded from the LSR Wiki.

The information in this document is subject to change without notice.

MECHANICAL DATA
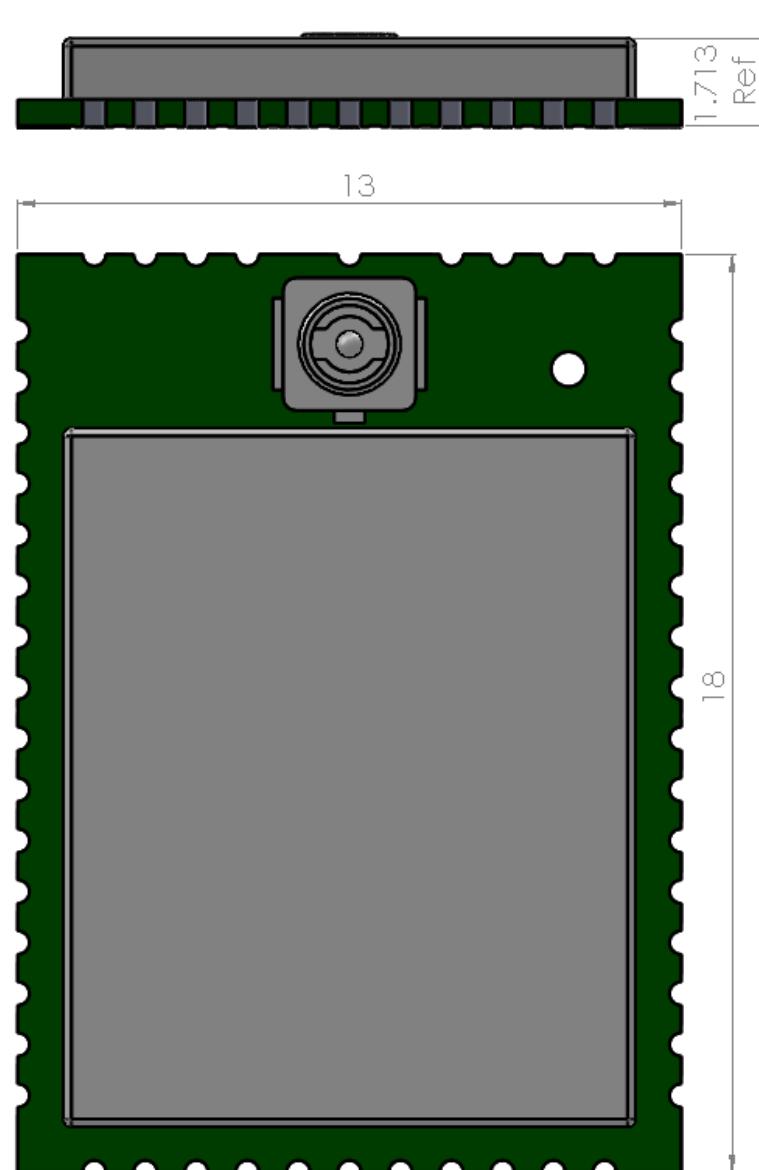
Figure 16 Module Mechanical Dimensions (Maximum Module Height = 1.9 mm)

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DETAIL A (2X SCALE)
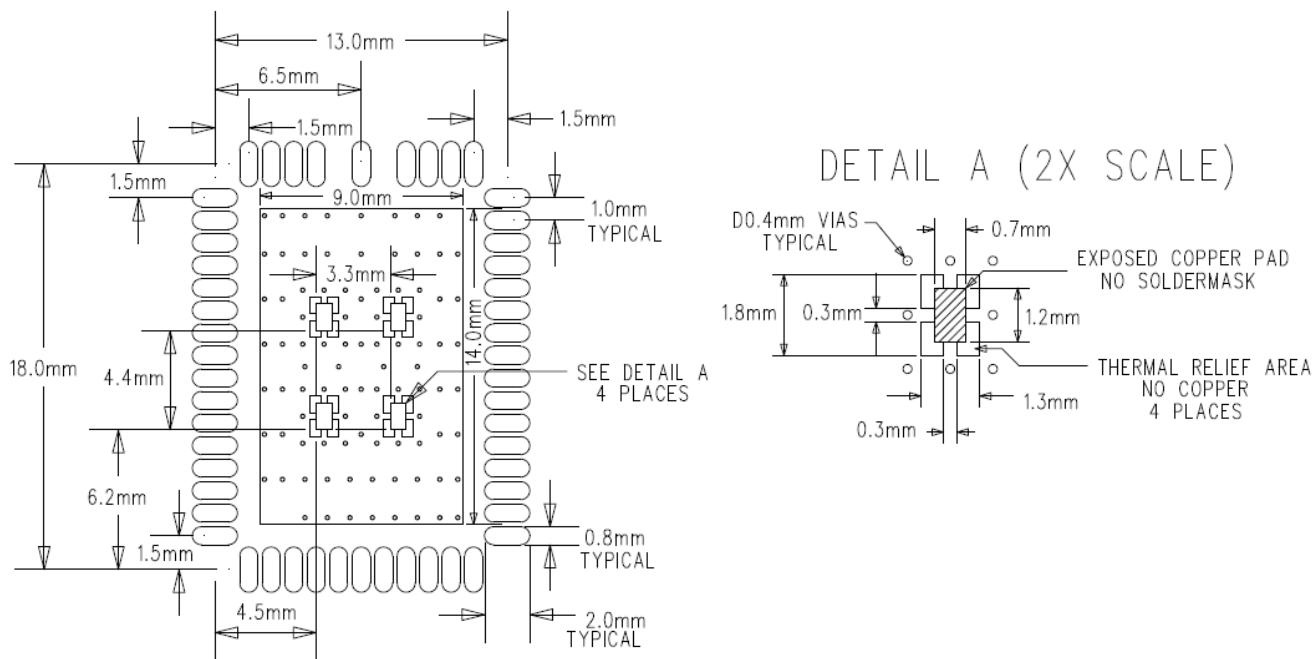
LAYOUT NOTES:
1 — MINIMUM 4—LAYER PCB WITH SECOND LAYER GROUND PLANE
2 — FOUR GROUND PADS BENEATH MODULE TO BE THERMALLY TIED TO
    TOP LAYER GROUND POUR (SEE DETAIL A).
    CONNECT TOP SIDE POUR TO LAYER 2 GROUND PLANE USING AMPLE VIAS.
3 — AVOID LONG ROUTES ON TOP LAYER BENEATH MODULE. VIA FANOUT BENEATH MODULE IS ACCEPTABLE,

Figure 17 TiWi-R2 Recommended PCB Footprint (Top View)

The information in this document is subject to change without notice.

TAPE AND REEL SPECIFICATION

Tape Dimensions

NOTES:
1. DIM in mm.
2. 10 Sprocket Hole Pitch Cumulative Tolerance ± 0.2.
3. Pocket Position Relative to Sprocket Hole Measured as True Position of Pocket, not Pocket Hole
4. A Full Reel contains 1000 Modules

(Module Must Be in this Orientation when Feeding Tape)
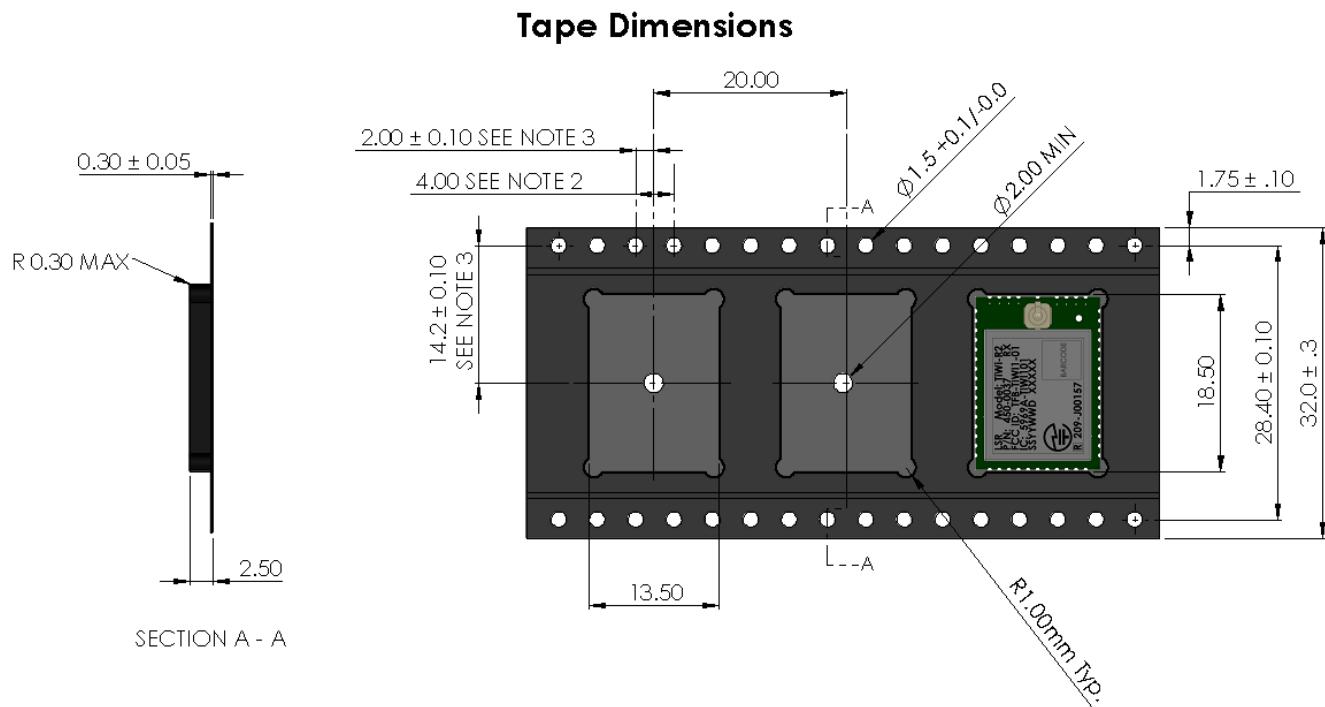
Figure 18 TiWi-R2 Tape and Reel Specification

The information in this document is subject to change without notice.

DEVICE MARKINGS

Rev 0 Devices

WL1271: WL1271A1YFVR PG2.1
Front End: TQM679002A
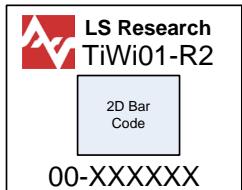
Where 00 = revision
XXXXXX = incremental serial number
2D Barcode Format is Data Matrix Standard

Rev 1 Devices

WL1271: WL1271BYFVR PG3.1
Front End: TQM679002A

- Changed the WL1271 IC to WL1271BYFVR PG3.1.
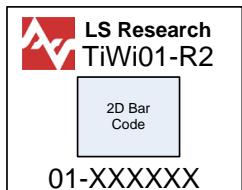
Where 01 = revision
XXXXXX = incremental serial number
2D Barcode Format is Data Matrix Standard

Rev 2 Devices

WL1271: WL1271BYFVR PG3.1
Front End: TQM679002A

- Changed PCB supplier.
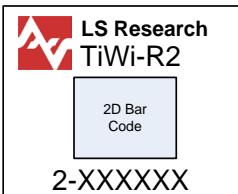
Where 2 = revision
XXXXXX = incremental serial number
2D Barcode Format is Data Matrix Standard

Rev 3 Devices

WL1271: WL1271BYFVR PG3.1
Front End: TQM679002A

- Incorporated PCB DFM improvements.
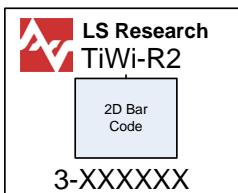
Where 3 = revision
XXXXXX = incremental serial number
2D Barcode Format is Data Matrix Standard

The information in this document is subject to change without notice.

Rev 4 Devices

WL1271: WL1271BYFVR PG3.1
Front End: TQM679002A

- LSR logo changed from red to black.
- Improvements to prevent solder from wicking to bottom pad on module pin 48.
- Switched the locations of the serial number and model name on the label.

LS RESEARCH
4-XXXXXX

2D Bar
Code

Model: TiWi-R2
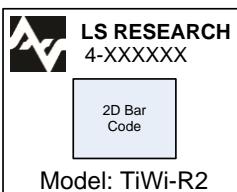
Where 4 = Revision
XXXXXX = incremental serial number
2D Barcode Format is Data Matrix Standard

Rev 5 Devices

WL1271: WL1271BYFVR PG3.1
Front End: TQM679002A

- Improvements in the manufacturing process of the PCB.

LS RESEARCH
5-XXXXXX

2D Bar
Code

Model: TiWi-R2
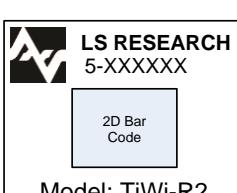
Where 5 = Revision
XXXXXX = incremental serial number
2D Barcode Format is Data Matrix Standard

The information in this document is subject to change without notice.

Rev 6 Devices

WL1271: WL1271BYFVR PG3.1
Front End: TQM679002A

- Updated the label to include FCC, IC, and Giteki EMC marking information.
- Updated the label to include a Date Code.
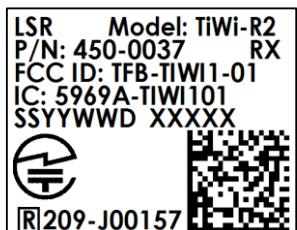
Where RX = Revision X
SSYYWWD = Date Code (YY=Year, WW=Week)
XXXXX = Incremental Serial Number
2D Barcode Format is Data Matrix Standard

CONTACTING LSR

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