



**Migrating to MX25L512E and MX25L1006E  
from MX25L512/512C and MX25L1005/1005C**

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## **1. Introduction**

This application note is the migration guide from the MX25L512/MX25L512C to the MX25L512E, and the MX25L1005/MX25L1005C to the MX25L1006E.

The MX25L512E and MX25L1006E are capable of Dual Output mode (Single Input / Dual Output). In most applications, the MX25L512E and MX25L1006E are backward compatible with the MX25L512/512C and MX25L1005/1005C, respectively, and do not require any firmware or hardware modifications if the application continues to use them in Single I/O mode.

The information provided is based on the data available at the time. The MX25L512E and MX25L1006E datasheets may override this application note if there is a different description for the same specifications in the datasheets.



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## 2. General Features

### 2-1. Feature Comparison

The Dual Output mode (1I/2O) is one of the new features of the MX25L512E and MX25L1006E. The new devices also support clock rates up to 104MHz.

**Table 2-1: Major Feature Comparison**

Parameter/Product		MX25L512 MX25L512C	MX25L512E	MX25L1005 MX25L1005C	MX25L1006E
<b>Technology</b>		150nm	110nm	150nm	110nm
<b>Package</b>		150mil 8SOP 2x3mm 8USON 173mil 8TSSOP	150mil 8SOP 2x3mm 8USON 173mil 8TSSOP	150mil 8SOP 2x3mm 8USON	150mil 8SOP 2x3mm 8USON
<b>Voltage</b>		2.7-3.6V	2.7-3.6V	2.7-3.6V	2.7-3.6V
<b>Interface</b>		x1	x1, 1I/2O	x1	x1, 1I/2O
<b>Clock Rate</b>	<b>Fast Read</b>	85MHz	104MHz	85MHz	104MHz
	<b>Normal Read</b>	33MHz	33MHz	33MHz	33MHz
	<b>DREAD (Dual Output)</b>	--	80MHz	--	80MHz
<b>Page</b>		256 bytes	256 bytes	256 bytes	256 bytes
<b>Sector</b>		4KB	4KB	4KB	4KB
<b>Block</b>		64KB	64KB	64KB	64KB

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**2-2: Performance Comparison**

Table below is the comparison of new product and the former product.

**Table 2-2: Performance Comparison for the MX25L512/512C and MX25L512E Products**

Parameter		MX25L512 MX25L512C	MX25L512E
Clock High/ Low Time@33MHz	tCH	15ns(min.)	13ns(min.)
	tCL	15ns(min.)	13ns(min.)
Program Time	Byte	Not Defined	9us (typ) ; 300us (max)
	Page	1.4ms(typ.) ; 5ms(max.)	1.4ms(typ.) ; 5ms(max.)
Erase Time	Sector(4KB)	60ms(typ.); 120ms (max)	60ms(typ.); 300ms (max)
	Block(64KB)	1s(typ.) ; 2s(max.)	0.7s(typ.) ; 2s(max.)
	Chip	1s(typ.) ; 2s(max.)	0.7s(typ.) ; 2s(max.)
Read ID	tRES1	3us(max.)	8.8us(max.)
	tRES2	1.8us(max.)	8.8us(max.)
CS# Deselect Time	tSHSL	100ns(min.)	Read=15ns(min.); Write=40ns(min)
CS# Active Setup Time	tSLCH	5ns(min.)	7ns(min.)
CS# Not Active Setup Time	tSHCH	5ns(min.)	7ns(min.)
CS# Active Hold Time	tCHSH	5ns(min.)	7ns(min.)
CS# Not Active Hold Time	tCHSL	5ns(min.)	7ns(min.)
VCC Standby Current	ISB1	10uA(max.)	25uA(max.)
Deep Power Down Current	ISB2	5uA(max.)	10uA(max.)
Active Current	ICC1	12mA(max.) @85MHz 4mA(max.) @33MHz	12mA(max.) @104MHz 4mA(max.) @33MHz
	ICC2	15mA (max.)	20mA (max.)
	ICC3	15mA (max.)	15mA (max.)
	ICC4	15mA (max.)	15mA (max.)
	ICC5	15mA (max.)	20mA (max.)



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Table 2-3: Performance Comparison for the MX25L1005/1005C and MX25L1006E

Parameter		MX25L1005 MX25L1005C	MX25L1006E
Clock High/ Low Time@33MHz	tCH	15ns(min.)	13ns(min.)
	tCL	15ns(min.)	13ns(min.)
Program Time	Byte	Not Defined	9us (typ.) ; 300us (max)
	Page	1.4ms(typ.) ; 5ms(max.)	1.4ms(typ.) ; 5ms(max.)
Erase Time	Sector(4KB)	60ms(typ.) ; 120ms(max.)	60ms(typ.); 300ms (max)
	Block(64KB)	1s(typ.) ; 2s(max.)	0.7s(typ.) ; 2s(max.)
	Chip	1s(typ.) ; 2s(max.)	1s(typ.) ; 2s(max.)
Read ID	tRES1	3us(max.)	8.8us(max.)
	tRES2	1.8us(max.)	8.8us(max.)
CS# Deselect Time	tSHSL	100ns(min.)	Read=15ns(min.); Write=40ns(min)
CS# Active Setup Time	tSLCH	5ns(min.)	7ns(min.)
CS# Not Active Setup Time	tSHCH	5ns(min.)	7ns(min.)
CS# Active Hold Time	tCHSH	5ns(min.)	7ns(min.)
CS# Not Active Hold Time	tCHSL	5ns(min.)	7ns(min.)
VCC Standby Current	ISB1	10uA(max.)	25uA(max.)
Deep Power Down Current	ISB2	5uA(max.)	10uA(max.)
Active Current	ICC1	12mA(max.) @85MHz 4mA(max.) @33MHz	12mA(max.) @104MHz 4mA(max.) @33MHz
	ICC2	15mA(max.)	20mA(max.)
	ICC3	15mA(max.)	15mA(max.)
	ICC4	15mA(max.)	15mA(max.)
	ICC5	15mA(max.)	20mA(max.)

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### 3. Command Set Comparison

The new product adds new command Double Output Mode Command (DREAD) for the new feature. The other commands are the same as previous products.

**Table 3-1: Commands for the MX25L512/512C/1005/1005C and MX25L512E/1006E**

Command		MX25L512 MX25L512C MX25L1005 MX25L1005C	MX25L512E MX25L1006E
<b>Write</b>	WREN	06h	06h
	WRDI	04h	04h
	WRSR	01h	01h
<b>Read</b>	RDID	9Fh	9Fh
	RDSR	05h	05h
	READ	03h	03h
	FAST READ	0Bh	0Bh
	DREAD	-	3Bh
	RES	ABh	ABh
	REMS	90h	90h
	<b>Erase</b>	SE	20h
BE		52h or D8h	52h or D8h
CE		60h or C7h	60h or C7h
<b>Program</b>	PP	02h	02h
<b>Deep Power Down</b>	DP	B9h	B9h
	RDP	ABh	ABh

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#### 4. Device ID Code Comparison

The following tables show that the Manufacturer and Device IDs have not changed.

**Table 4-1: Device ID Comparison of 512Kb Devices**

Command Type	MX25L512			MX25L512C			MX25L512E		
RDID Command	M ID	Type	Density	M ID	Type	Density	M ID	Type	Density
	C2	20	10	C2	20	10	C2	20	10
RES Command	E ID			E ID			E ID		
	05			05			05		
REMS	M ID	Device ID		M ID	Device ID		M ID	Device ID	
	C2	05		C2	05		C2	05	

**Table 4-2: Device ID Comparison of 1Mb Devices**

Command Type	MX25L1005			MX25L1005C			MX25L1006E		
RDID Command	M ID	Type	Density	M ID	Type	Density	M ID	Type	Density
	C2	20	11	C2	20	11	C2	20	11
RES Command	E ID			E ID			E ID		
	10			10			10		
REMS	M ID	Device ID		M ID	Device ID		M ID	Device ID	
	C2	10		C2	10		C2	10	

#### 5. References

The following datasheets were used for preparing this comparison note:

Datasheet	Location	Date Issued	Version
MX25L512	Macronix Website	Apr., 2009	1.7
MX25L512C	Macronix Website	Jan., 2010	1.3
MX25L512E	Macronix Website	Apr., 2011	1.0
MX25L1005	Macronix Website	Apr., 2009	2.0
MX25L1005C	Macronix Website	Apr., 2010	1.3
MX25L1006E	Macronix Website	Apr., 2011	1.0

For more functional and parametric specifications, please refer to the datasheet on the Macronix Website at <http://www.macronix.com/> and go to: Products/Flash Memory/Serial Flash.



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**Revision History**

<b>Revision No.</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
1.0	1. Initial release	All	MAY/09/2011
1.1	1. Revise page heading format and table to sync with other Application Note	All	AUG/15/2011
	2. Move Introduction section ahead of Table of Contents	P1, P2	
	3. Add Performance Comparisons section in detail, and remove original "DC Characteristic Differences", "Read Performance" and "Write Performance" sections	All	
	4. Add Command Set Comparison section	P5	
	5. Add Device ID Code Comparison section	P6	
	6. Add References section	P6	
	7. Remove Conclusion section		





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## APPLICATION NOTE

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