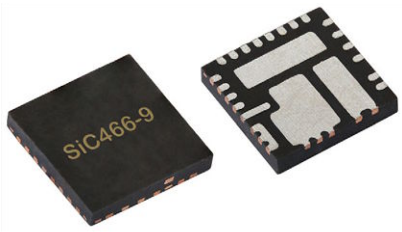
4.5 V to 60 V Input, 2 A, 4 A, 6 A, 10 A microBUCK® DC/DC Converter



LINKS TO ADDITIONAL RESOURCES

PowerCAD Design Tool | Evaluation Boards | Design Tools

DESCRIPTION

The SiC46x is a family of wide input voltage high efficiency synchronous buck regulators with integrated high side and low side power MOSFETs. Its power stage is capable of supplying high continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.8 V from 4.5 V to 60 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC46x's architecture delivers ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and is stable with any capacitor. No external ESR network is required for loop stability purpose. The device also incorporates a power saving scheme that significantly increases light load efficiency. The regulator integrates a full protection feature set, including over current protection (OCP), output overvoltage protection (OVP), short circuit protection (SCP), output undervoltage protection (UVP) and thermal shutdown (OTP). It also has UVLO for input rail and a user programmable soft start.

The SiC46x family is available in 2 A, 4 A, 6 A, 10 A pin compatible 5 mm by 5 mm lead (Pb)-free power enhanced MLP55-27L package.

TYPICAL APPLICATION CIRCUIT

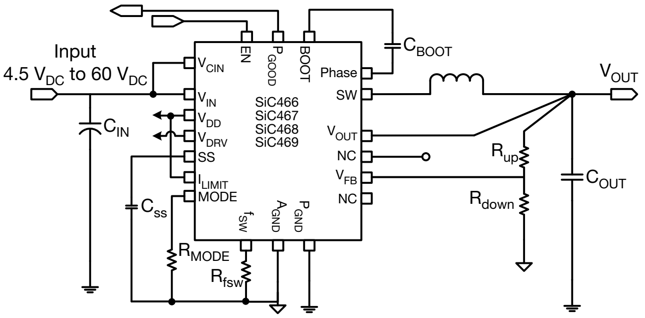


Fig. 1 - Typical Application Circuit

FEATURES

RoHS COMPLIANT
HALOGEN FREE

- Versatile
  - Single supply operation from 4.5 V to 60 V input voltage
  - Adjustable output voltage down to 0.8 V
  - Scalable solution 2 A (SiC469), 4 A (SiC468), 6 A (SiC467), 10 A (SiC466)
  - Output voltage tracking and sequencing with pre-bias start up
  - ± 1 % output voltage accuracy at -40 °C to +125 °C
- Internal compensation
- Highly efficient
  - 98 % peak efficiency
  - 4 μA supply current at shutdown
  - 156 μA operating current not switching
- Highly configurable
  - Adjustable switching frequency from 100 kHz to 2 MHz
  - Adjustable soft start and selectable preset 100 %, 75 %, and 50 % current limit
  - 2 modes of operation, forced continuous conduction, power save
- Robust and reliable
  - Output over voltage protection
  - Output under voltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
  - Supported by Vishay PowerCAD online design simulation
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Industrial and automation
- Home automation
- Industrial and server computing
- Networking, telecom, and base station power supplies
- Wall transformer regulation
- Robotics
- High end hobby electronics: remote control cars, planes, and drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machines

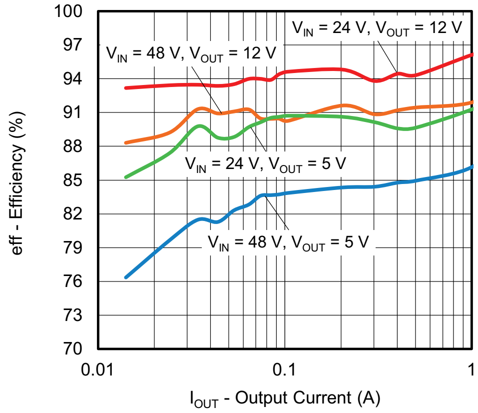


Fig. 2 - SiC467 Efficiency vs. Output Current

PIN CONFIGURATION

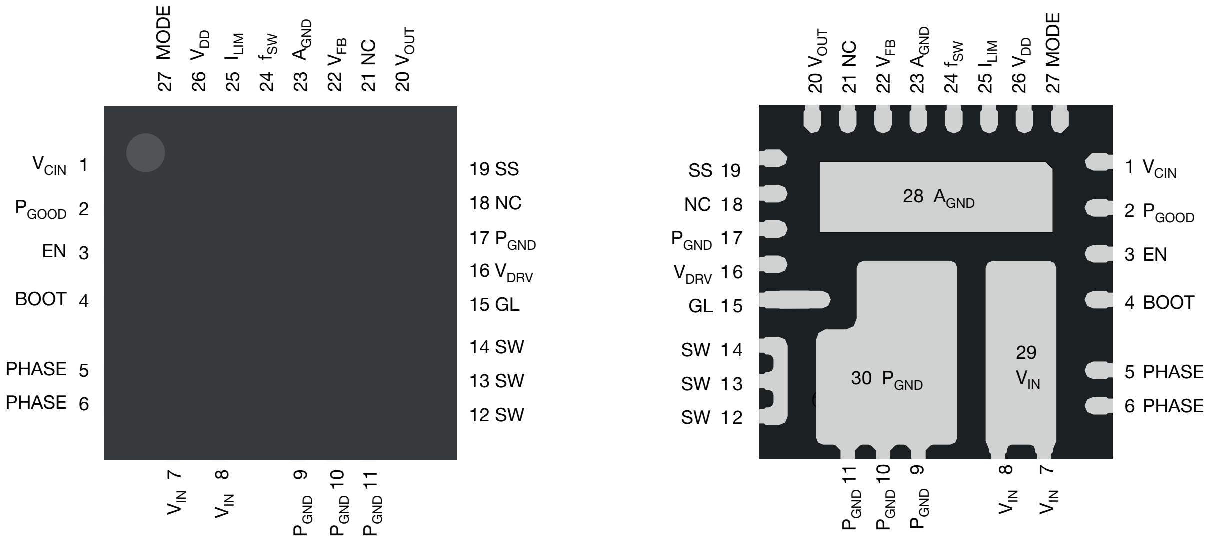


Fig. 3 - Pin Configuration

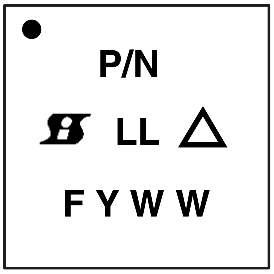
PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{CIN}	Supply voltage for internal regulators V_{DD} and V_{DRV}. This pin should be tied to V_{IN}, but can also be connected to a lower supply voltage (> 5 V) to reduce losses in the internal linear regulators
2	P_{GOOD}	Open-drain power good indicator - high impedance indicates power is good. An external pull-up resistor is required
3	EN	Enable pin. Tie high / low to enable / disable the IC accordingly. This is a high voltage compatible pin, can be tied to 60 V
4	BOOT	High side driver bootstrap voltage
5, 6	PHASE	Return path of high side gate driver
7, 8, 29	V_{IN}	Power stage input voltage. Drain of high side MOSFET
9, 10, 11, 17, 30	P_{GND}	Power ground
12, 13, 14	SW	Power stage switch node
15	GL	Low side MOSFET gate signal
16	V_{DRV}	Supply voltage for internal gate driver. When using the internal LDO as a bias power supply, V_{DRV} is the LDO output. Connect a 4.7 μF decoupling capacitor to P_{GND}
18, 21	NC	No connection internally
19	SS	Set the soft start ramp by connecting a capacitor to A_{GND}. An internal current source will charge the capacitor
20	V_{OUT}	Output voltage sense point for internal ripple injection components
22	V_{FB}	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from V_{OUT} to A_{GND}
23, 28	A_{GND}	Analog ground
24	f_{SW}	Set the on-time by connecting a resistor to A_{GND}
25	I_{LIMIT}	Set the current limit by connecting I_{LIMIT} pin to A_{GND}, float or V_{DD}
26	V_{DD}	Bias supply for the IC. V_{DD} is an LDO output, connect a 1 μF decoupling capacitor to A_{GND}
27	Mode	Set various operation modes by connecting a resistor to A_{GND}. See specification table for details

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING CODE
SiC466ED-T1-GE3	PowerPAK® MLP55-27L	SiC466
SiC466EVB-D	Reference board	
SiC467ED-T1-GE3	PowerPAK® MLP55-27L	SiC467
SiC467EVB-D	Reference board	
SiC468ED-T1-GE3	PowerPAK® MLP55-27L	SiC468
SiC468EVB-E	Reference board	
SiC469ED-T1-GE3	PowerPAK® MLP55-27L	SiC469
SiC469EVB-E	Reference board	

PART MARKING INFORMATION



● = pin 1 indicator
P/N = part number code
= Siliconix logo
△ = ESD symbol
F = assembly factory code
Y = year code
WW = week code
LL = lot code

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

ELECTRICAL PARAMETER	CONDITIONS	LIMITS	UNIT
V_{CIN}, V_{IN}	Reference to P_{GND}	-0.3 to 66	V
EN	Reference to P_{GND}	-0.3 to 60	
SW / PHASE	Reference to P_{GND}	-0.3 to 66	
SW / PHASE (AC)	100 ns	-10 to 72	
V_{DRV}	Reference to P_{GND}	-0.3 to 6	
V_{DD}	Reference to A_{GND}	-0.3 to V_{DRV} + 0.3	
BOOT		-0.3 to V_{PHASE} + V_{DRV}	
A_{GND} to P_{GND}		-0.3 to 0.3	
V_{OUT}	Reference to P_{GND}	30	
All other pins	Reference to A_{GND}	-0.3 to V_{DD} + 0.3	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Thermal resistance from junction to ambient		12	°C/W
Thermal resistance from junction to case		2	
ESD Protection			
Electrostatic discharge protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-A101	500	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	4.5	-	60	V
Control input voltage (V_{CIN}) (1)	4.5	-	60	
Enable (EN)	0	-	60	
Bias supply (V_{DD})	4.75	5	5.25	
Drive supply voltage (V_{DRV})	4.75	5.3	5.55	
Output voltage (V_{OUT})	0.8	-	15	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

Note

(1) For input voltages below 5 V, provide a separate supply to V_{CIN} of at least 5 V to prevent the internal V_{DD} rail UVLO from triggering

ELECTRICAL SPECIFICATIONS ($V_{IN} = V_{CIN}$ = 48 V, T_J = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power Supplies						
V_{DD} supply	V_{DD}	$V_{IN} = V_{CIN}$ = 6 V to 60 V, V_{EN} = 5 V, not switching	4.55	5	5.3	V
		$V_{IN} = V_{CIN}$ = 5 V, V_{EN} = 5 V, not switching	4.5	5	-	
V_{DD} dropout	$V_{DD\_DROPOUT}$	$V_{IN} = V_{CIN}$ = 5 V, I_{VDD} = 1 mA	-	150	-	mV
V_{DD} UVLO threshold, rising	V_{DD_UVLO}		3.75	4	4.25	V
V_{DD} UVLO hysteresis	$V_{DD\_UVLO\_HYST}$		-	150	-	mV
Input current	IV_{CIN}	Non-switching, V_{FB} > 0.8 V	-	156	200	μA
Shutdown current	IV_{CIN_SHDN}	V_{EN} = 0 V	-	4	8	
Controller and Timing						
Feedback voltage	V_{FB}	T_J = 25 °C	796	800	804	m/V
		T_J = -40 °C to +125 °C (1)	792	800	808	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Minimum on-time	$t_{ON\_MIN.}$		-	45	100	ns
t_{ON} accuracy	$t_{ON\_ACCURACY}$		-10	-	10	%
On-time range	t_{ON_RANGE}		100	-	8000	ns
Minimum off-time	$t_{OFF\_MIN.}$		-	250	-	ns
Soft start current	I_{SS}		2	5	7	μA
Zero crossing detection point	ZCD	LX-P_{GND}	-3	-	3	mV

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, T_J = -40 °C to +125 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fault Protections						
SiC466 valley current limit	I_{OCP}	I_{LM} tied to V_{DD}	-	13	-	A
		I_{LM} is not connect	-	9.75	-	
		I_{LM} tied to A_{GND}	-	6.5	-	
SiC467 valley current limit		I_{LM} tied to V_{DD}	-	10	-	
		I_{LM} is not connect	-	7.5	-	
		I_{LM} tied to A_{GND}	-	5	-	
SiC468 valley current limit		I_{LM} tied to V_{DD}	-	6	-	
		I_{LM} is not connect	-	4.2	-	
		I_{LM} tied to A_{GND}	-	3	-	
SiC469 valley current limit		I_{LM} tied to V_{DD}	-	4	-	
		I_{LM} is not connect	-	3	-	
		I_{LM} tied to A_{GND}	-	2	-	
Output OVP threshold	OVP	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	UVP		-	-80	-	
Over temperature protection	OTP_R	Rising temperature	-	150	-	°C
	OTP_{HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	P_{GOOD_HYST}		30	40	55	mV
Power good on resistance	R_{ON_PGOOD}		-	6	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	μs
EN / MODE / Threshold						
EN logic high level	V_{EN_H}		1.2	1.4	1.5	V
EN logic low level	V_{EN_L}		1	1.2	1.35	
EN logic hysteresis	V_{EN_HYS}		150	200	400	mV
EN pull down resistance	R_{EN}		-	6	-	MΩ
Mode pull up current	I_{MODE}		-	5	-	μA
Mode 1	R_{MODE}	Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	-	2	-	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	-	301	-	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	-	499	-	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	-	1000	-	

Note

(1) Guaranteed by design

FUNCTIONAL BLOCK DIAGRAM

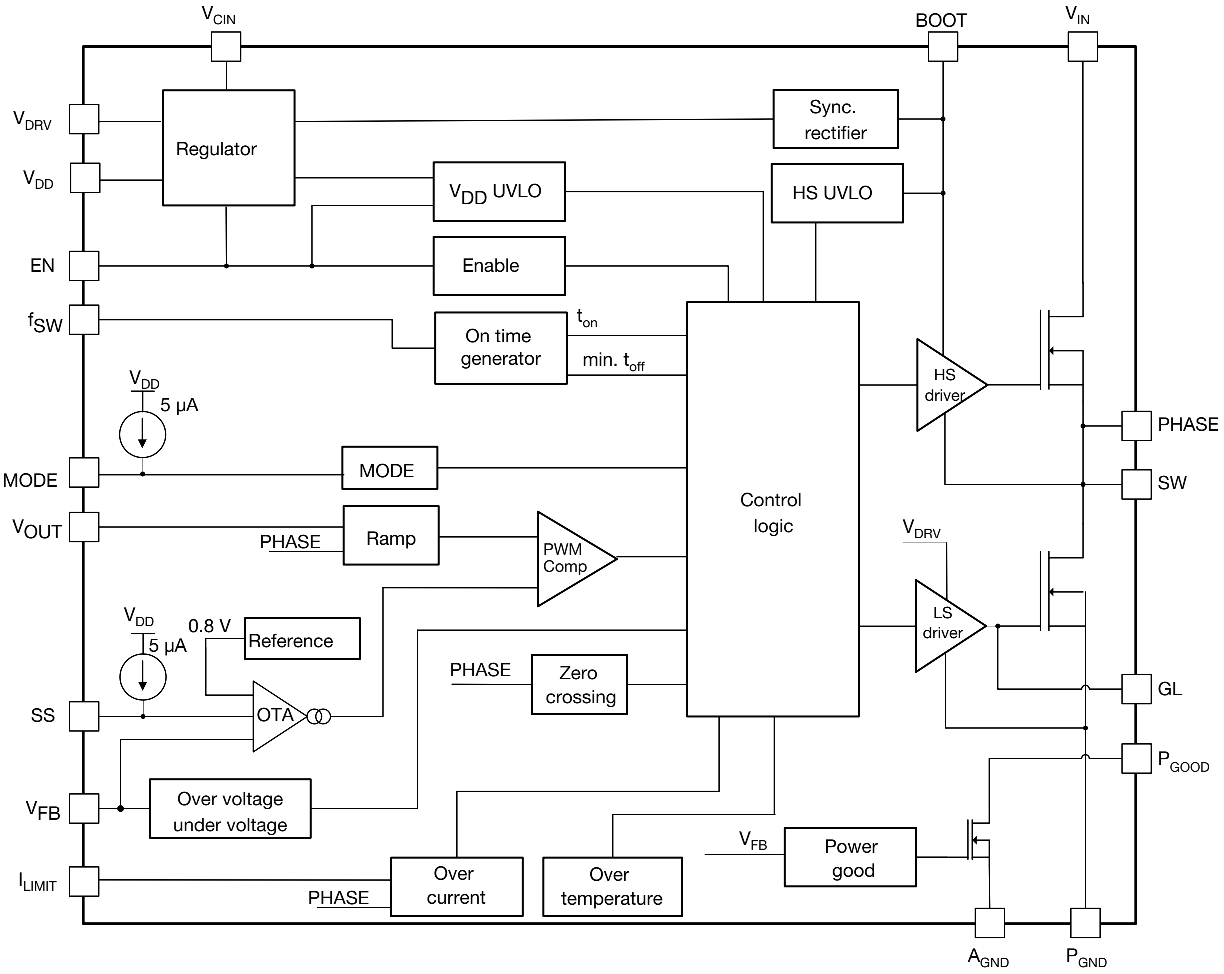


Fig. 4 - Functional Block Diagram

OPERATIONAL DESCRIPTION

Device Overview

SiC46x is a high efficiency synchronous buck regulator family capable of delivering up to 10 A continuous current. The device has programmable switching frequency of 100 kHz to 2 MHz. The control scheme is based on voltage mode constant on time. It delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency fold back as the load decreases.

SiC46x has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output overvoltage protection
- Output undervoltage protection with device going into hiccup mode
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output
- This device is available in MLP55-27L package to deliver high power density and minimize PCB area

Power Stage

SiC46x integrates a high performance power stage with a n-channel high side MOSFET and a n-channel low side MOSFET optimized to achieve up to 98 % efficiency.

The power input voltage (V_{IN}) can go up to 60 V and down as low as 4.5 V for power conversion.

Control Scheme

SiC46x employs a voltage - mode COT control mechanism in conjunction with adaptive zero current detection which allows for power saving in discontinuous conduction mode (DCM). The switching frequency, f_{SW}, is set by an external resistor R_{fsw} connected from f_{sw} pin to ground. The SiC46x operates between 200 kHz to 2 MHz depending on V_{IN} and V_{OUT} conditions.

$$R_{fsw} = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

Note, that there is no V_{IN} dependency on f_{SW} as long as V_{IN} and V_{CIN} are connected to the same supply.

SiC46x employs an advanced voltage - mode COT control mechanism.

During steady-state operation, feedback voltage (V_{FB}) is compared with internal reference (0.8 V typ.) and the amplified error signal (V_{COMP}) is generated at the internal comp node. An internally generated ramp signal and V_{COMP} feed into a comparator. Once V_{RAMP} crosses V_{COMP}, an on-time pulse is generated for a fixed time. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a dead time period. The low side MOSFET will stay on for a minimum duration equal to the minimum off-time ($t_{OFF\_MIN.}$) and remains on until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 5 illustrates the operation as described above.

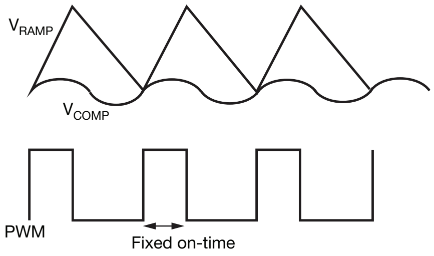


Fig. 5 - Operational Principle

Power-Save Mode and Mode Pin Operation

To improve efficiency at light-loads, SiC46x provides a set of innovative implementations to eliminate LS re-circulating current and switching losses. The internal zero crossing detector (ZCD) monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off the LS FET. If load further decreases, switching frequency is reduced proportional to the load condition to save switching losses while keeping output ripple within tolerance.

To improve the converter efficiency, the user can choose to disable the internal V_{DRV} regulator by picking either mode 3 or mode 4 and connecting a 5 V supply to the V_{DRV} pin. This reduces power dissipation in the SiC46x by eliminating the V_{DRV} linear regulator losses.

The mode pin supports several modes of operation as shown in table 1. An internal current source is used to set the voltage on this pin using an external resistor:

TABLE 1 - OPERATION MODES

MODE	RANGE (kΩ)	POWER SAVE MODE	INTERNAL V_{DRV} REGULATOR
1	0 to 100	Enabled	ON
2	298 to 304	Disabled	ON
3	494 to 504	Disabled	OFF (1)
4	900 to 1100	Enabled	OFF (1)

Note

(1) Connect a 5 V (± 5 %) supply to the V_{DRV} pin

The mode pin is not latched to any state and can be changed on the fly.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiC46x has cycle by cycle current limiting. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the valley current is compared with an internal threshold. If monitored current is higher than threshold, high side MOSFET is kept off until the inductor current falls below OCP threshold.

OCP is enabled immediately after V_{DD} passes UVLO rising threshold.

There are 3 settings for the valley current OCP namely 50 %, 75 % and 100 %. The selection can be chosen by connecting the I_{LIMIT} pin either to V_{DD}, float or GND. Connecting to V_{DD} will select 100 % of the preset valley current OCP corresponding to the SiC46x being used. If the pin is floating, the valley current OCP is 75 %. Connecting to GND, the valley current OCP is 50 %.

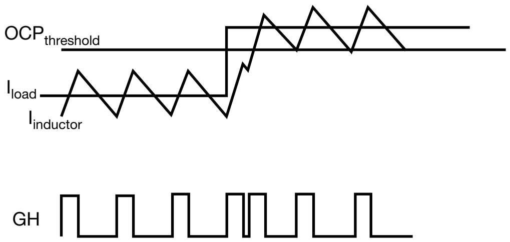


Fig. 6 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. If the voltage level at V_{FB} goes below 0.16 V (V_{OUT} is 20 % of V_{OUT} set point) for more than 25 µs a UVP event is recognized and both HS and LS MOSFETs are turned off. After a time-out period equal to 20 soft start cycles, the IC attempts to re-start by going through a soft start cycle. If the fault condition still exists, the above cycle will be repeated.

UVP is only active after the completion of soft-start sequence.

Output Over Voltage Protection (OVP)

For OVP implementation, output is monitored through FB pin. After soft start, if the voltage level at FB is above 0.96 V (typ.) (V_{OUT} is 120 % of V_{OUT} set point), OVP is triggered with both the HS and LS MOSFETs turned off. Normal operation is resumed once FB voltage drops back to 0.96 V.
OVP is active immediately after V_{DD} passes UVLO level.

Over Temperature Protection (OTP)

SiC46x has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 150 °C (typ). A hysteresis of 35 °C is implemented, so when junction temperature drops below 115 °C, the device restarts by initiating soft-start sequence again.

In order to improve the efficiency at light load condition, OTP is disabled when the inductor current is discontinued.

Sequencing of Input / Output Supplies

SiC46x has no sequencing requirements on any of its input / output (V_{IN}, V_{DRV}, V_{DD}, V_{CIN}, EN) supplies or enables.

Enable

The SiC46x has an enable pin to turn the part on and off. Driving this pin high enables the device, while grounding it turns it off.

The SiC46x enable has a weak pull down to prevent unwanted turn on due to a floating GPIO.

There are no sequencing requirements with respect to other input / output supplies.

Soft-Start

During soft start time period, inrush current is limited and the output voltage is ramped gradually. The following control scheme is implemented:
Once the V_{DD} voltage reaches the UVLO trip point, an internal “Soft start Reference” (SR) begins to ramp up. The SR ramp rate is determined by the external soft start capacitor. There is an internal 5 µA current source tied to the soft start pin which charges the external soft start cap.
The internal SR signal is being used as a reference voltage to the loop error amplifier (see functional block diagram). The control scheme guarantees that the output voltage during the soft start interval will ramp up coincidently with the SR signal. voltage. The speed of the internal soft start ramp can SiC46x soft-start time is adjustable by selecting a capacitor value from the following equation.

$$\text{SS time} = \frac{C_{ext} \text{ x } 0.8 \text{ V}}{5 \text{ µA}}$$

During soft-start period, OCP is activated. Short circuit protection is not active until soft-start is complete.

Pre-Bias Start-Up

In case of pre-bias startup, if the sensed voltage on FB is higher than the internal soft-start ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

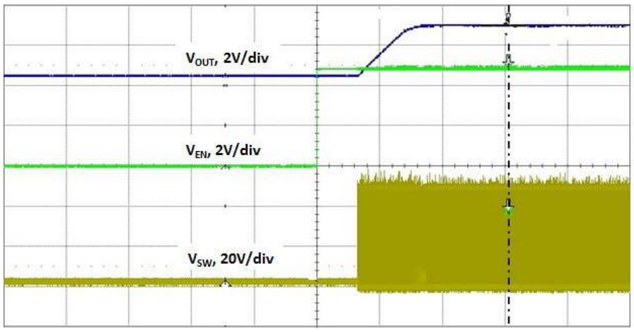


Fig. 7 - Pre-Bias Start-Up

Power Good

SiC46x's power good is an open-drain output. Pull P_{GOOD} pin high up to 5 V through a 10K resistor to use this signal. Power good window is shown in the Fig. 8. If voltage level on FB pin is out of this window, PG signal is de-asserted by pulling down to GND. To prevent false triggering during transient events, P_{GOOD} has a 25 μs blanking time.

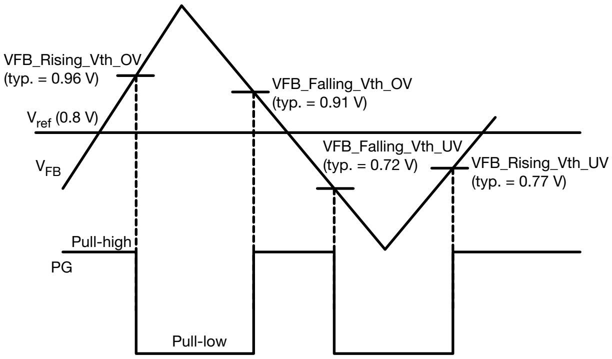


Fig. 8 - P_{GOOD} Window and Timing Diagram

SiC46x microBUCK FAMILY SCHEMATIC

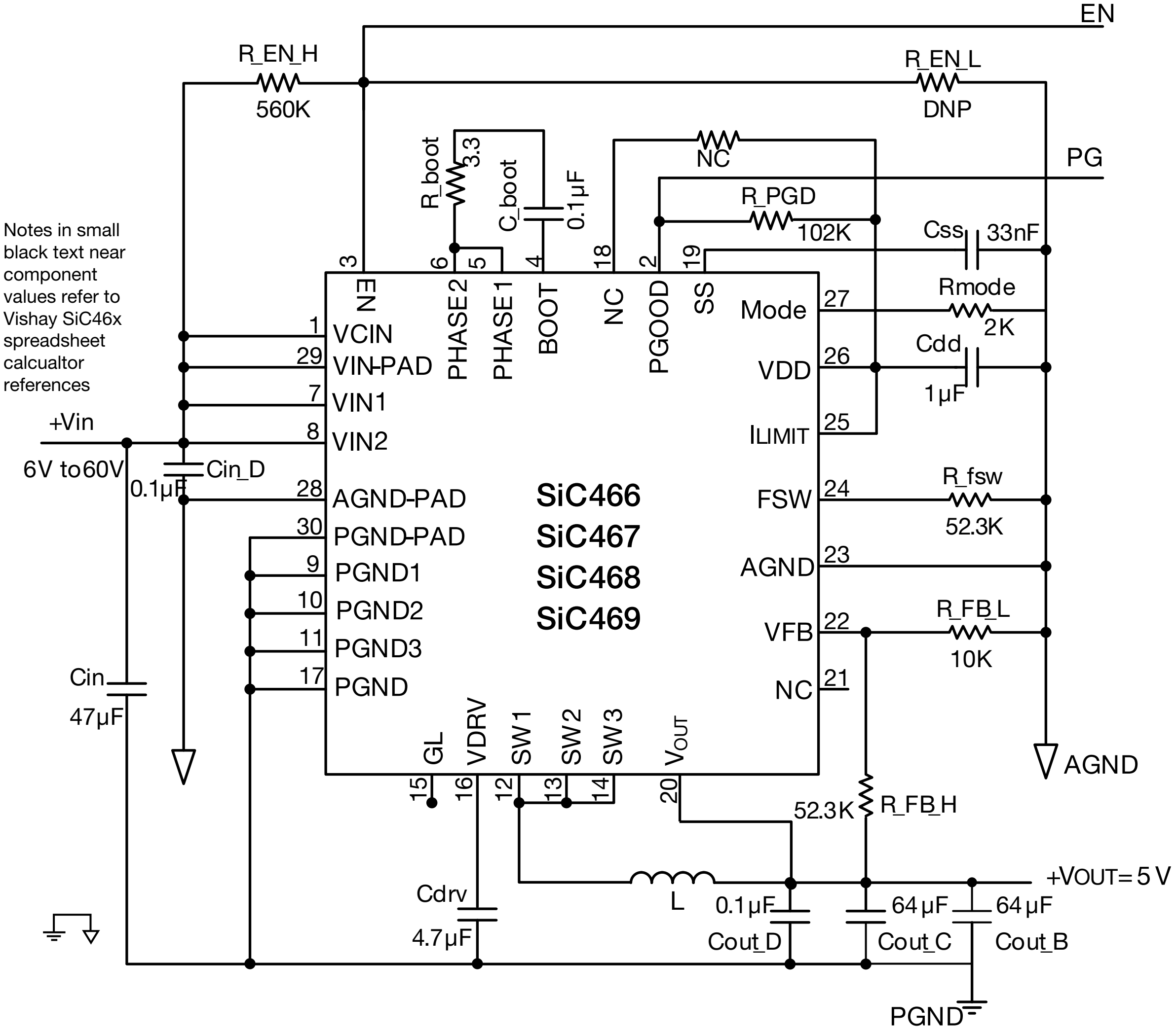


Fig. 9 - SiC467 Configured for 6 V to 60 V Input, 5 V Output at 6 A, 500 kHz Operation with Power Save Mode Enabled all Ceramic Output Capacitance Design

EXTERNAL COMPONENT SELECTION FOR THE SiC46x

This section explains external component selection for the SiC46x family of regulators. Component reference designators in any equation refer to the schematic shown in Fig. 9.

The online simulation tool PowerCAD helps to make external component calculation simple. The user simply needs to enter required operating conditions.

Output Voltage Adjustment

If a different output voltage is needed, simply change the value of V_{OUT} and solve for $R_{\_FB\_H}$ based on the following formula:

$$R_{\_FB\_H} = \frac{R_{\_FB\_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

Where V_{FB} is 0.8 V for the SiC46x. $R_{\_FB\_L}$ should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

Switching Frequency Selection

The following equation illustrates the relationship between on-time, V_{IN}, V_{OUT}, and R_{fsw} value:

$$R_{\_fsw} = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

Inductor Selection

The choice of inductor is specific to each application and quickly determined with the following equations:

$$t_{ON} = \frac{V_{OUT}}{V_{IN\_max.} \text{ x } f_{sw}}$$

and

$$L = \frac{(V_{IN} - V_{OUT}) \text{ x } t_{ON}}{I_{OUT\_MAX.} \text{ x } K}$$

Where K is a percentage of maximum output current ripple required. The designer can quickly make a choice of inductor if the ripple percentage is decided, usually no more than 30 % however higher or lower percentages of I_{OUT} can be acceptable depending on application. This device allows choices larger than 30 %.

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an I^2R loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus ½ of the ripple current. In an over current condition the inductor current may be very high. All this needs to be considered when selecting the inductor.

Output Capacitor Selection

The SiC46x is stable with any type of output capacitors by choosing the appropriate V_{RAMP} components. This allows the user to choose the output capacitance based on the best trade off of board space, cost and application requirements.

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple voltage requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus half of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output. The relationship between output voltage ripple, output capacitance and ESR of the output capacitor is shown by the following equation:

$$V_{RIPPLE} = I_{RIPPLE(MAX.)} \text{ x } \left(\frac{1}{8 \text{ x } C_o \text{ x } f_{sw}} + ESR\right) \qquad (1)$$

Where V_{RIPPLE} is the maximum allowed output ripple voltage; $I_{RIPPLE(MAX.)}$ is the maximum inductor ripple current; f_{sw} is the switching frequency of the converter; C_o is the total output capacitance; ESR is the equivalent series resistance of the total output capacitors.

In addition to the output ripple voltage requirement, the output capacitors need to meet transient requirements. A worst case load release condition (from maximum load to no load at the exact moment when inductor current is at the peak) determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero within 1 μs), the output capacitor must absorb all the energy stored in the inductor. The peak voltage on the capacitor, V_{PK}, under this worst case condition can be calculated by following equation:

$$C_{OUT\_MIN.} = \frac{L \text{ x } \left(I_{OUT} + \frac{1}{2} \text{ x } I_{RIPPLE(MAX.)}\right)^2}{(V_{PK})^2 - (V_{OUT})^2} \qquad (2)$$

During the load release time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor; therefore a smaller capacitance can be used. The following can be used to calculate the required capacitance for a given di_{LOAD}/dt.

Peak inductor current, I_{LPK}, is shown by the next equation:

$$I_{LPK} = I_{MAX.} + \frac{1}{2} \text{ x } I_{RIPPLE(MAX.)}$$

$$\text{The slew rate of load current} = \frac{di_{LOAD}}{dt}$$

$$C_{OUT\_MIN.} = I_{LPK} \text{ x } \frac{L \text{ x } \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX.}}{dI_{LOAD}} \text{ x } dt}{2(V_{PK} - V_{OUT})} \qquad (3)$$

Based on application requirement, either equation (2) or equation (3) can be used to calculate the ideal output capacitance to meet transition requirement. Compare this calculated capacitance with the result from equation (1) and choose the larger value to meet both ripple and transition requirement.

Enable Pin Voltage

The EN pin has an internal pull down resistor and only requires an enable voltage. This needs to be greater than 1.4 V. An input voltage or a resistor connected across V_{IN} and EN can be used. The internal pull down resistance is 5 MΩ.

Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{CINPKPK} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{CIN(RMS)} =$$

$$I_{OUT} \text{ x } \sqrt{D \text{ x } (1 - D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1 - D)^2 \times D}$$

The minimum input capacitance can then be found,

$$C_{IN\_min.} = I_{OUT} \text{ x } \frac{D \text{ x } (1 - D)}{V_{CINPKPK} \text{ x } f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7 μF ceramic input capacitance is a suitable starting point.
Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic input capacitance.

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC466 (10 A), unless otherwise noted)

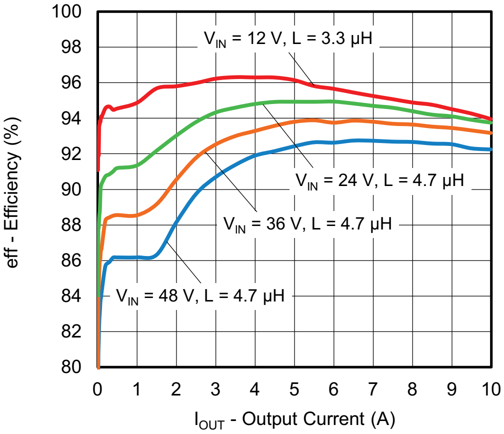


Fig. 10 - SiC466 Efficiency vs. Output Current, V_{OUT} = 5 V

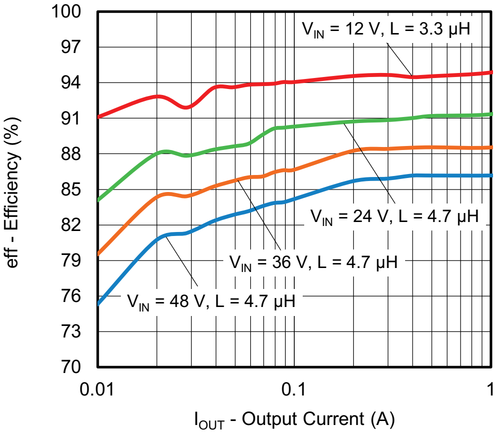


Fig. 13 - SiC466 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

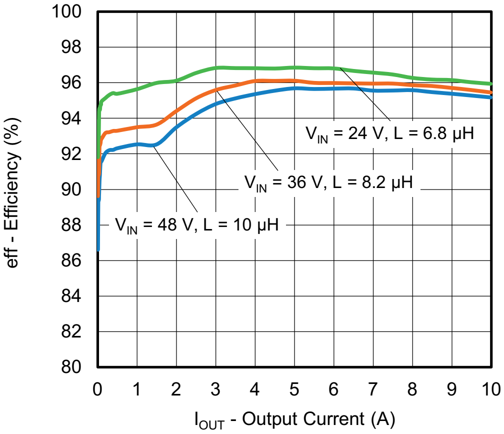


Fig. 11 - SiC466 Efficiency vs. Output Current, V_{OUT} = 12 V

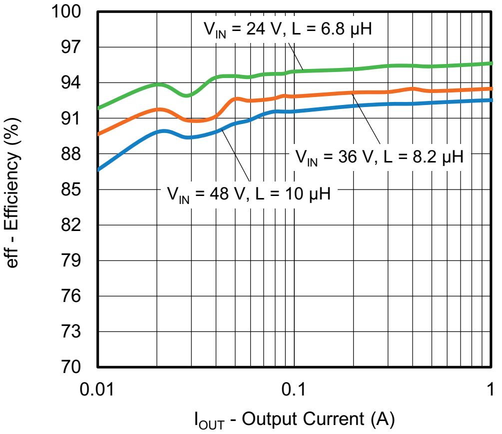


Fig. 14 - SiC466 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

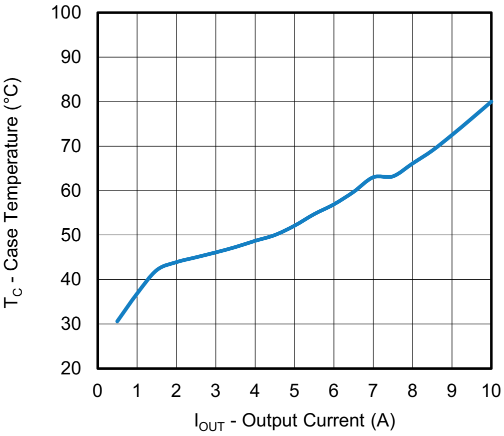


Fig. 12 - SiC466 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

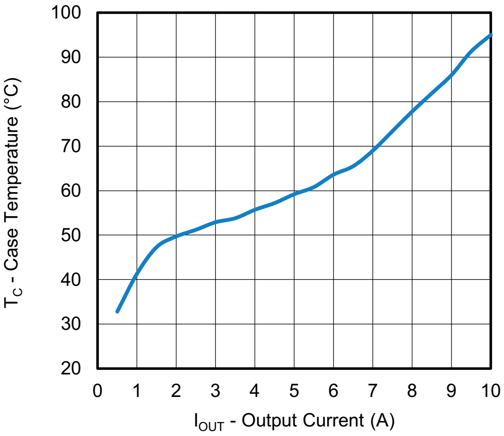


Fig. 15 - SiC466 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC467 (6 A), unless otherwise noted)

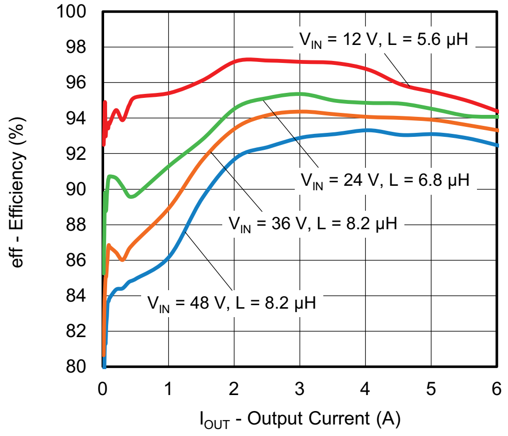


Fig. 16 - SiC467 Efficiency vs. Output Current, V_{OUT} = 5 V

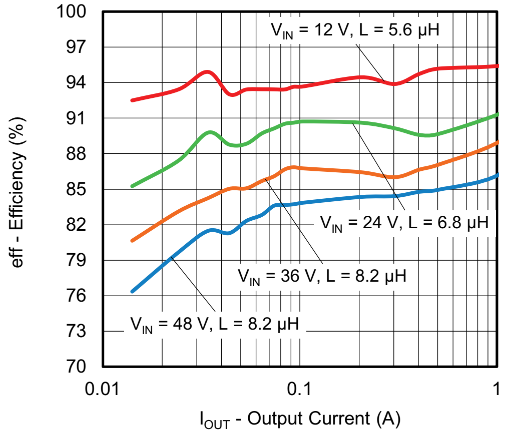


Fig. 19 - SiC467 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

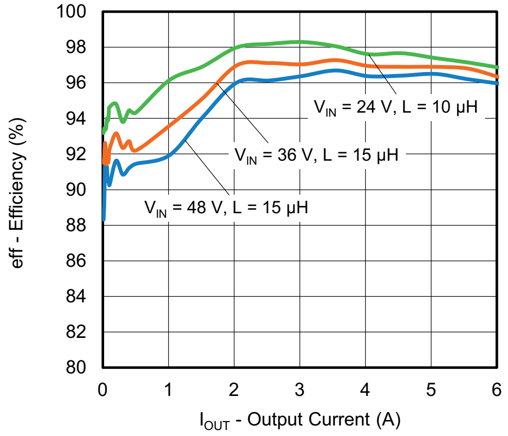


Fig. 17 - SiC467 Efficiency vs. Output Current, V_{OUT} = 12 V

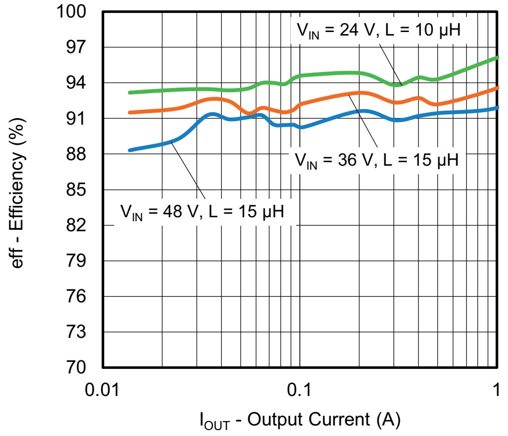


Fig. 20 - SiC467 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

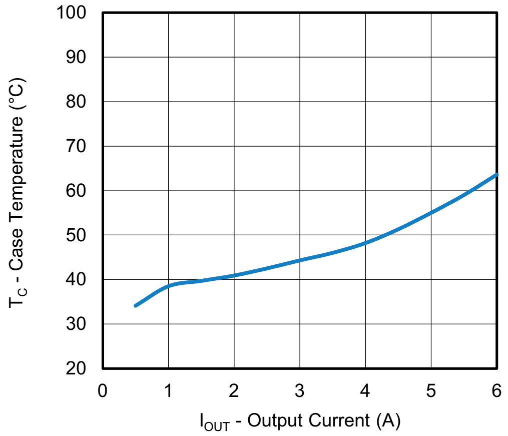


Fig. 18 - SiC467 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

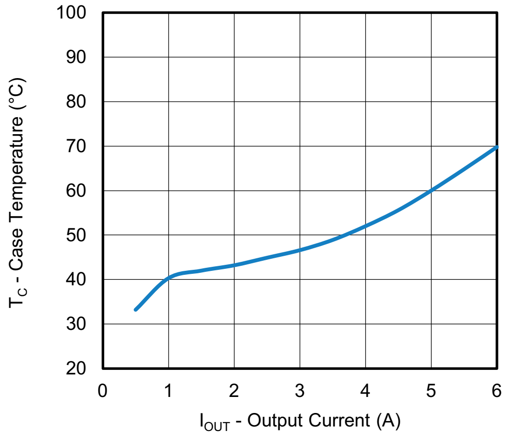


Fig. 21 - SiC467 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC468 (4 A), unless otherwise noted)

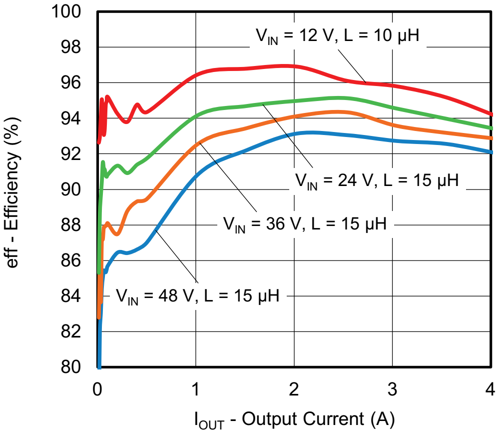


Fig. 22 - SiC468 Efficiency vs. Output Current, V_{OUT} = 5 V

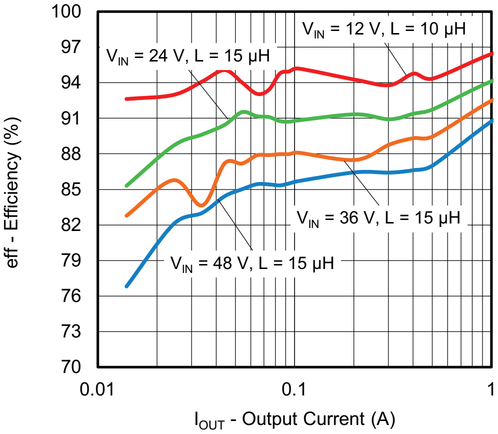


Fig. 25 - SiC468 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

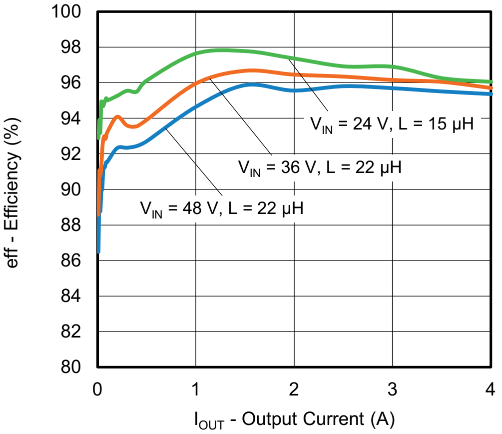


Fig. 23 - SiC468 Efficiency vs. Output Current, V_{OUT} = 12 V

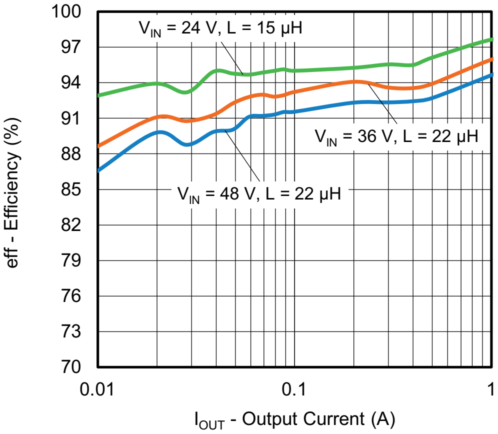


Fig. 26 - SiC468 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

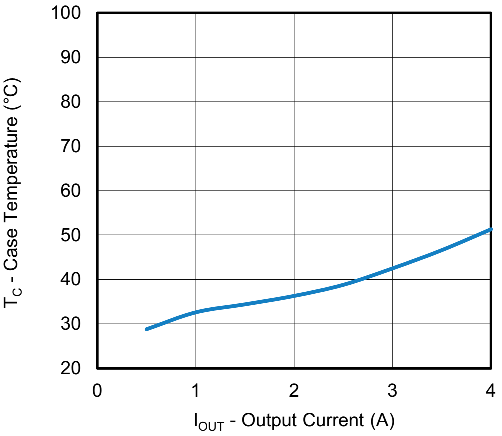


Fig. 24 - SiC468 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

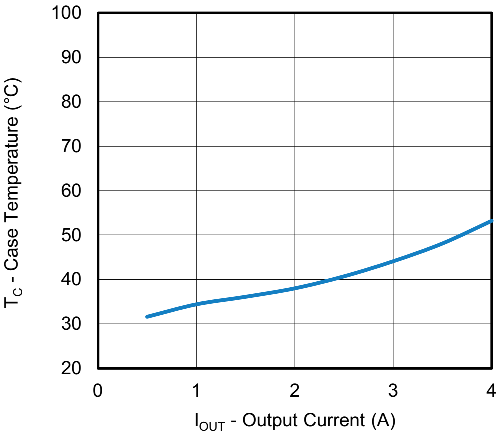


Fig. 27 - SiC468 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC469 (2 A), unless otherwise noted)

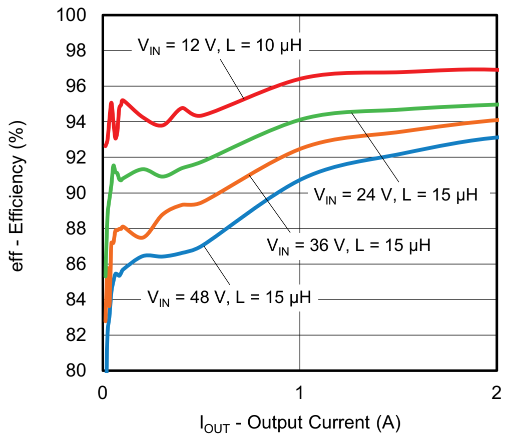


Fig. 28 - SiC469 Efficiency vs. Output Current, V_{OUT} = 5 V

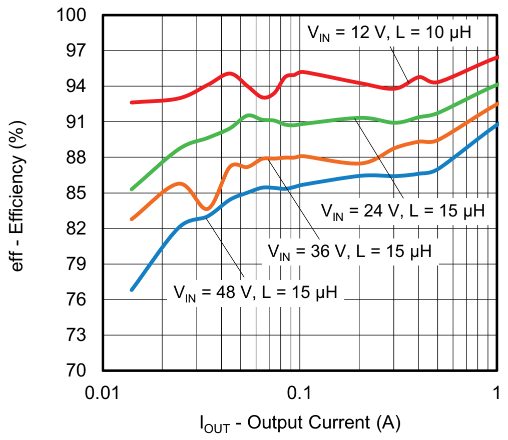


Fig. 31 - SiC469 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

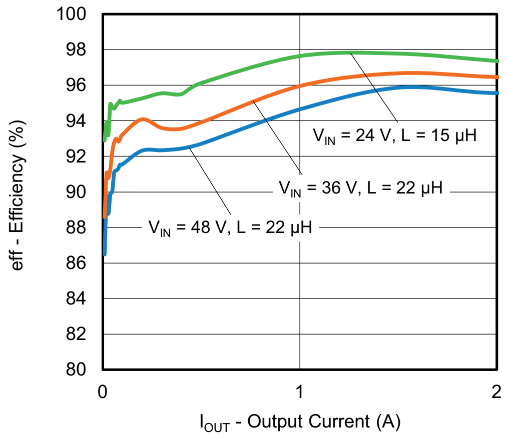


Fig. 29 - SiC469 Efficiency vs. Output Current, V_{OUT} = 12 V

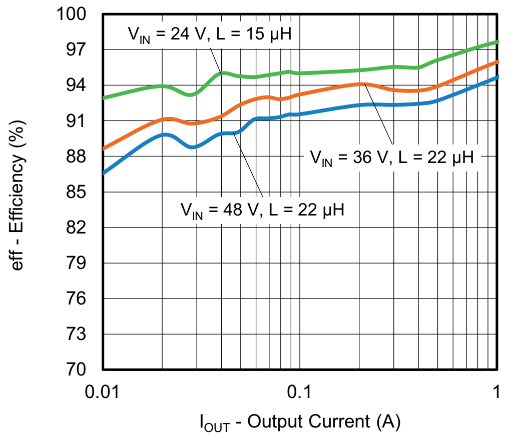


Fig. 32 - SiC469 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

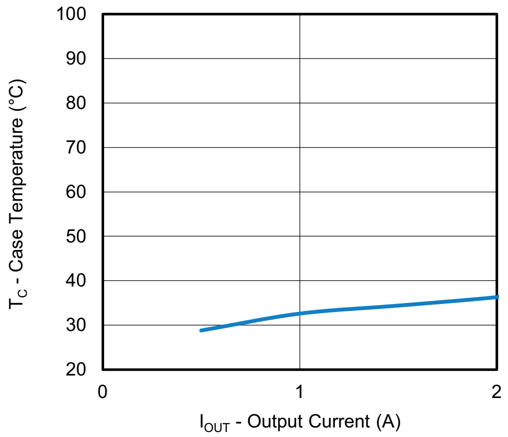


Fig. 30 - SiC469 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

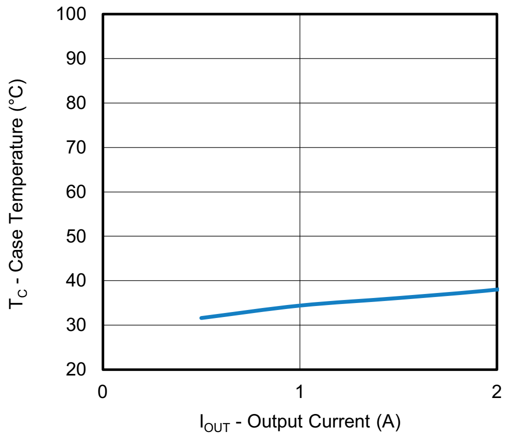


Fig. 33 - SiC469 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC467 (6 A), unless otherwise noted)

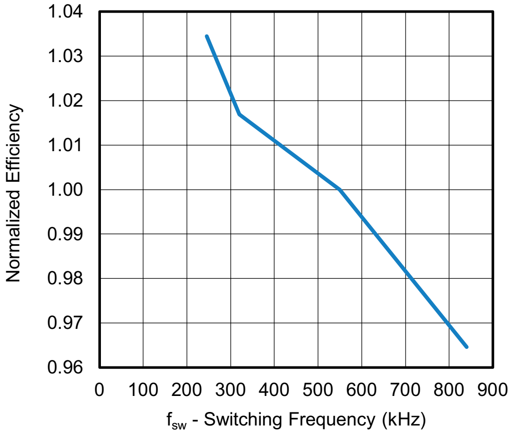


Fig. 34 - SiC466 Efficiency vs. Switching Frequency

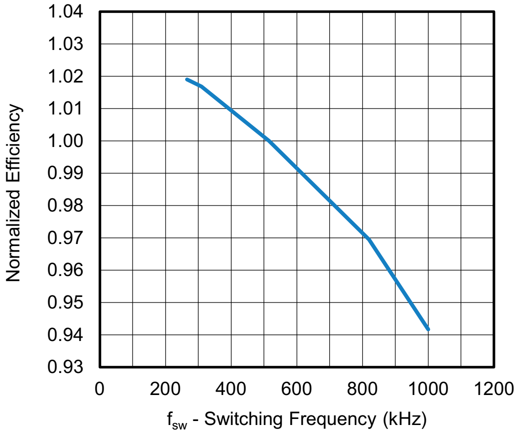


Fig. 37 - SiC467 Efficiency vs. Switching Frequency

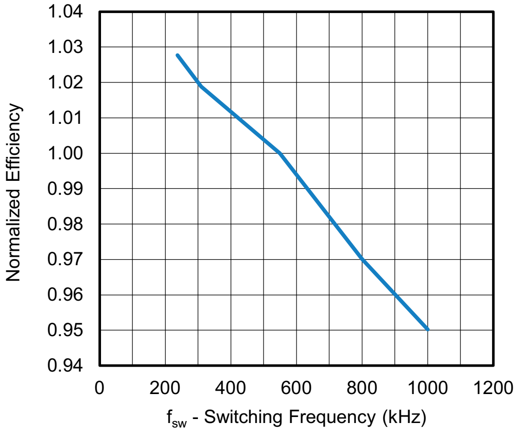


Fig. 35 - SiC468 Efficiency vs. Switching Frequency

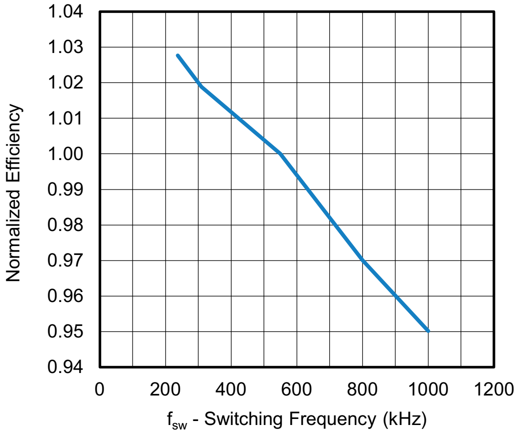


Fig. 38 - SiC469 Efficiency vs. Switching Frequency

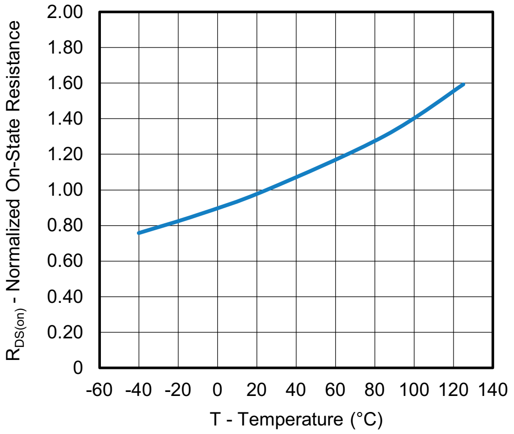


Fig. 36 - $R_{DS(ON)}$ vs. Temperature

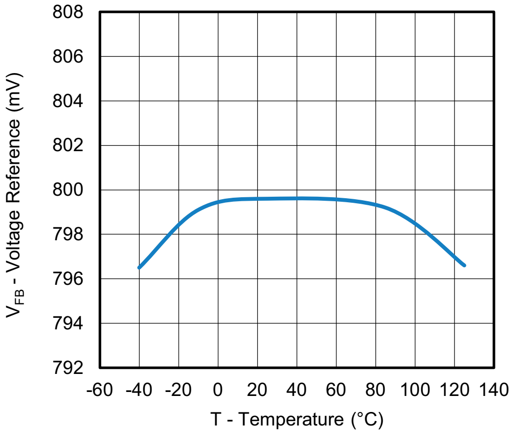


Fig. 39 - Voltage Reference vs. Temperature

For technical questions, contact: powerictechsupport@vishay.com

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC467 (6 A), unless otherwise noted)

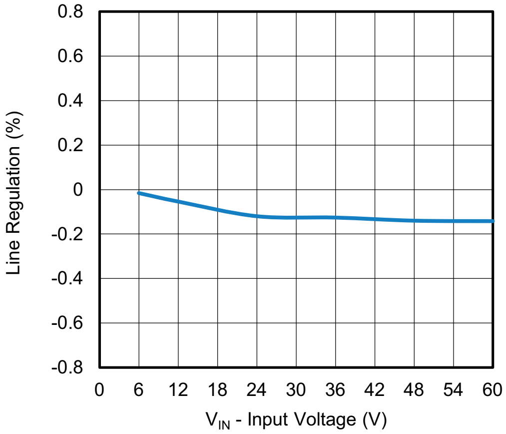


Fig. 40 - Line Regulation

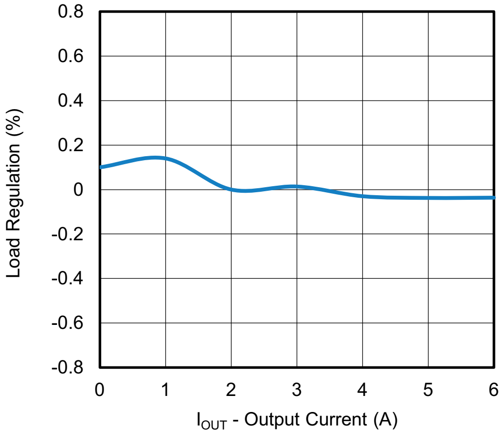


Fig. 43 - Load Regulation

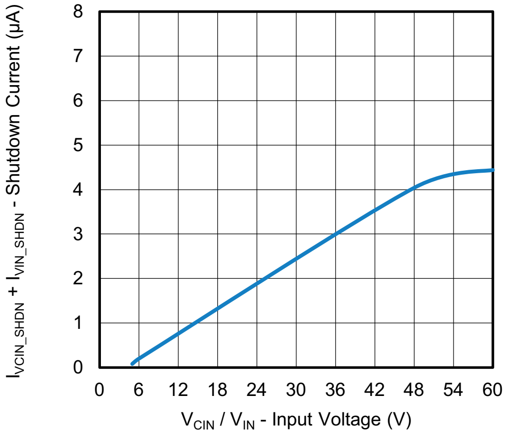


Fig. 41 - Shutdown Current vs. Input Voltage

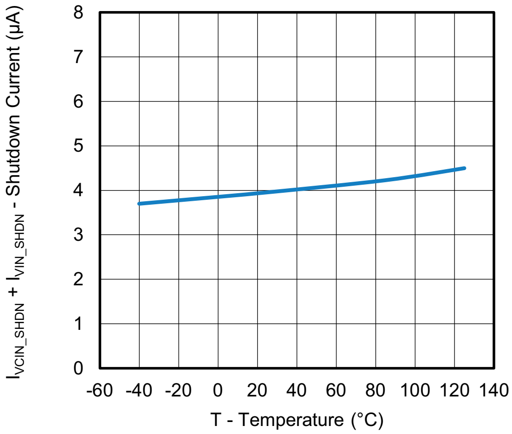


Fig. 44 - Shutdown Current vs. Junction Temperature

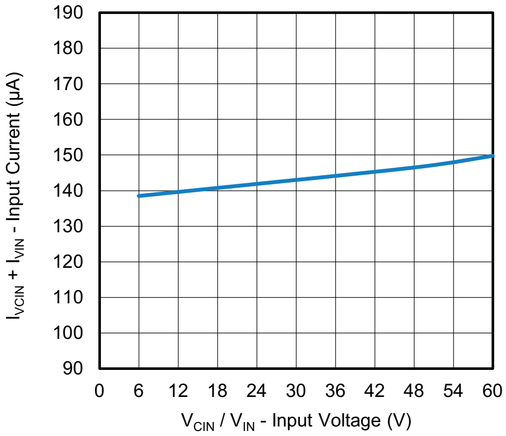


Fig. 42 - Input Current vs. Input Voltage

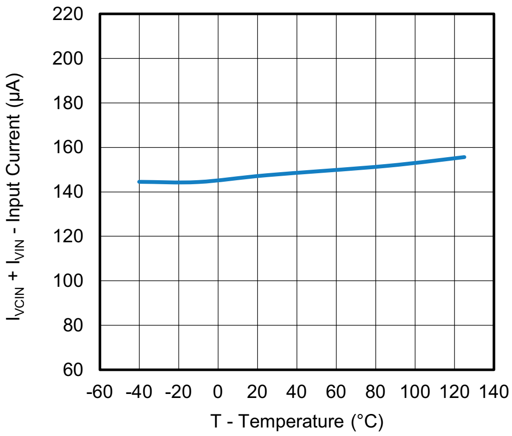


Fig. 45 - Input Current vs. Junction Temperature

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC467 (6 A), unless otherwise noted)

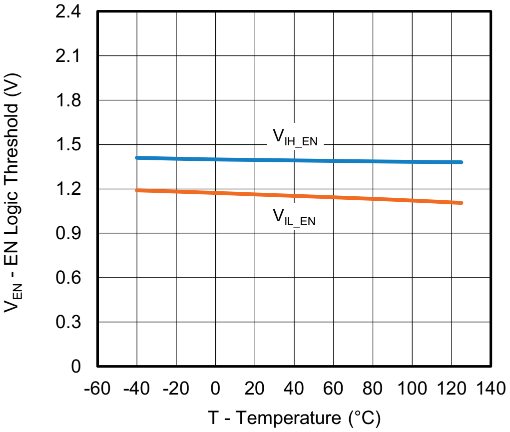


Fig. 46 - EN Logic Threshold vs. Junction Temperature

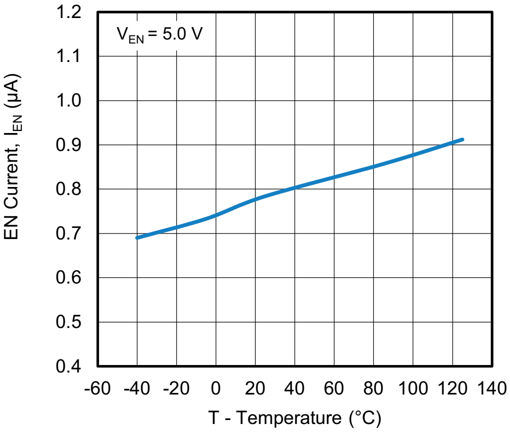


Fig. 49 - EN Current vs. Junction Temperature

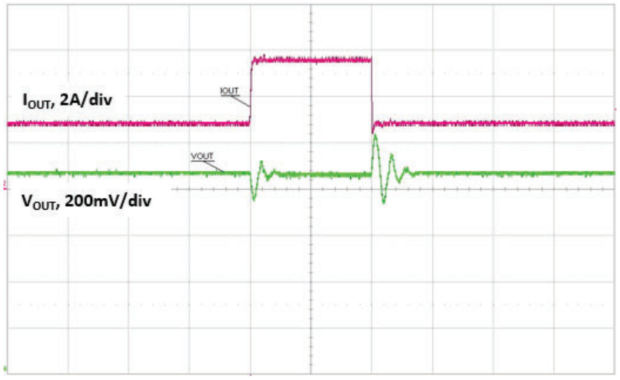


Fig. 47 - Load Transient (3 A to 6 A), Time = 100 µs/div

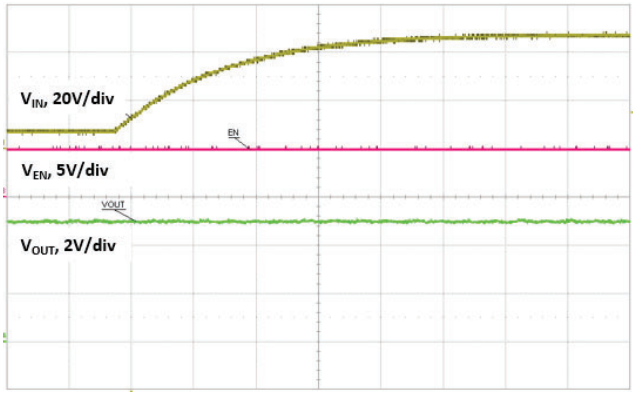


Fig. 50 - Line Transient (8 V to 48 V), Time = 10 ms/div

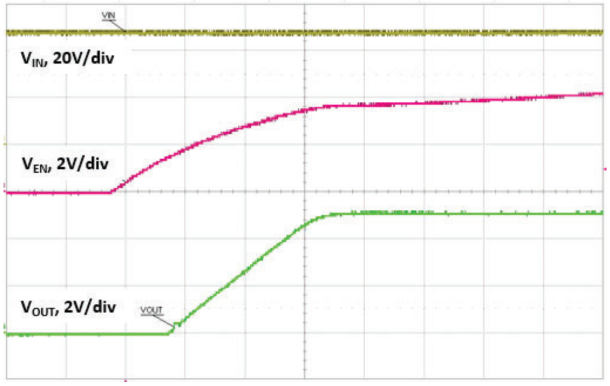


Fig. 48 - Start-Up with EN, Time = 1 ms/div

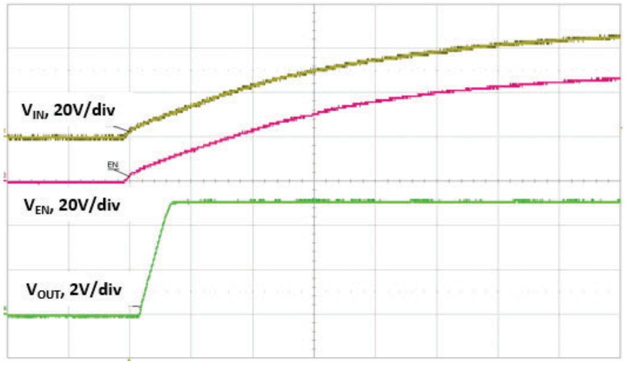


Fig. 51 - Start-up with V_{IN}, Time = 5 ms/div

ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC467 (6 A), unless otherwise noted)

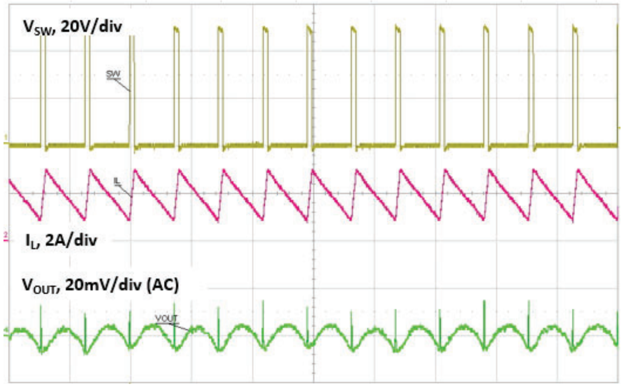


Fig. 52 - Output Ripple 2 A, Time = 5 μs/div

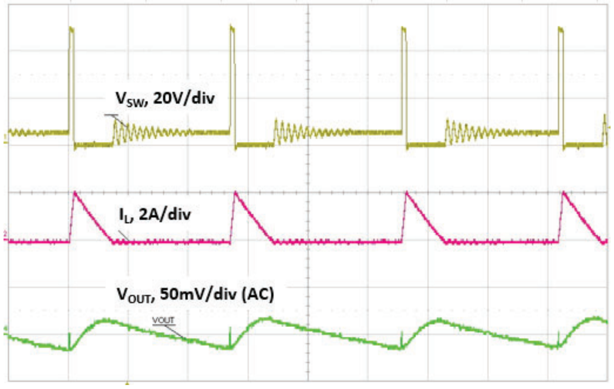


Fig. 54 - Output Ripple 300 mA, Time = 5 μs/div

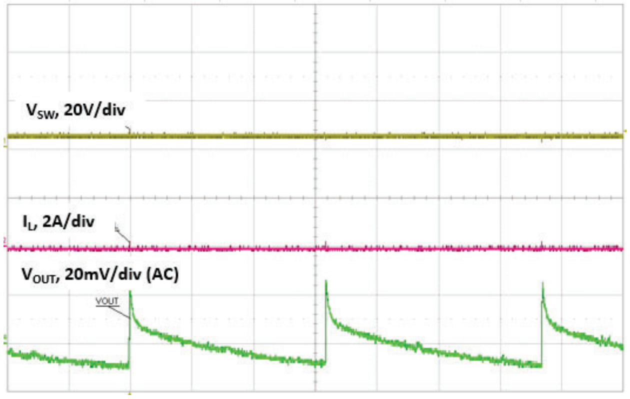


Fig. 53 - Output Ripple PSM, Time = 10 ms/div

PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling

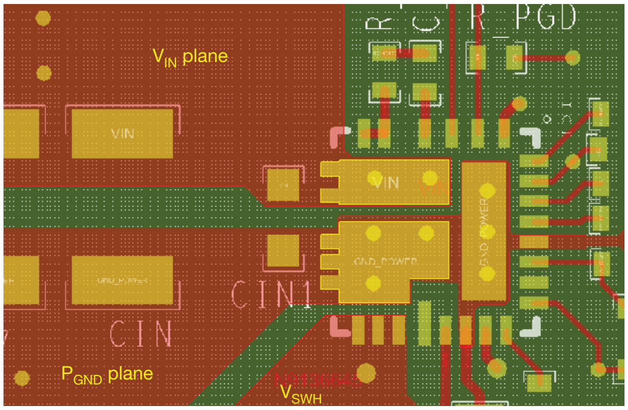


Fig. 55

1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 and 0603
4. Smaller capacitance values, placed closer to device's V_{IN} pin(s), is better for high frequency noise absorbing

Step 2: V_{CIN} Pin

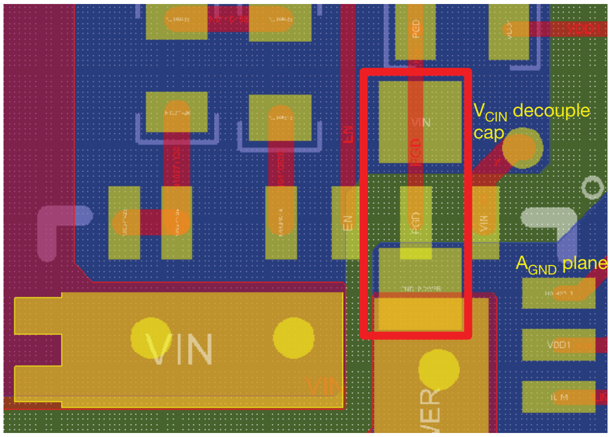


Fig. 56

1. V_{CIN} (pin 1) is the input pin for both internal LDO and t_{ON} block. t_{ON} time varies based on input voltage. It is necessary to put a decoupling capacitor close to this pin
2. The connection can be made through a via and the cap can be placed at bottom layer

Step 3: V_{SWH} Plane

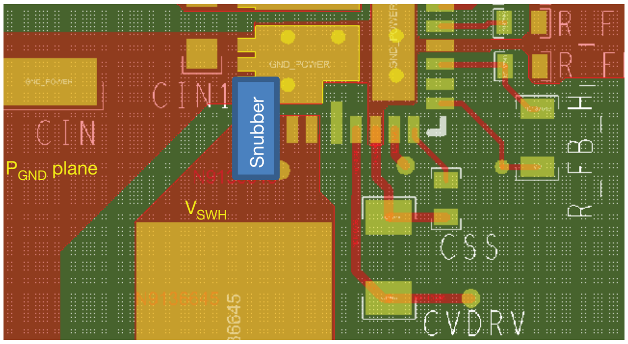


Fig. 57

1. Connect output inductor to SiC46x with large plane to lower the resistance
2. If any snubber network is required, place the components on the bottom side as shown above

Step 4: V_{DD}/V_{DRV} Input Filter

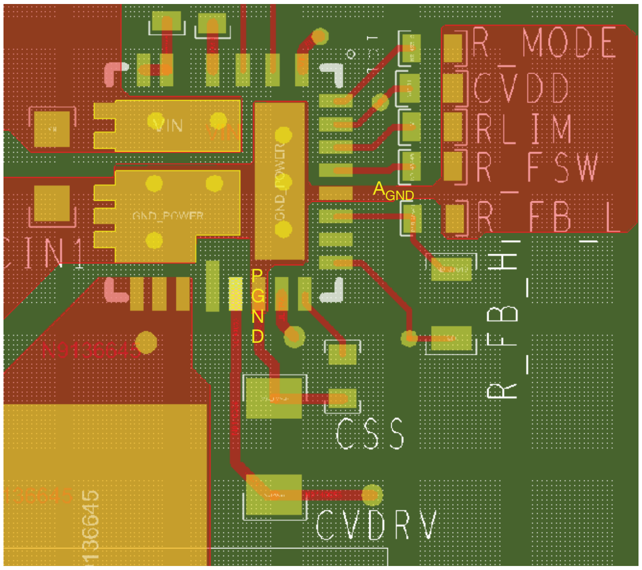


Fig. 58

1. C_{VDD} cap should be placed between pin 26 and pin 23 (the A_{GND} of driver IC) to achieve best noise filtering
2. C_{VDRV} cap should be placed close to V_{DRV} (pin 16) and P_{GND} (pin 17) to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

Step 5: BOOT Resistor and Capacitor Placement

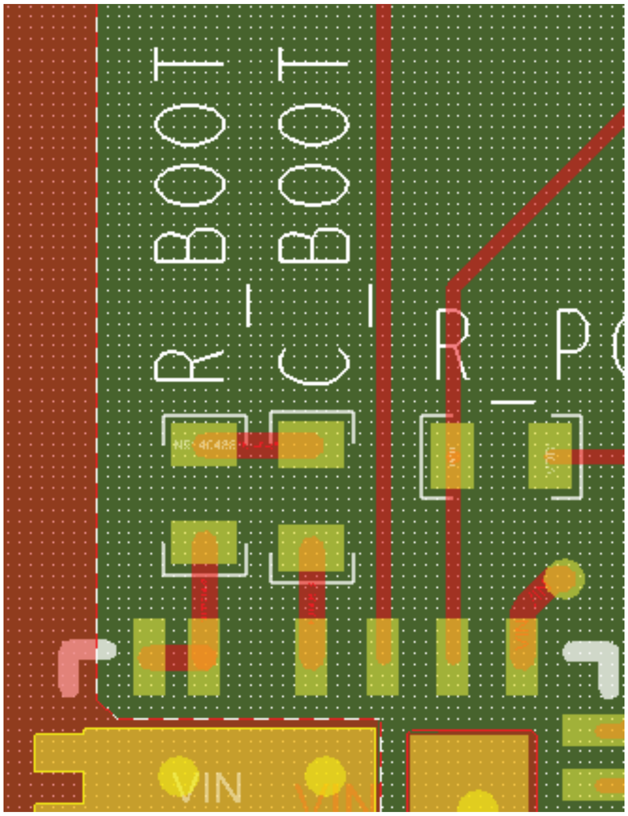


Fig. 59

1. These components need to be placed very close to SiC46x, right between PHASE (pin 5, 6) and BOOT (pin 4)
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor

Step 6: Signal Routing

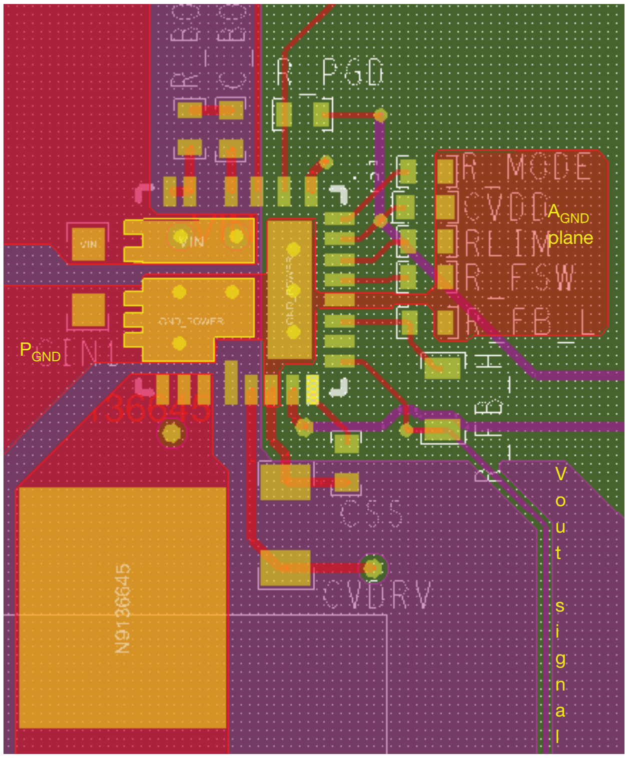


Fig. 60

1. Separate the small analog signal from high current path. As shown above, the high current paths with high dv/dt, di/dt are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. Pin 23 is the IC analog ground, which should have a single connection to power ground. The A_{GND} ground plane connected with pin 23 helps keep A_{GND} quiet and improve noise immunity
3. Feedback signal can be routed through inner layer. Make sure this signal is far away from V_{SWH} node and shielded by inner ground layer

Step 7: Adding Thermal Relief Vias and Duplicate Power Path Plane

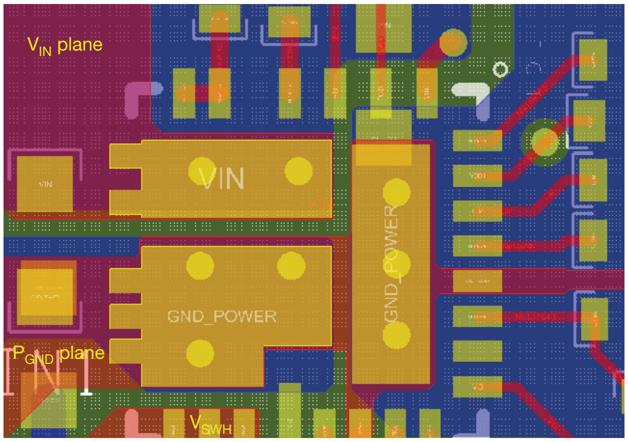


Fig. 61

1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be put on V_{IN} and P_{GND} plane. Also, it is necessary to duplicate the V_{IN} and ground planes at bottom layer to maximize the power dissipation capability from PCB.
3. V_{SWH} pad is a noise source and not recommended to put vias on this pad.
4. 8 mil drill for pads and 10 mils drill for plane are optional via sizes. The vias on pads may drain solder during assembly and cause assembly issues. Please consult with the assembly house for guidelines

Step 8: Ground Layer

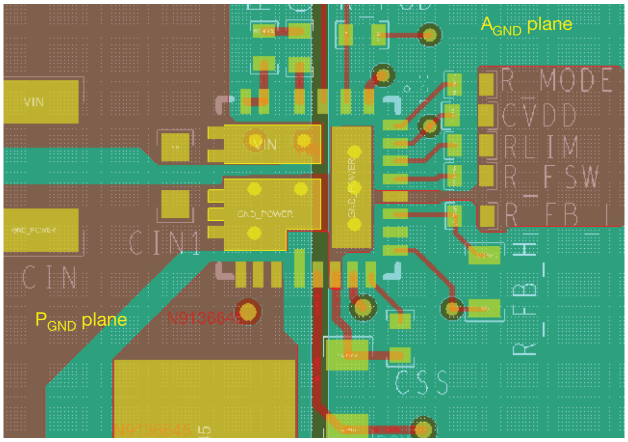


Fig. 62

1. It is recommended to make the entire inner layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer.
3. The ground plane can be broken into two sections as P_{GND} and A_{GND}

PRODUCT SUMMARY

Part number	SiC466	SiC467	SiC468	SiC469
Description	10 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous microBUCK regulator	6 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous microBUCK regulator	4 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous microBUCK regulator	2 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous microBUCK regulator
Input voltage min. (V)	4.5	4.5	4.5	4.5
Input voltage max. (V)	60	60	60	60
Output voltage min. (V)	0.8	0.8	0.8	0.8
Output voltage max. (V)	15	15	15	15
Continuous current (A)	10	6	4	2
Switch frequency min. (kHz)	100	100	100	100
Switch frequency max. (kHz)	2000	2000	2000	2000
Pre-bias operation (yes / no)	Yes	Yes	Yes	Yes
Internal bias reg. (yes / no)	Yes	Yes	Yes	Yes
Compensation	Internal	Internal	Internal	Internal
Enable (yes / no)	Yes	Yes	Yes	Yes
P_{GOOD} (yes / no)	Yes	Yes	Yes	Yes
Overcurrent protection	Yes	Yes	Yes	Yes
Protection	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Selectable powersave	Selectable powersave	Selectable powersave	Selectable powersave
Peak efficiency (%)	97	98	98	98
Package type	PowerPAK MLP55-27L	PowerPAK MLP55-27L	PowerPAK MLP55-27L	PowerPAK MLP55-27L
Package size (W, L, H) (mm)	5 x 5 x 0.75	5 x 5 x 0.75	5 x 5 x 0.75	5 x 5 x 0.75
Status code	1	1	1	1
Product type	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)
Applications	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking

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