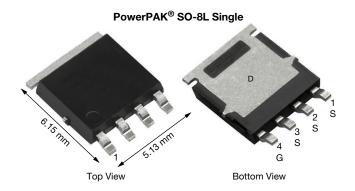


www.vishay.com

Vishay Siliconix

# Automotive N-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY					
V <sub>DS</sub> (V)	40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.00940				
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.01173				
I <sub>D</sub> (A)	20				
Configuration	Single				
Package	PowerPAK SO-8L				

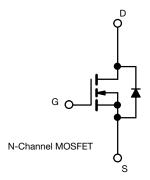
#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



ABSOLUTE MAXIMUM RATINGS	$I_C = 25  ^{\circ}C$ , unles	s otherwise noted	1)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		$V_{DS}$	40	V	
Gate-source voltage		$V_{GS}$	± 20		
Continuous drain current <sup>a</sup>	T <sub>C</sub> = 25 °C	1	20		
Continuous drain current ~	T <sub>C</sub> = 125 °C	I <sub>D</sub>	20		
Continuous source current (diode conduction	Is	20	Α		
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	80		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	18		
Single pulse avalanche energy	L = 0.1 MH	E <sub>AS</sub>	16	mJ	
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	27	W	
	T <sub>C</sub> = 125 °C		9	VV	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e		-	260	-0	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	$R_{thJA}$	70	°C/W
Junction-to-case (drain)		$R_{thJC}$	5.5	C/VV

#### Notes

- a. Package limited
- b. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static					•	l .	
Drain-source breakdown voltage	$V_{DS}$	V <sub>GS</sub>	= 0, I <sub>D</sub> = 250 μA	40	-	-	\/
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.3	1.8	2.3	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	10	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A	-	0.00770	0.00940	
Dynin anywas an atata vasiatanas 3	В	V <sub>GS</sub> = 4.5 V V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4 A	-	0.00970	0.01173	V nA μA A
Drain-source on-state resistance a	R <sub>DS(on)</sub>		I <sub>D</sub> = 6 A, T <sub>J</sub> = 125 °C	-	-	0.01370	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A, T <sub>J</sub> = 175 °C	-	-	0.01600	
Forward transconductance b	9 <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 6 A	-	32	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>			-	1197	1700	
Output capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	331	500	pF
Reverse transfer capacitance	C <sub>rss</sub>	1		-	31	50	
Total gate charge c	$Q_g$			-	22	33	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ A}$	-	3.5	-	nC
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>	1		-	3.9	-	
Gate resistance	$R_g$		f = 1 MHz	1.74	3.49	5.30	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	10	20	
Rise time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> :	= 20 V, $R_L$ = 20 $\Omega$	-	4	10	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 1 A, Y$	$V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$	-	24	50	ns
Fall time <sup>c</sup>	t <sub>f</sub>	1		-	25	50	
Source-Drain Diode Ratings and Charac	teristics <sup>b</sup>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	80	Α
Forward voltage	$V_{SD}$	I <sub>F</sub>	= 6 A, V <sub>GS</sub> = 0	-	0.77	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>			-	28	60	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	] , ,	۸ ما:/ملد ۱۰۰۱ ۸ /۰۰۰	-	17	35	nC
Reverse recovery fall time	ta	I <sub>F</sub> = 1.	A, di/dt = 100 A/μs	-	14	-	
Reverse recovery rise time	t <sub>b</sub>	1		-	14	-	пs
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-1.1	-	Α

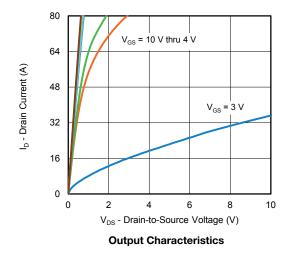
### **Notes**

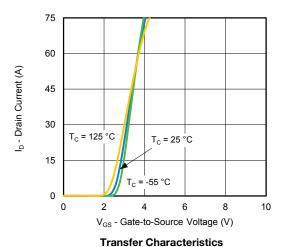
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

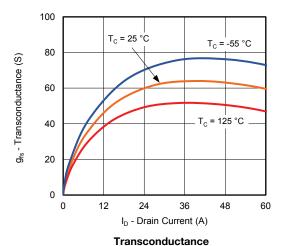
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

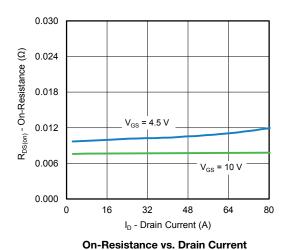


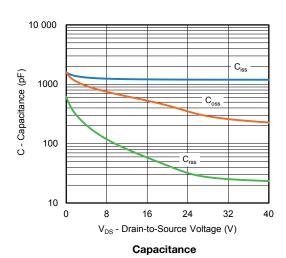
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

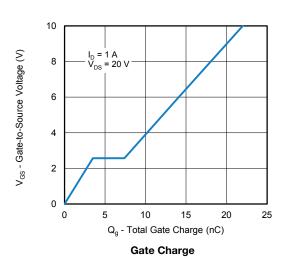






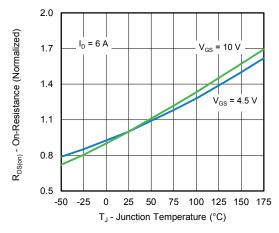




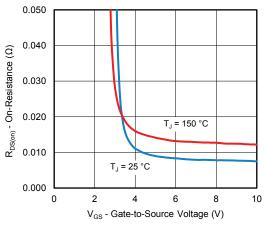




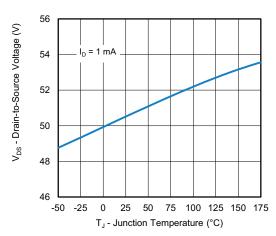
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



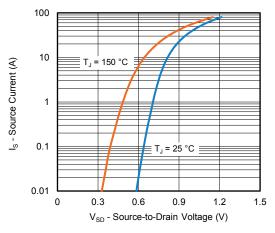
On-Resistance vs. Junction Temperature



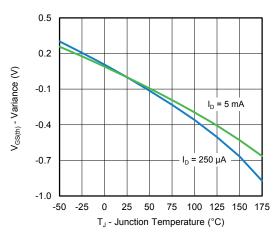
On-Resistance vs. Gate-to Source Voltage



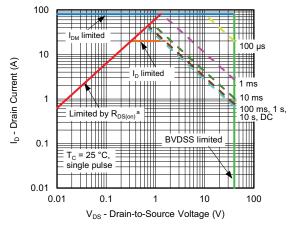
Drain Source Breakdown vs. Junction Temperature



**Source Drain Diode Forward Voltage** 



Threshold Voltage



Safe Operating Area

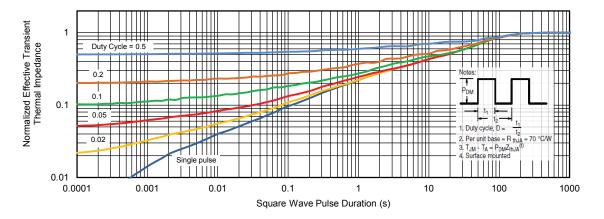
#### Note

a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

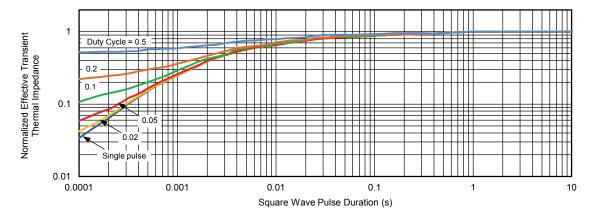
For technical questions, contact: automostech



## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

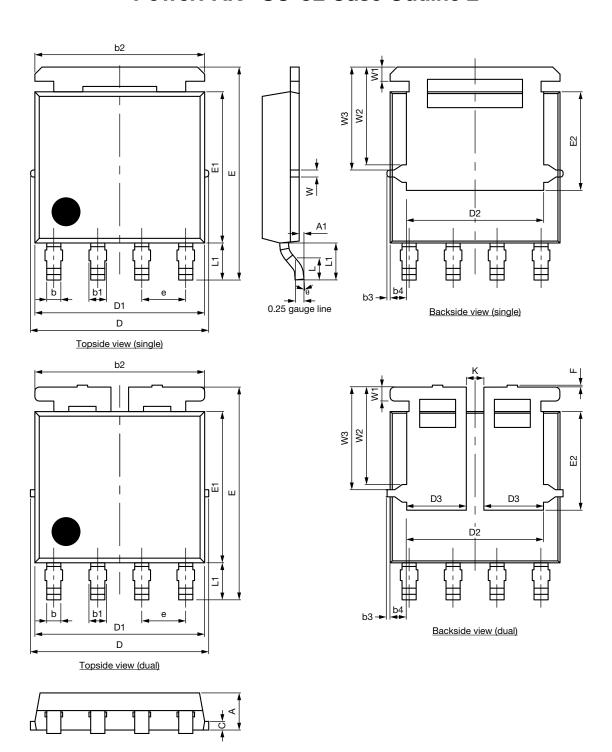
#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76936.



# PowerPAK® SO-8L Case Outline 2



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DIM.		MILLIMETERS		INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
А	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3		0.094		0.004		
b4		0.47			0.019	
С	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
е		1.27 BSC		0.050 BSC		
Е	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K		0.51			0.020	
W	0.23		0.009			
W1	0.41		0.016			
W2	2.82		0.111			
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°

ECN: C21-1498-Rev. C, 01-Nov-2021

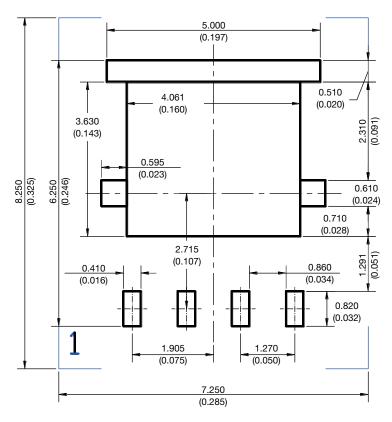
DWG: 6044

### Note

• Millimeters will govern



## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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