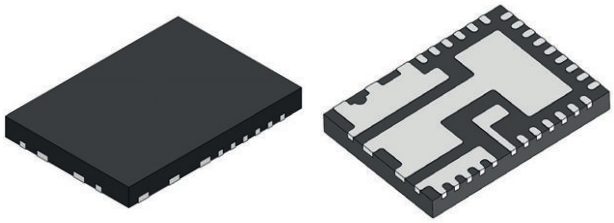
# 4.5 V to 20 V Input, 15 A, 25 A, 40 A microBuck® DC/DC Converter With PMBus Interface



## LINKS TO ADDITIONAL RESOURCES

PowerCAD Design Tool | Evaluation Boards | Design Tools

## DESCRIPTION

The SiC45x is a PMBus 1.3 compliant non-isolated DC/DC buck regulator with integrated MOSFETs. It is capable of supplying up to 40 A (SiC450) continuous output current. Its output voltage is digitally adjustable from 0.3 V to 12 V from a 4.5 V to 20 V input with switching frequencies up to 1.5 MHz.

SiC45x architecture delivers ultrafast transient response with minimum output capacitance and tight regulation over a broad load range. The device has integrated internal compensation and is stable with any type of output capacitor. The device incorporates a power saving scheme that significantly increases light load efficiency.

The SiC45x allows power block configuration programs to be stored in non volatile memory (NVM). Various operation parameters can all be locally stored and used to determine fault behavior. Operation is firmware based and is field upgradable Pinstrap option is also available for default configuration without PMBus.

The SiC45x is available in lead (Pb)-free power enhanced MLP 5 mm x 7 mm package.

## TYPICAL APPLICATION CIRCUIT

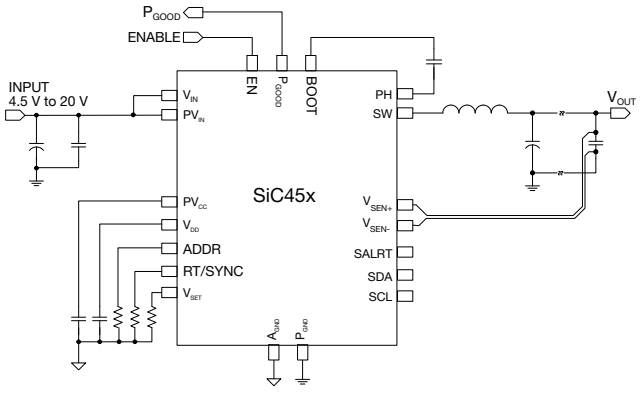



**Fig. 1 - Typical Application Circuit**

## FEATURES

- Versatile
  - Single supply operation from 4.5 V to 20 V input voltage
  - Scalable solution with continuous output current of 40 A (SiC450), 25 A (SiC451), 15 A (SiC453)
  - Continuous current of SiC451 by $V_{OUT}$ range
    - 30 A at $V_{OUT} < 2.5$ V
    - 25 A at $V_{OUT} \geq 2.5$ V
  - Adjustable output voltage from 0.3 V to 12 V
  - Built in 5 V regulator for internal circuits and driver supply
  - 1 % output voltage accuracy over temperature
  - 0.5 % output accuracy at $V_{OUT} = 3.3$ V / 1.8 V, $T_A = 25$ °C
  - Ultrafast transient response
- Highly efficient
  - 98 % peak efficiency
  - Optional power save mode
- Highly configurable
  - PMBus 1.3 compliant with 1 MHz bus speed
  - Internal NVM
  - $V_{OUT}$ adjustability and reading resolution of 2 mV
  - Supports over 50 PMBus commands
  - Supports in phase or 180° out of phase synchronization
  - Output voltage source and sink capability
- Robust and reliable
  - $PV_{IN}$, $V_{OUT}$, $I_{IN}$ and $I_{OUT}$ and temperature reporting
  - Over current protection in pulse-by-pulse mode
  - Output over and under voltage protection
  - Over temperature protection with hysteresis
  - Differential output remote sensing

RoHS COMPLIANT HALOGEN FREE

## APPLICATIONS

- Server, cloud, and infrastructure
- Networking, telecom, storage applications
- Distributed point of load power architectures
- DDR memory

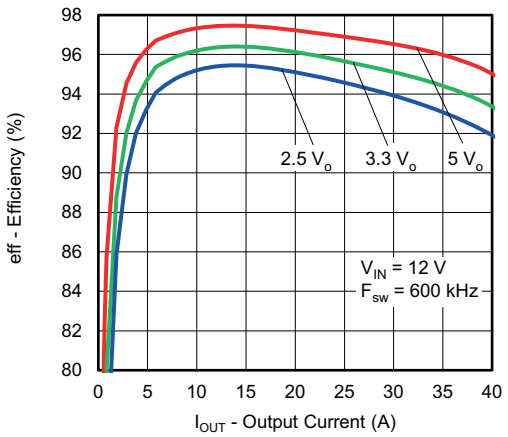



**Fig. 2 - SiC450 Efficiency Curve**

## PIN CONFIGURATION

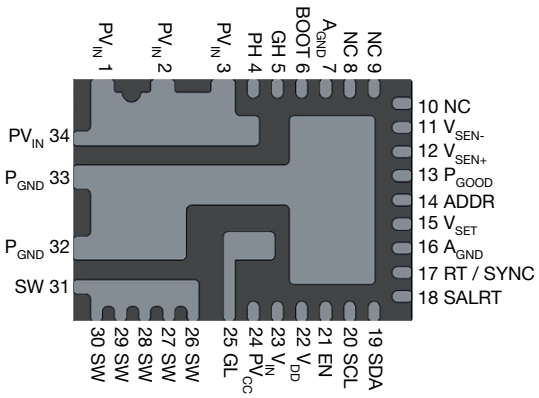
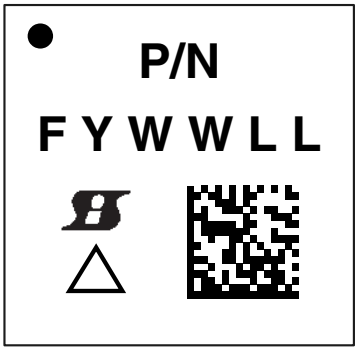



**Fig. 3 - Pin Configuration - Bottom View**

| PIN DESCRIPTION | | |
|---|---|---|
| **PIN NUMBER** | **SYMBOL** | **DESCRIPTION** |
| 1, 2, 3, 34 | $PV_{IN}$ | Input voltage for power stage |
| 4 | PH | Phase node, return path of high side gate driver |
| 5 | GH | High side MOSFET gate monitor |
| 6 | BOOT | Bootstrap voltage for high side gate driver (referenced to PH) |
| 7, 16 | $A_{GND}$ | Analog signal return ground |
| 8 | NC | Not used in Vishay device |
| 9 | NC | Not used in Vishay device |
| 10 | NC | Not used in Vishay device |
| 11 | $V_{SEN-}$ | Remote sense amplifier negative input connect to output ground |
| 12 | $V_{SEN+}$ | Remote sense amplifier positive input connect to output |
| 13 | $P_{GOOD}$ | Power good; open-drain output indicating $V_{OUT}$ is within set limits. Connect a pull up resistor typically 10 kΩ to $V_{DD}$ |
| 14 | ADDR | PMBus address programming pin |
| 15 | $V_{SET}$ | Output voltage set point by connecting a resistor from $V_{SET}$ to $A_{GND}$ |
| 17 | RT/SYNC | Clock synchronization pin. Frequency can be set by connecting a resistor to $A_{GND}$.<br>Pending on master / salve configuration, a clock can be send / receive via the pin |
| 18 | SALRT | PMBus alert. Connect to external host interface if desired |
| 19 | SDA | PMBus data. Connect to external host interface |
| 20 | SCL | PMBus clock. Connect to external host interface |
| 21 | EN | Enable pin. Active high 5 V logic level input |
| 22 | $V_{DD}$ | Internal 5 V circuits supply voltage. $V_{DD}$ is a LDO output, connect a 1 µF decoupling capacitor to $A_{GND}$ |
| 23 | $V_{IN}$ | Internal driver supply voltage |
| 24 | $PV_{CC}$ | Supply voltage for internal gate drive. $PV_{CC}$ is a LDO output. Connect a 4.7 µF decoupling capacitor to $P_{GND}$ |
| 25 | GL | Low side MOSFET gate monitor |
| 26 to 31 | SW | Switch node |
| 32, 33 | $P_{GND}$ | Power ground. Common return for internal MOSFETs |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **PART NUMBER** | **PART MARKING** | **MAXIMUM CURRENT** | **PACKAGE** |
| SiC450ED-T1-GE3 | SiC450 | 40 A | PowerPAK MLP34-57 |
| SiC450EVB | Reference board | | |
| SiC451ED-T1-GE3 | SiC451 | 25 A | PowerPAK MLP34-57 |
| SiC451EVB | Reference board | | |
| SiC453ED-T1-GE3 | SiC453 | 15 A | PowerPAK MLP34-57 |
| SiC453EVB | Reference board | | |

## PART MARKING INFORMATION




- ● = pin 1 indicator
- P/N = part number code
- Siliconix logo
- △ = ESD symbol
- F = assembly factory code
- Y = year code
- WW = week code
- LL = lot code

| **ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted) | | | |
|---|---|---|---|
| **ELECTRICAL PARAMETER** | **CONDITIONS** | **LIMITS** | **UNIT** |
| $PV_{IN}$, $V_{IN}$ | Reference to $P_{GND}$ | -0.3 to +28 | V |
| Switching FETs break down voltage | Drain to source | +28 | |
| SW / PH | Reference to $P_{GND}$ | -0.3 to +28 | |
| SW / PH (AC) | Reference to $P_{GND}$ (100 ns) | -8 to +33 | |
| BOOT | | -0.3 to $V_{PH}$ + $P_{VCC}$ | |
| BOOT to SW | | -0.3 to +6 | |
| Drive supply voltage ($PV_{CC}$) | | -0.3 to +6 | |
| Bias supply voltage ($V_{DD}$) | | -0.3 to +6 | |
| $A_{GND}$ to $P_{GND}$ | | -0.3 to +0.3 | |
| All other pins | Reference to $A_{GND}$ | -0.3 to $V_{DD}$ + 0.3 | |
| **Temperature** | | | |
| Junction temperature | | -40 to +150 | °C |
| Storage temperature | | -65 to +150 | |
| **Power Dissipation** | | | |
| Junction-to-ambient thermal impedance ($R_{thJA}$) | | 24 | °C/W |
| Thermal resistance from junction to case ($R_{thJ-C}$) | | 4.5 | |
| Thermal resistance from junction to PCB ($R_{thJ-PCB}$) | | 5 | |
| **ESD Protection** | | | |
| Electrostatic discharge protection | HBM | 2 | kV |
| | CDM | 750 | V |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating / conditions for extended periods may affect device reliability.*

| **RECOMMENDED OPERATING CONDITIONS** (all voltages referenced to GND = 0 V) | | | | |
|---|---|---|---|---|
| **ELECTRICAL PARAMETER** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| $PV_{IN}$, $V_{IN}$ | 4.5 | - | 20 | V |
| Logic pins | 0 | - | 5.5 | |
| $V_{OUT}$ | 0.3 | - | 12 | |
| Drive supply voltage ($P_{VCC}$) | 4.75 | 5 | 5.25 | |
| Bias supply voltage ($V_{DD}$) | 4.75 | 5 | 5.25 | |
| **Temperature** | | | | |
| Recommended ambient temperature | -40 to +85 | | | °C |
| Operating junction temperature | -40 to +125 | | | |

| **ELECTRICAL SPECIFICATIONS** ($PV_{IN}$ = 12 V, $T_J$ = -40 °C to +125 °C, unless otherwise specified) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **LIMITS** | | | **UNIT** |
| | | | **MIN.** | **TYP.** | **MAX.** | |
| **Power Supplies** | | | | | | |
| $PV_{IN}$, $V_{IN}$ | $PV_{IN}$, $V_{IN}$ | | 4.5 | - | 20 | V |
| $V_{IN\_ON,\ default}$ | $V_{IN\_ON}$ | Default setting | - | 10 | - | |
| $V_{IN\_OFF,\ default}$ | $V_{IN\_OFF}$ | Default setting | - | 9 | - | |
| $PV_{CC}$ supply | $V_{PVCC}$ | $V_{IN}$ = 4.5 V to 20 V | 4.5 | 5 | 5.5 | |
| $V_{DD}$ supply | $V_{DD}$ | Logic supply voltage | 4.5 | 5 | 5.5 | |
| $PV_{CC}$ UVLO threshold | $V_{PVCC\_UVLO\_TH}$ | | 3.4 | 3.6 | 3.8 | |
| $PV_{CC}$ UVLO hysteresis | $V_{PVCC\_UVLO\_HYS}$ | | - | 300 | - | mV |
| Input current | $I_{VIN}$ | $T_J$ = 25 °C, non-switching, no load, $V_{OUT} > V_{SET}$ | - | 3.5 | 6 | mA |
| Shutdown current | $I_{VIN\_SDN}$ | EN = 0 V, $I_{PVCC} + I_{PVDD} + I_{PVIN}$ | - | 2.5 | 6 | |
| **$PV_{IN}$ Monitoring** | | | | | | |
| $PV_{IN}$ monitor accuracy | $V_{PVIN\_MON\_ACC}$ | | - | 3 | - | % |
| $PV_{IN}$ min. monitor resolution | $V_{PVIN\_MON\_RSO}$ | | - | 70 | - | mV |
| $PV_{IN}$ monitor full scale | $V_{PVIN\_MON\_SCL}$ | | - | - | 28 | V |
| $PV_{IN}$ read frequency | $t_{PVIN\_RSP}$ | | - | 78 | - | Hz |
| **$I_{IN}$ Fault Response Time** | | | | | | |
| $I_{IN}$ fault response time | $t_{IIN\_RSP}$ | $I_{IN\_OC\_WARN}$ | - | 78 | - | Hz |
| **Pin (Input power)** | | | | | | |
| Pin sense accuracy | $P_{PVIN\_SNS\_ACC}$ | 5 W to 160 W | - | 5 | - | % |
| Pin sense resolution | $P_{PVIN\_SNS\_RSO}$ | | - | 0.5 | - | W |
| **Output Voltage** | | | | | | |
| $V_{OUT}$ default set-point | $V_{OUT}$ | $V_{SET}$ resistor = OPEN or SHORT | - | 0.6 | - | V |
| $V_{OUT}$ set-point accuracy | $V_{OUT\_ACC}$ | Measured as $\Delta V$ ($V_{SEN+}$ - $V_{SEN-}$) | -1 | - | 1 | % |
| | | Measured as $\Delta V$ ($V_{SEN+}$ - $V_{SEN-}$), $V_{IN}$ = 12 V, $V_O$ = 3.3 V and $T_A$ = 25 °C | -0.5 | - | +0.5 | |
| | | Measured as $\Delta V$ ($V_{SEN+}$ - $V_{SEN-}$), $V_{IN}$ = 12 V, $V_O$ = 1.8 V and $T_A$ = 25 °C | -0.5 | - | +0.5 | |
| $V_{OUT}$ set-point range | $V_{OUT\_RNG}$ | | 0.3 | - | 12 | V |
| $V_{OUT}$ set-point resolution | $V_{OUT\_RSO}$ | | - | 2 | - | mV |
| Line regulation | $V_{OUT\_REG}$ | | - | 1 | - | % |
| Load regulation | $V_{OUT\_REG}$ | | - | 1 | - | |
| $V_{OUT}$ min. monitor resolution | $V_{OUT\_MON\_RSO}$ | $V_{OUT}$ scale loop = 1 | - | 5 | - | mV |
| $V_{OUT}$ start up delay range | $t_{S\_DLY\_RNG}$ | From $PV_{IN}$ valid until 1st PWM pulse | - | 0 | - | ms |
| $V_{SEN+}$ common mode range | $V_{VSNS\_RNG}$ | | -0.2 | - | 12 | V |
| $V_{SEN-}$ common mode range | $V_{VSNS\_RNG}$ | | -200 | - | 200 | mV |
| $V_{OUT}$ read conversion frequency | $t_{VOUT\_RSP}$ | | - | 78 | - | Hz |
| **Controller and Timing** | | | | | | |
| Minimum on-time | $t_{ON\_MIN}$ | | - | 50 | - | ns |
| Minimum off-time | $t_{OFF\_MIN}$ | | - | 250 | - | |
| $t_{ON}$ accuracy | $t_{ON\_ACC}$ | | -10 | - | 10 | % |
| Frequency, default | $f_{SW}$ | | 540 | 600 | 660 | kHz |
| Frequency setting range | $f_{SW\_RNG}$ | CCM mode | 300 | - | 1500 | |

| **ELECTRICAL SPECIFICATIONS** ($PV_{IN}$ = 12 V, $T_J$ = -40 °C to +125 °C, unless otherwise specified) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **LIMITS** | | | **UNIT** |
| | | | **MIN.** | **TYP.** | **MAX.** | |
| **$V_{OUT}$ Soft Start / Soft Stop** | | | | | | |
| $t_{ON}$ rise, default | $t_{ON\_RISE}$ | From $V_{OUT}$ = 0 V to $V_{OUT}$ set point | - | 5 | - | ms |
| $t_{ON}$ rise, setting range | $t_{ON\_RNG}$ | | 0 | - | 127 | |
| $t_{OFF}$ fall, default | $t_{SSP}$ | | - | 5 | - | |
| $t_{OFF}$ fall, setting range | $t_{SSP,RNG}$ | | 0 | - | 127 | |
| $t_{ON}$ delay, default | $t_{ON\_DLY}$ | From $V_{OUT}$ = 0 V to $V_{OUT}$ set point | - | 0 | - | |
| $t_{ON}$ delay, setting range | $t_{ON\_DLY,RNG}$ | | 0 | - | 127 | |
| $t_{OFF}$ delay, default | $t_{OFF\_DLY}$ | | - | 0 | - | |
| $t_{OFF}$ delay, setting range | $t_{OFF\_DLY,RNG}$ | | 0 | - | 127 | |
| $t_{ON}$ max. fault limit, default | $t_{max\_FLT}$ | | - | 20 | - | |
| $t_{ON}$ max. fault limit, setting range | $t_{max\_FLT,RNG}$ | | 0 | - | 127 | |
| **Enable** | | | | | | |
| EN pull down resistance | $R_{EN}$ | | - | 5 | - | MΩ |
| **RT/SYNC** | | | | | | |
| Logic high level | $V_{RT/SYNC\_HI}$ | | 2 | - | - | V |
| Logic low level | $V_{RT/SYNC\_LO}$ | | - | - | 0.8 | |
| Input minimum pulse width | $t_{IN\ Pulse\_min}$ | | - | 100 | - | ns |
| Sync switching | $F_{SYNC}$ | | 300 | - | 1500 | kHz |
| **Power Good** | | | | | | |
| Power good output rising threshold | $V_{FB\_RISING\_TH}$ | Default value respect to $V_{OUT}$ default setting = 0.6 V | - | 90 | - | % |
| Power good output falling threshold | $V_{FB\_FALLING\_TH}$ | | - | 85 | - | |
| Power good hysteresis | $V_{FB\_HYST}$ | | - | 5 | - | |
| Power good on resistance | $R_{PG}$ | | - | 5.5 | - | Ω |
| Power good delay time (rising) | $t_{PG\_RISE\_DLY}$ | | - | 25 | - | µs |
| Power good delay time (falling) | $t_{PG\_FALL\_DLY}$ | | - | 100 | - | |
| **Temperature Monitor and Temperature Shutdown** | | | | | | |
| Monitoring resolution | $T_{MON\_RSO}$ | | - | 1 | - | °C |
| Monitoring range | $T_{MON\_RNG}$ | | -40 | - | +150 | |
| Monitoring accuracy | $T_{MON\_ACC}$ | | -5 | - | +5 | |
| Thermal shutdown | $T_{SD}$ | | - | 125 | - | |
| Thermal shutdown hysteresis | $T_{SD\_HYS}$ | | - | 35 | - | |
| **Digital Inputs (ADDR, SALRT, SCLK, SDA, EN)** | | | | | | |
| Input high threshold | $V_{IH}$ | | 2 | - | - | V |
| Input low threshold | $V_{IL}$ | | - | - | 0.8 | |
| Input hysteresis | $V_{HYST}$ | | - | 0.1 | - | |
| Pin capacitance | $C_{PIN}$ | | - | 5 | - | pF |
| **Fault Protections** | | | | | | |
| Valley current limit, default | $I_{OCP}$ | SiC450 (40 A), $T_J$ = -40 °C to +85 °C | - | 56 | - | A |
| | | SiC451 (25 A), $T_J$ = -40 °C to +85 °C | - | 35 | - | |
| | | SiC453 (15 A), $T_J$ = -40 °C to +85 °C | - | 21 | - | |
| Output OVP threshold, default | $V_{OVP}$ | $V_{OUT}$ with respect to $V_{SET}$ | - | 115 | - | % |
| Output UVP threshold, default | $V_{UVP}$ | | - | 80 | - | |

| **ELECTRICAL SPECIFICATIONS** ($PV_{IN}$ = 12 V, $T_J$ = -40 °C to +125 °C, unless otherwise specified) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **LIMITS** | | | **UNIT** |
| | | | **MIN.** | **TYP.** | **MAX.** | |
| **Telemetry** | | | | | | |
| $V_{IN}$ | $V_{IN}$ | Load current, 20 % to 100 % ($T_A$ = -40 °C to +125 °C) | -3 | - | 3 | % |
| $I_{IN}$ | $I_{IN}$ | 20 % of load current ($T_A$ = 25 °C) | -15 | - | 15 | |
| | | 50 % of load current ($T_A$ = 25 °C) | -6 | - | 6 | |
| | | 100 % of load current ($T_A$ = 25 °C) | -5 | - | 5 | |
| $P_{IN}$ | $P_{IN}$ | 20 % of load current ($T_A$ = 25 °C) | -9 | - | 9 | |
| | | 50 % of load current ($T_A$ = 25 °C) | -4 | - | 4 | |
| | | 100 % of load current ($T_A$ = 25 °C) | -3 | - | 3 | |
| $V_{OUT}$ | $V_{OUT}$ | 2 V < $V_{OUT}$ < 5.5 V, load current, 20 % to 100 % ($T_A$ = -40 °C to +125 °C) | -1.5 | - | 1.5 | |
| | | 0.5 V < $V_{OUT}$ < 2 V, load current, 20 % to 100 % ($T_A$ = -40 °C to +125 °C) | -2 | - | 2 | |
| $I_{OUT}$ | $I_{OUT}$ | 20 % of load current ($T_A$ = 25 °C) | -12 | - | 12 | |
| | | 50 % of load current ($T_A$ = 25 °C) | -4 | - | 4 | |
| | | 100 % of load current ($T_A$ = 25 °C) | -3 | - | 3 | |
| $P_{OUT}$ | $P_{OUT}$ | 20 % of load current ($T_A$ = 25 °C) | -9 | - | 9 | |
| | | 50 % of load current ($T_A$ = 25 °C) | -4 | - | 4 | |
| | | 100 % of load current ($T_A$ = 25 °C) | -3 | - | 3 | |

## FUNCTIONAL BLOCK DIAGRAM

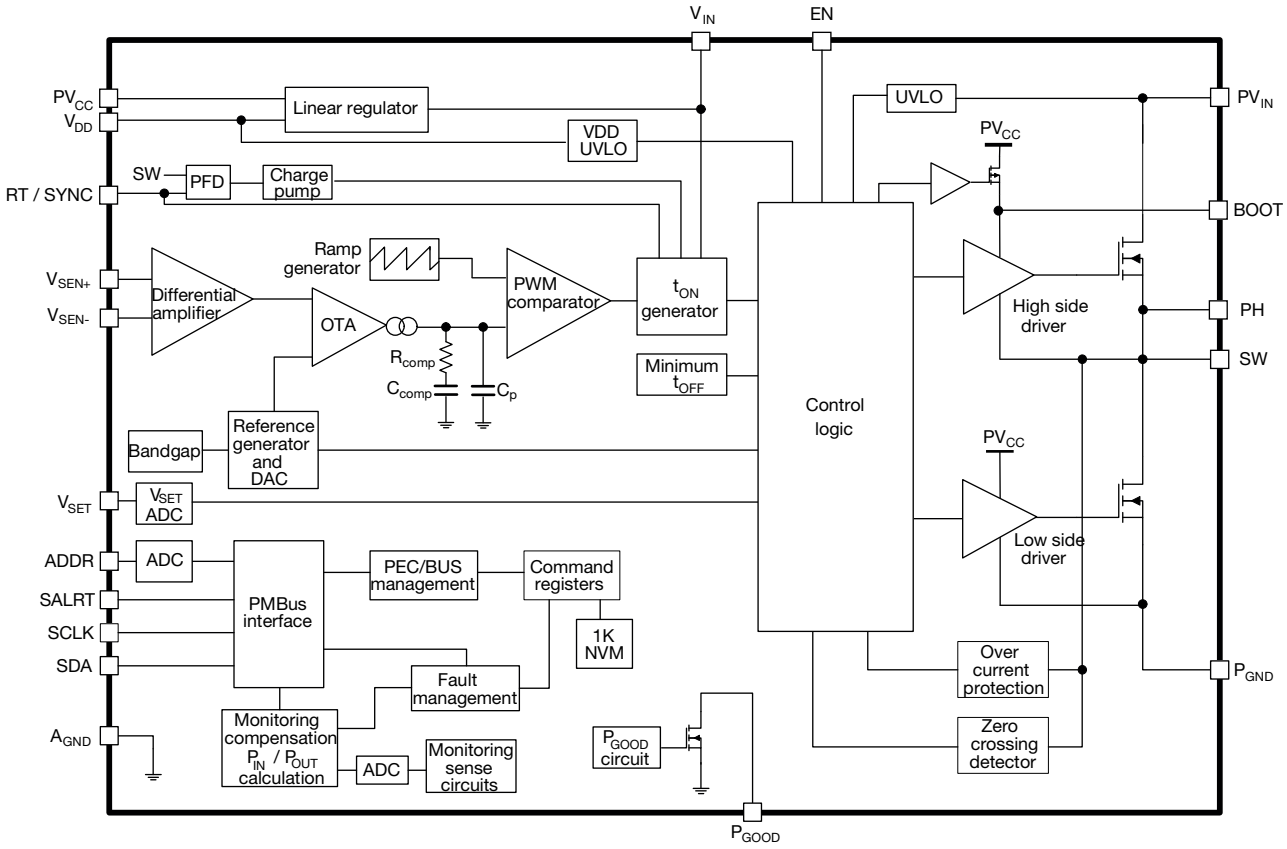



**Fig. 4 - Functional Block Diagram**

## OPERATIONAL DESCRIPTION

### Device Overview

SiC45x is a high efficiency synchronous buck regulator capable of delivering up to 25 A continuous current. The device has programmable switching frequency of 300 kHz to 1.5 MHz. The control scheme delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency fold back as the load decreases.

In addition, a built in PLL allows in phase or 180° out of phase synchronization under master / slave configuration.

SiC45x has a full set of protection and monitoring features with response that can be set with PMBus:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in MLP34-57 package to deliver high power density and minimize PCB area.

### PWM Control Mechanism

SiC45x employs a voltage - mode COT control mechanism. During steady-state operation, feedback voltage is compared with internal reference and the amplified error signal ($V_{COMP}$) is generated in the internal comp node. An internally generated ramp signal and $V_{COMP}$ are fed into a comparator. Once $V_{RAMP}$ crosses $V_{COMP}$, a single shot on-time pulse is generated for a fixed time, programmed by the external $R_{fsw}$. During the on-time pulse, the high side MOSFET will be turned on. Once the on-time pulse expires, the low side MOSFET will be turned on after a break-before-make period. The low side MOSFET will be on for duration of minimum off-time pulse until $V_{RAMP}$ crosses $V_{COMP}$. The cycle is then repeated.

Fig. 5 illustrates the basic block diagram for VM-COT architecture. In this architecture the following is achieved:

- The reference of a basic ripple control regulator is replaced with a high again error amplifier loop
- This establishes two parallel voltage regulating feedback paths, a fast and slow path
- Fast path is the ripple injection which ensures rapid correction of the transient perturbation
- Slow path is the error amplifier loop which ensures the DC component of the output voltage follows the internal accurate reference voltage

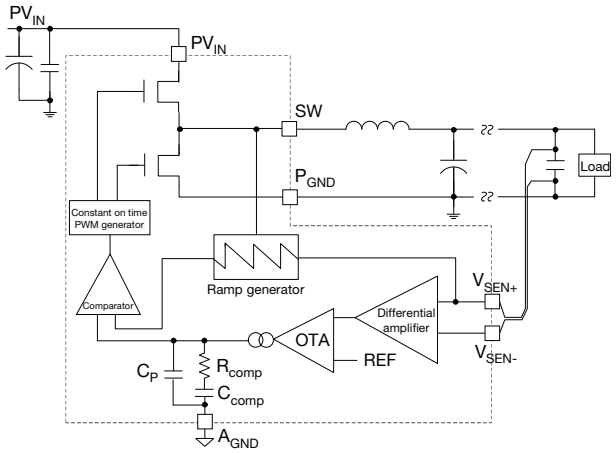



**Fig. 5 - VM-COT Block Diagram**

All components for RAMP signal generation and error amplifier compensation required for the control loop are internal to the IC, see Fig. 5. In order for the device to cover a wide range of $V_{OUT}$ operation, the internal RAMP signal components are automatically selected depending on the $V_{OUT}$ voltage and switching frequency. The error amplifier internal compensation consists of a resistor in series with a capacitor ($R_{COMP}$, $C_{COMP}$).

Fig. 6 demonstrates the basic operational waveforms:

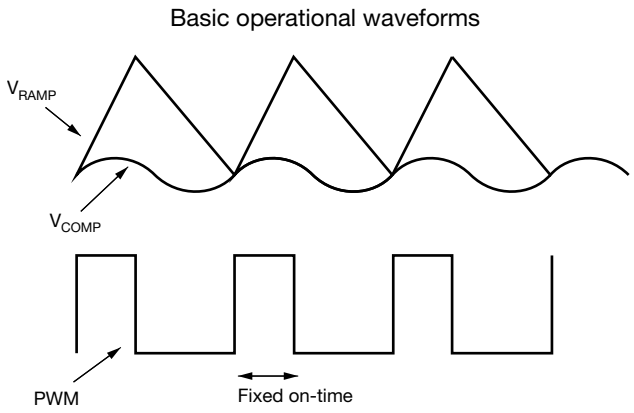



**Fig. 6 - VM-COT Operational Principle**

### Light Load Condition

To improve efficiency at light-load condition, SiC45x provide a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal zero crossing detector monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device deploys diode emulation mode by turning off low side MOSFET. If load further decreases, switching frequency is reduced proportional to load condition to save switching losses while keeping output ripple within

tolerance. The switching frequency is set by the controller to maintain regulation. In the standard power save mode, there is no minimum switching frequency. If ultrasonic mode is selected via PMBus, the minimum switching frequency that the regulator will reduce to is > 20 kHz as the part avoids switching frequencies in the audible range.

### Power Stage

SiC45x integrates a high performance power stage with a 4 mΩ n-channel high side MOSFET and a 1.4 mΩ n-channel low side MOSFET. The MOSFETs are optimized to achieve up to 96 % efficiency.

The power input voltage ($PV_{IN}$) can go up to 20 V and down as low as 4.5 V. The output voltage must always be less than the input voltage.

### Sequencing of Input / Output Supplies

SiC45x has no sequencing requirements on any of its input / output, $PV_{IN}$, $PV_{CC}$, $V_{IN}$, $V_{DD}$ and EN. $V_{IN}$ is internal supply voltage and is used to implement on time of COT control. $V_{IN}$ shall be directly connected to $PV_{IN}$.

### EN

The SiC45x has an EN pin to turn the part on and off. Driving this pin high enables the device, while grounding it turns it off.

There are no sequencing requirements with respect to input / output supplies.

### Output Overcurrent Protection (OCP)

SiC45x has pulse-by-pulse overcurrent (OC) limit control. The inductor valley current is monitored during low-side (LS) FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the valley current is compared with an internal OCP threshold named IOUT_OC_FAULT_LIMIT, which can be programmed via PMBus. Once monitored valley current is larger than IOUT_OC_FAULT_LIMIT, a pulse-by-pulse over-current limit is broken, high-side (HS) turn-on pulse is skipped and LS FET is kept on until the inductor valley current returns below OCP limit as illustrated by Fig. 7.

An equation is given in (1) to calculate IOUT_OC_FAULT_LIMIT from steady-state value of DC load current when OCP happens.

$$\text{IOUT\_OC\_FAULT\_LIMIT} = I_{OUT\_OCP} - \frac{(PV_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times PV_{IN} \times f_{SW}} \quad (1)$$

where: IOUT_OC_FAULT_LIMIT is the OCP threshold to be programmed via PMBus; $I_{OUT\_OCP}$ is the steady-state value of DC load current when pulse-by-pulse OC event happens; $PV_{IN}$ is the input voltage for power stage; $V_{OUT}$ is the output voltage for power stage; L is inductance of power inductor; and $f_{SW}$ is switching frequency for power stage.

SiC45x also provides secondary level OCP protection. If the pulse-by-pulse overcurrent limit is persistently broken for more than a specific number of consecutive switching pulses in a row, secondary level OC fault is recognized and both HS and LS MOSFETs are turned off. The device continues restart attempt in a delay time until the OC fault condition no longer exists.

The consecutive switching pulse in a row, the delay time, and other types of fault responses can be programmed via PMBus (see PMBus command section). The default number is 128 for counting consecutive switching pulse in a row. The default delay time is 20 ms.

The OCP is enabled immediately after $V_{DD}$ passes UVLO level.

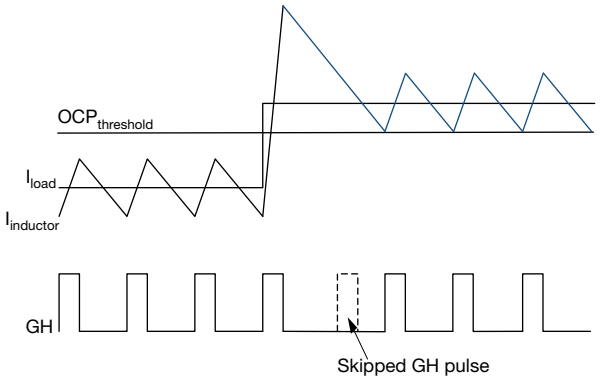



**Fig. 7 - Over-Current Protection Illustration**

### Power Good

Power good is an open-drain output. Pull $P_{GOOD}$ pin high up to 5 V through a 10K resistor to use this signal.

- $P_{GOOD}$ rising threshold and falling threshold are adjustable by using VOUT_PGOOD_ON (5Eh) and VOUT_PGOOD_OFF (5Fh) commands
- $P_{GOOD}$ signal also goes low when output voltage is above a threshold voltage ($V_{OFL}$)

### Output Undervoltage Protection (UVP)

UVP is implemented by monitoring the output voltage. If the output voltage drops below a threshold voltage $V_{OUT\_UV\_FAULT\_LIMIT}$ ($V_{UFL}$), the output-undervoltage (UV) fault condition is recognized and both the HS and LS MOSFETs are turned off. The device continues restart attempt in a delay time until the UV condition no longer exists.

The $V_{UFL}$ and the delay time can be programmed via PMBus (see PMBus command section). The default value of $V_{UFL}$ is 20 % less than the target $V_{OUT}$. The default delay time is 20 ms.

The UVP is only active after the completion of soft-start sequence.

### Output-Overvoltage Protection (OVP)

OVP is implemented by monitoring the output voltage. If the output voltage is above a threshold voltage $V_{OUT\_OV\_FAULT\_LIMIT}$ ($V_{OFL}$), the output-overvoltage (OV) fault condition is recognized and both the HS and LS MOSFETs are turned off. The device restarts when the OV fault condition no longer exists.

The UVFL can be programmed via PMBus (see PMBus command section). The default value of $V_{OFL}$ is 15 % more than the target $V_{OUT}$.

The OVP is enabled immediately after $V_{DD}$ passes UVLO level.

### Input-Overvoltage Protection ($V_{IN\text{-}OVP}$)

$V_{IN\text{-}OVP}$ is implemented by monitoring the input voltage. When the input voltage is pulled above a threshold voltage $V_{IN\_OV\_FAULT\_LIMIT}$ ($V_{IN\text{-}OFL}$), the input-overvoltage ($V_{IN\text{-}OV}$) fault condition is recognized and both the HS and LS MOSFETs are turned off. When the input voltage is pulled below the $V_{IN\text{-}OFL}$, the $V_{IN\text{-}OV}$ fault condition no longer exists and the device restarts.

The $V_{IN\text{-}OFL}$ can be programmed via PMBus (see PMBus command section). The default value of $V_{IN\text{-}OFL}$ is 15 V.

The $V_{IN\text{-}OVP}$ is enabled immediately after $V_{DD}$ passes UVLO level.

### Input-Undervoltage Protection ($V_{IN\text{-}UVP}$)

$V_{IN\text{-}UVP}$ is implemented by monitoring the input voltage. When the input voltage is pulled below a threshold $V_{IN\_OFF}$, the input-undervoltage ($V_{IN\text{-}UV}$) fault condition is recognized and both the HS and LS MOSFETs are turned off. When the input voltage is pulled above a threshold $V_{IN\_ON}$, the $V_{IN\text{-}UV}$ fault condition no longer exists and the device restarts.

The $V_{IN\text{-}OFF}$ and $V_{IN\_ON}$ can be programmed via PMBus (see PMBus command section). The default value of $V_{IN\text{-}OFF}$ is 9 V. The default value of $V_{IN\_ON}$ is 10 V.

The $V_{IN\text{-}UVP}$ is enabled immediately after $V_{DD}$ passes UVLO level.

### $t_{ON\text{-}MAX.}$ Protection ($t_{MP}$)

SiC45x has power up time limit control. When the device does not power up the output voltage above the $V_{UFL}$ in a time interval longer than $t_{ON\_MAX\_FAULT\_LIMIT}$ ($t_{MFL}$), the $t_{ON\text{-}MAX.}$ ($t_M$) fault condition is recognized and both the HS and LS MOSFETs are turned off. The device continues restart attempt after the shutdown in a delay time until the $t_M$ fault no longer exists.

The $t_{MFL}$ and delay time can be programmed via PMBus (see PMBus command section). The default value of $t_{MFL}$ is 20 ms. The default delay time is 20 ms.

The $t_{MP}$ is enabled immediately after $V_{DD}$ passes UVLO level.

### Overtemperature Protection (OTP)

SiC45x has internal thermal monitor block to support device temperature control. When the device temperature rises above OT_FAULT_LIMIT (OFL), the overtemperature (OT) fault condition is recognized and both the HS and LS MOSFETs are turned off. When OT fault condition no longer exists, the device restarts.

The OFL can be programmed via PMBus (see PMBus command section). The default value of OFL is 125 °C.

The OTP is enabled immediately after $V_{DD}$ passes UVLO level.

### Pre-Bias Start-Up

$V_{OUT}$ is monitored through differential output voltage sense pins $V_{sen+}$ and $V_{sen-}$. If the sensed voltage is higher than $V_{SET}$, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

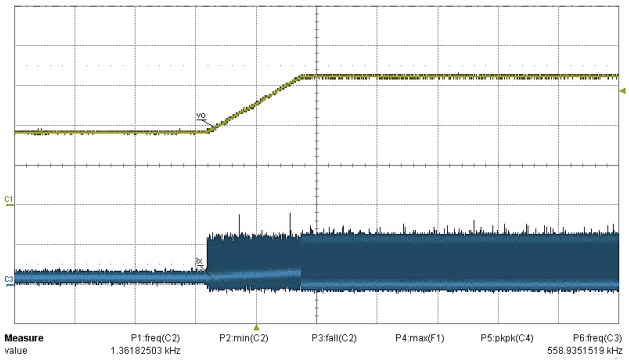



**Fig. 8 - Pre-Bias Start-Up**

### Output Voltage Setting

Connecting a resistor from $V_{SET}$ to $A_{GND}$ will set output voltage ($V_{OUT}$), eight $V_{OUT}$ related warning and fault voltage limits, and the value of VOUT_SCALE_LOOP as listed in the "VOUT_SCALE_LOOP look up" table. See below table for the list of supported output voltage ($V_{OUT}$) set by the $V_{SET}$ resistor value. After $V_{OUT}$ is set by the resistor, the voltage level of eight $V_{OUT}$ related warning and fault limits defined by PMBus and the VOUT_SCALE_LOOP register are automatically set also. See below table for the list of the eight $V_{OUT}$ related warning and fault limits set by $V_{OUT}$ setting resistor. Please do not leave the setting resistor open or short, or contact Vishay for technical support. The resistor setting $V_{OUT}$ or anyone of the eight $V_{OUT}$ related warning and fault limits can be separately overridden by a PMBus command with resolution 1.953 mV (see PMBus command table).

| OUTPUT VOLTAGE SETTINGS | |
|---|---|
| $V_{SET}$ RESISTOR (kΩ) | $V_{OUT}$ (V) |
| 0.845 | 0.60 |
| 1.30 | 0.90 |
| 1.78 | 0.95 |
| 2.32 | 1.00 |
| 2.87 | 1.05 |
| 3.48 | 1.20 |
| 4.12 | 1.25 |
| 4.75 | 1.50 |
| 5.49 | 1.80 |
| 6.19 | 2.10 |
| 6.98 | 2.50 |
| 7.87 | 3.30 |
| 8.87 | 5.00 |
| 11.0 | 12.00 |

| $V_{OUT}$ RELATED WARNINGS AND FAULTS | VOLTAGE LEVEL |
|---|---|
| POWER_GOOD_ON | 90 % $V_{OUT}$ |
| POWER_GOOD_OFF | 85 % $V_{OUT}$ |
| VOUT_OV_FAULT_LIMIT | 115 % $V_{OUT}$ |
| VOUT_OV_WARN_LIMIT | 110 % $V_{OUT}$ |
| VOUT_UV_WARN_LIMIT | 90 % $V_{OUT}$ |
| VOUT_UV_FAULT_LIMIT | 80 % $V_{OUT}$ |
| VOUT_MARGIN_LOW | 95 % $V_{OUT}$ |
| VOUT_MARGIN_HIGH | 105 % $V_{OUT}$ |

### RT/SYNC PIN and Mode of Switching Configuration

The SiC45x has an RT / SYNC pin. This pin can be used to set the switching frequency and to send or receive a clock signal for synchronization between a master and slave. SiC45x will inject less than 1 mA DC current across the RT/SYNC pin to the ground during initial power up process, and connecting a resistor from the RT/SYNC pin to ground will be used to set the switching frequency according to the table listed below. The following table shows the supported frequency settings by the RT resistor value. Please do not leave the setting resistor open or short, or contact Vishay for technical support. The frequency set by the external resistor can be overridden by a PMBus command with resolution 50 kHz (see PMBus command table).

| FREQUENCY SETTINGS | |
|---|---|
| RT RESISTOR (kΩ) | FREQUENCY (kHz) |
| 0.845 | 300 |
| 1.30 | 400 |
| 1.78 | 500 |
| 2.32 | 550 |
| 2.87 | 600 |
| 3.48 | 650 |
| 4.12 | 700 |
| 4.75 | 750 |
| 5.49 | 800 |
| 6.19 | 850 |
| 6.98 | 900 |
| 7.87 | 950 |
| 8.87 | 1000 |
| 10 | 1250 |
| 11 | 1500 |

SiC45x supports four modes of switching configuration, including standalone mode, master mode, slave mode in phase, and slave mode 180° out of phase. The master mode is default one of switching configuration and user can override it to be either standalone mode, slave mode in phase, or slave mode 180° out of phase by PMBus command INTERLEAVE (see PMBus command table).

The following table introduces four modes of switching configuration, recommended RT/SYNC pin connections, and content of related PMBus command INTERLEAVE.

| MODE OF SWITCHING CONFIGURATION, PIN CONNECTION, AND INTERLEAVE PMBus | | | | |
|---|---|---|---|---|
| **MODE TYPE** | **MODE DESCRIPTION** | **SWITCHING FREQUENCY AND RECOMMENDED RT/SYNC PIN CONNECTION** | **SWITCHING PHASE** | **INTERLEAVE COMMAND** |
| Standalone | Chip works individually | Cross a resistor $R_{RT}$ from RT / SYNC pin to ground. During power up, less than 1 mA DC current will be injected into resistor $R_{RT}$ to determine default switching frequency. The default switching frequency can be overridden by PMBus command. After power up, RT / SYNC pin is released and connected to ground via $R_{RT}$. | Self determined | 0x0000 |
| Master | Chip works as a master chip outputting a clock signal in phase with its switching to drive an external slave chip's switching frequency and phase | Cross a resistor $R_{RT}$ from RT / SYNC pin to ground. During power up, less than 1 mA DC current will be injected into resistor $R_{RT}$ to determine default switching frequency. The default switching frequency can be overridden by PMBus command. After power up, RT / SYNC pin outputs a 50 % duty cycle pulse signal toggling between 0 and $V_{DD}$, which is in phase with the chip's switching node. | Self determined | 0x0100 |
| Slave in phase | Chip works as a slave chip receiving an external clock signal and synchronize its switching in phase with the clock signal | Cross a resistor $R_{RT}$ from RT / SYNC pin to ground. During power up, less than 1 mA DC current will be injected into resistor $R_{RT}$ to determine default switching frequency. The default switching frequency can be overridden by PMBus command. When there is an external clock signal presented at the RT / SYNC pin, the switching frequency will be overridden and the chip's switching node is in phase with the external clock signal. If the external clock signal comes from a SiC45x working in master mode switching configuration, the resistor $R_{RT}$ shall be same to the $R_{RT}$ used by the master chip. | In phase with the external clock, or self determined when individually works | 0x0120 |
| Slave 180 ° out of phase | Chip works as a slave chip receiving an external clock signal and synchronize its switching 180 ° out of phase with the clock signal | Cross a resistor $R_{RT}$ from RT / SYNC pin to ground. During power up, less than 1 mA DC current will be injected into resistor $R_{RT}$ to determine default switching frequency. The default switching frequency can be overridden by PMBus command. When there is an external clock signal presented at the RT / SYNC pin, the switching frequency will be overridden and the chip's switching node is 180° out of phase with the external clock signal. If the external clock signal comes from a SiC45x working in master mode switching configuration, the resistor $R_{RT}$ shall be same to the $R_{RT}$ used by the master chip | 180° out of phase with the external clock, or self determined when individually works | 0x0121 |

### PMBus ADDRESS (ADDR pin)

The SiC45x has a 7-bit register that are used to set the base PMBus address of the device. A resistor assembled between ADDR pin and ground sets an offset from the default pre-configured MFR base address in the memory. Up to 15 different offsets can be set allowing 15 SiC45x devices with unique addresses in a single system. This offset and therefore the device address is read by the ADC during the initialization sequence. The table below provides the resistor values needed to set the 15 offsets from the base address. Please do not leave the setting resistor open or short.

| MFR_BASE_ADDRESS | | | | |
|---|---|---|---|---|
| **CONNECTION** | **ADDRESS** | **HEX [3 : 0]** | **NVM [6 : 4]** | **BIN [6 : 0]** |
| 0.845K | 1 | 0 | 001b | 0010 000b |
| 1.3K | 2 | 1 | 001b | 0010 001b |
| 1.78K | 3 | 2 | 001b | 0010 010b |
| 2.32K | 4 | 3 | 001b | 0010 011b |
| 2.87K | 5 | 4 | 001b | 0010 100b |
| 3.48K | 6 | 5 | 001b | 0010 101b |
| 4.12K | 7 | 6 | 001b | 0010 110b |
| 4.75K | 8 | 7 | 001b | 0010 111b |
| 5.49K | 9 | 8 | 001b | 0011 000b |
| 6.19K | 10 | 9 | 001b | 0011 001b |
| 6.98K | 11 | A | 001b | 0011 010b |
| 7.87K | 12 | B | 001b | 0011 011b |
| 8.87K | 13 | C | 001b | 0011 100b |
| 10K | 14 | D | 001b | 0011 101b |
| 11K | 15 | E | 001b | 0011 110b |

Vishay provides another 15 options of PMBus address listed in table of MFR_BASE_ADDRESS_2. Please contact Vishay for technical support.

**MFR_BASE_ADDRESS_2**

| CONNECTION | ADDRESS | HEX [3 : 0] | NVM [6 : 4] | BIN [6 : 0] |
|---|---|---|---|---|
| 0.845K | 1 | 0 | 101b | 1010 000b |
| 1.3K | 2 | 1 | 101b | 1010 001b |
| 1.78K | 3 | 2 | 101b | 1010 010b |
| 2.32K | 4 | 3 | 101b | 1010 011b |
| 2.87K | 5 | 4 | 101b | 1010 100b |
| 3.48K | 6 | 5 | 101b | 1010 101b |
| 4.12K | 7 | 6 | 101b | 1010 110b |
| 4.75K | 8 | 7 | 101b | 1010 111b |
| 5.49K | 9 | 8 | 101b | 1011 000b |
| 6.19K | 10 | 9 | 101b | 1011 001b |
| 6.98K | 11 | A | 101b | 1011 010b |
| 7.87K | 12 | B | 101b | 1011 011b |
| 8.87K | 13 | C | 101b | 1011 100b |
| 10K | 14 | D | 101b | 1011 101b |
| 11K | 15 | E | 101b | 1011 110b |

**PMBus COMMAND LIST**

| ADDRESS | PMBus COMMAND NAME | TYPE | DATA FORMAT (UNITS) | DEFAULT VALUE IN NVM | DEFAULT | VALID RANGE |
|---|---|---|---|---|---|---|
| 01h | OPERATION | R/W | Byte | 88h (1000,1000) | [7] 1: PMBus unit output is on<br>[6] 0: output is turned off immediately and any power down sequencing commads are ignored<br>[5 : 4] 00: $V_{OUT}$ set by VOUT_COMMAND<br>[3 : 2] 10: faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the nominal output voltage source are acted upon according to the settings of the VOUT_OV_FAULT_RESPONSE and VOUT_IV_FAULT_RESPONSE data bytes<br>[1] 0: not used<br>[0]: reserved 02h | - |
| 02h | ON_OFF_CONFIGURATION | R/W | Byte | 1Fh (0001,1111) | [7 : 5] 000: reserved<br>[4] 1: no power up until commanded by the CONTROL and OPERATION<br>[3] 1: to start, the unit requires on/off portion of the OPERATION command<br>[2] 1: to start, the unit requires CONTROL asserted<br>[1] 1: active high to start the unit<br>[0] 1: turn off $V_{OUT}$ as fast as possible, ignore TOFF_DELAY and TOFF_FALL | - |
| 03h | CLEAR_FAULTS | Write | - | - | - | - |
| 10h | WRITE_PROTECT | Write | Byte | 00h (0000,0000) | [7 : 0]: 0000,0000: allows write to all registers | - |
| 15h | STORE_USER_ALL | Write | - | - | - | - |
| 16h | RESTORE_USER_ALL | Write | - | - | - | - |

| PMBus COMMAND LIST | | | | | | |
|---|---|---|---|---|---|---|
| ADDRESS | PMBus COMMAND NAME | TYPE | DATA FORMAT (UNITS) | DEFAULT VALUE IN NVM | DEFAULT | VALID RANGE |
| 19h | CAPABILITY | Read | Byte | D0h (1101,0000) | [7] 1: packet error checking is supported<br>[6 : 5] 10: maximum supported bus speed is 1 MHz<br>[4] 1: the unit has SMBALERT# pin and supports SMBus alert response protocol<br>[3] 0: numeric data is in LINEAR11, LINEAR16, or DIRECT format<br>[2] 0: AVSBUS not supported<br>[1 : 0] 00: reserved | - |
| 1Bh | SMBALERT_MASK | R/W | Block | 0x0000 (0000,0000, 0000,0000) | - | - |
| 20h | VOUT_MODE | Read | LINEAR16 (V) | 17h (0001,0111) | [7 : 5] 000: the unit uses LINEAR16 format for $V_{OUT}$ related commands<br>[4 : 0] 1,0111: five bit two is complement exponent equals -9 for $V_{OUT}$ related commands | - |
| 21h | VOUT_COMMAND | R/W | LINEAR16 (V) | 0133h (0000,0001, 0011,0011) | 0.6 V | 0.3 V to 14 V, 1.953 mV resolution |
| 22h | VOUT_TRIM | R/W | LINEAR16 (V) | xxxxh (xxxx,xxxx, xxxx,xxxx) | This command deviates from standard PMBus 1.3 specifications; a factory trim value varying by devices | -2 V to 2 V, 1.953 mV resolution |
| 24h | VOUT_MAX | R/W | LINEAR16 (V) | 1C00h (0001,1100, 0000,0000) | 14 V | 0.3 V to 14 V, 1.953 mV resolution |
| 25h | VOUT_MARGIN_HIGH | R/W | LINEAR16 (V) | 0142h (0000,0001, 0100,0010) | 0.63 V | 0.3 V to 14 V, 1.953 mV resolution |
| 26h | VOUT_MARGIN_LOW | R/W | LINEAR16 (V) | 0123h (0000,0001, 0010,0011) | 0.57 V | 0.3 V to 14 V, 1.953 mV resolution |
| 27h | VOUT_TRANSITION_RATE | R/W | LINEAR11 (mV/µs) | E002h (1110,0000, 0000,0010) | 0.125 mV/µs | 0.0625 mV/µs to2 mV/µs, 0.0625 mV/µs resolution |
| 29h | VOUT_SCALE_LOOP | R/W | LINEAR11 (V/V) | E808h (1110,1000, 0000,1000) | This command deviates from standard PMBus 1.3 specifications; 1 V/V | 0.125 V/V, 0.25 V/V, 0.5 V/V, 1 V/V |
| 33h | FREQUENCY_SWITCH | R/W | LINEAR11 (kHz) | 0258h (0000,0010, 0101,1000) | 600 kHz | 300 kHz to 1500 kHz, 50 kHz resolution |
| 35h | VIN_ON | R/W | LINEAR11 (V) | F814h (1111,1000, 0001,0100) | 10 V | 1 V to 80 V, 0.5 V resolution |
| 36h | VIN_OFF | R/W | LINEAR11 (V) | 0100h (0000,0001, 0000,0000) | 9 V | 1 V to 80 V, 0.5 V resolution |

| PMBus COMMAND LIST | | | | | | |
|---|---|---|---|---|---|---|
| ADDRESS | PMBus COMMAND NAME | TYPE | DATA FORMAT (UNITS) | DEFAULT VALUE IN NVM | DEFAULT | VALID RANGE |
| 37h | INTERLEAVE | R/W | Word | 0100h (0000,0001, 0000,0000) | [15 : 12] 0000: reserved<br>[11 : 8] 0001: sets unit as Master or Slave<br>[7 : 4] 0000: sets unit as master<br>[3 : 0] 0000: not used | Standalone, master, slave in phase, slave 180° out of phase |
| 40h | VOUT_OV_FAULT_LIMIT | R/W | LINEAR1 6 (V) | 0161h (0000,0001, 0011,0011) | 0.69 V | 0.3 V to 14 V, 1.953 mV resolution |
| 41h | VOUT_OV_FAULT_RESPONSE | R/W | Byte | F8h (1111,1000) | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It attempts to restart continuously, without limitation, until it is commanded off (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down | 00h, 16h, 22h, 36h, C0h, D6h, E2h, F6h, F8h |
| 42h | VOUT_OV_WARN_LIMIT | R/W | LINEAR1 6 (V) | 0151h (0000,0001, 0101,0001) | 0.66 V | 0.3 V to 14 V, 1.953 mV resolution |
| 43h | VOUT_UV_WARN_LIMIT | R/W | LINEAR1 6 (V) | 0114h (0000,0001, 0001,0100) | 0.54 V | 0 V to 14 V, 1.953 mV resolution |
| 44h | VOUT_UV_FAULT_LIMIT | R/W | LINEAR1 6 (V) | 00F5h (0000,0000, 1111,0101) | 0.48 V | 0 V to 14 V, 1.953 mV resolution |
| 45h | VOUT_UV_FAULT_RESPONSE | R/W | Byte | B9h (1011,1001) | The device shuts down (disables the output) and attempts to restart continuously, without limitation, until it is commanded off (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. 20 ms delay | 00h, 16h, 22h, 36h, B9h, C0h, D6h, E2h, F6h |
| 46h | IOUT_OC_FAULT_LIMIT | R/W | LINEAR1 1 (A) | SiC450:F870h (1111,1000, 0111,0000)<br>SiC451: F846h (1111,1000, 0100,0110)<br>SiC453: F82Ah (1111,1000, 0010,1010) | SiC450: 56 A<br>SiC451: 35 A<br>SiC453: 21 A | 0 A to 127 A, 0.5 A resolution |
| 47h | IOUT_OC_FAULT_RESPONSE | R/W | Byte | A1h (1010,0001) | This command deviates from standard PMBus 1.3 specifications. The device continues operation for 128 consecutive OC cycles and then shut down. Waiting for 20 ms, it hiccups until the fault condition no longer exists | 00h, 16h, 22h, 36h, A1h, C0h, D6h, E2h, F6h, F8h |

| PMBus COMMAND LIST | | | | | | |
|---|---|---|---|---|---|---|
| ADDRESS | PMBus COMMAND NAME | TYPE | DATA FORMAT (UNITS) | DEFAULT VALUE IN NVM | DEFAULT | VALID RANGE |
| 4Ah | IOUT_OC_WARN_LIMIT | R/W | LINEAR1 1 (A) | SiC450: F868h (1111,1000, 0110,1000) SiC451: F841h (1111,1000, 0100,0010) SiC453: F827h (1111,1000, 0010,0111) | SiC450: 52 A SiC451: 32.5 A SiC453: 19.5 A | 0 A to 127 A, 0.5 A resolution |
| 4Fh | OT_FAULT_LIMIT | R/W | LINEAR1 1 (°) | 007Dh (0000,0000, 0111,1101) | 125 °C | 0 °C to 150 °C, 1 °C resolution |
| 50h | OT_FAULT_RESPONSE | R/W | Byte | F9h (1111,1001) | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It attempts to restart continuously, without limitation, until it is commanded off (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down | 00h, 16h, 22h, 36h, C0h, D6h, E2h, F6h, F9h |
| 51h | OT_WARN_LIMIT | R/W | LINEAR1 1 (°) | 0069h (0000,0000, 0110,1001) | 105 °C | 0 °C to 150 °C, 1 °C resolution |
| 55h | VIN_OV_FAULT_LIMIT | R/W | LINEAR1 1 (V) | F81Eh (1111,1000, 0001,1110) | 15 V | 1 V to 80 V, 0.5 V resolution |
| 56h | VIN_OV_FAULT_RESPONSE | R/W | Byte | B8h (1011,1000) | This command deviates from standard PMBus 1.3 specifications.The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It does not attempt to restart. The output remains disabled until the fault is cleared | 00h, 16h, 22h, 36h, B8h, C0h, D6h, E2h, F6h |
| 58h | VIN_UV_WARN_LIMIT | R/W | LINEAR1 1 (V) | F812h (1111,1000, 0001,0010) | 9 V | 1 V to 80 V, 0.5 V resolution |
| 5Dh | IIN_OC_WARN_LIMIT | R/W | LINEAR1 1 (A) | F80Ah (1111,1000, 0000,1010) | 5 A | 0 A to 127 A, 0.5 A resolution |
| 5Eh | POWER_GOOD_ON | R/W | LINEAR1 6 (V) | 0114h (0000,0001, 0001,0100) | 0.54 V | 0.24 V to 14 V, 1.953 mV resolution |
| 5Fh | POWER_GOOD_OFF | R/W | LINEAR1 6 (V) | 0105h (0000,0001, 0000,0101) | 0.51 V | 0.24 V to 14 V, 1.953 mV resolution |
| 60h | TON_DELAY | R/W | LINEAR1 1 (ms) | 0000h (0000,0000, 0000,0000) | 0 ms | 0 ms to 127 ms, 1 ms resolution |
| 61h | TON_RISE | R/W | LINEAR1 1 (ms) | 0005h (0000,0000, 0000,0101) | 5 ms | 0 ms to 127 ms, 1 ms resolution |

| PMBus COMMAND LIST | | | | | | |
|---|---|---|---|---|---|---|
| ADDRESS | PMBus COMMAND NAME | TYPE | DATA FORMAT (UNITS) | DEFAULT VALUE IN NVM | DEFAULT | VALID RANGE |
| 62h | TON_MAX_FAULT_LIMIT | R/W | LINEAR1 1 (mS) | 0014h (0000,0000, 0001,0100) | 20 ms | 0 ms to 127 ms, 1 ms resolution |
| 63h | TON_MAX_FAULT_RESPONSE | R/W | Byte | B9h (1011,1001) | The device shuts down (disables the output). It attempts to restart continuously, without limitation, until it is commanded off (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. 20 ms delay | 80h, 83h, 86h, 88h, 89h, 8Ah, 8Bh, B9h |
| 64h | TOFF_DELAY | R/W | LINEAR1 1 (ms) | 0000h (0000,0000, 0000,0000) | 0 ms | 0 ms to 127 ms, 1 ms resolution |
| 65h | TOFF_FALL | R/W | LINEAR1 1 (ms) | 0005h (0000,0000, 0000,0101) | 5 ms | 0 ms to 127 ms, 1 ms resolution |
| 66h | TOFF_MAX_WARN_LIMIT | R/W | LINEAR1 1 (ms) | 003Ch (0000,0000, 0011,1100) | 60 ms | 0 ms to 127 ms, 1 ms resolution |
| 78h | STATUS_BYTE | Read | Byte | 00h (0000,0000) | No faults | - |
| 79h | STATUS_WORD | Read | Word | 0000h (0000,0000, 0000,0000) | No faults | - |
| 7Ah | STATUS_VOUT | Read | Byte | 00h (0000,0000) | No faults | - |
| 7Bh | STATUS_IOUT | Read | Byte | 00h (0000,0000) | No faults | - |
| 7Ch | STATUS_INPUT | Read | Byte | 00h (0000,0000) | No faults | - |
| 7Dh | STATUS_TEMPERATURE | Read | Byte | 00h (0000,0000) | No faults | - |
| 7Eh | STATUS_CML | Read | Byte | 00h (0000,0000) | No faults | - |
| 80h | STATUS_MFR_SPECIFIC | Read | Byte | 00h (0000,0000) | No faults | - |
| 88h | READ_VIN | Read | LINEAR1 1 (V) | n/a | n/a | 0 V to 80 V |
| 89h | READ_IIN | Read | LINEAR1 1 (A) | n/a | n/a | exp: (-4) to (-16) |
| 8Bh | READ_VOUT | Read | LINEAR1 6 (V) | n/a | n/a | 0 V to 48 V |
| 8Ch | READ_IOUT | Read | LINEAR1 1 (A) | n/a | n/a | exp: (-4 ) to (-10) |
| 8Dh | READ_TEMPERATURE | Read | LINEAR1 1 (°) | n/a | n/a | (-50)° to 150° |
| 94h | READ_DUTY_CYCLE | Read | LINEAR1 1 (%) | n/a | n/a | 0 % to 100 % |
| 96h | READ_POUT | Read | LINEAR1 1 (W) | n/a | n/a | exp: (-4) to (-16) |
| 97h | READ_PIN | Read | LINEAR1 1 (W) | n/a | n/a | exp: (-4) to (-16) |
| 98h | PMBUS_REVISION | Read | Byte | 33h (0011,0011) | [7 :4] 0011: part I revision 1.3<br>[3 : 0] 0011: part II revision 1.3 | |

| PMBus COMMAND LIST | | | | | | |
|---|---|---|---|---|---|---|
| ADDRESS | PMBus COMMAND NAME | TYPE | DATA FORMAT (UNITS) | DEFAULT VALUE IN NVM | DEFAULT | VALID RANGE |
| 9Eh | MFR_SERIAL | R/W | Block | n/a | For user to store customized information | |
| ADh | IC_DEVICE_ID | R/W | Block | 0000h | - | |
| D7h | MFR_BASE_ADDRESS | Pins program | 7-bit | 10h | - | |
| E2h | MFR_BASE_ADDRESS_2 | Pins program | 7-bit | 50h | - | |

## PMBus COMMAND DETAILS

### OPERATION (01h)

The OPERATION command sets the operational state of the regulator. It is used for the following functions:

- Turn the regulator output on and off in conjunction with the input from EN signal
- Set the output voltage with upper or lower margins
- Select the fault handling behavior when fault is caused by margining state

| COMMAND | OPERATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | On/off | Off B | Margin | | MRGNFLT | | Nouse | RSV |
| Default (88h) | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Bit Description (default setting in bold)**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 7 | On/off | 0b | Output is disabled |
| | | **1b** | **Output is enabled** |
| 6 | Off B | **0b** | **Output is turned off immediately and power off sequence commands ignored** |
| | | 1b | Regulator turns off following the TOFF_DELAY and TOFF_FALL command |
| 5 : 4 | Margin | **00b** | **Output voltage is set by the PMBus VOUT_COMMAND data** |
| | | 01b | Output voltage is set by the PMBus VOUT_MARGIN_LOW data |
| | | 10b | Output voltage is set by the PMBus VOUT_MARGIN_HIGH data |
| | | 11b | Not supported |
| 3 : 2 | MRGNFLT | 00b | Not supported |
| | | 01b | Faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the nominal output voltage source are ignored |
| | | **10b** | **Faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the nominal output voltage source are acted upon according to the settings of the VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE** |
| | | 11b | Not supported |
| 1 | Nouse | x | Not used |
| 0 | RSV | x | Reserved |

### ON_OFF_CONFIGURATION (02h)

The ON_OFF_CONFIG command configures the combination of EN pin input and PMBus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

| COMMAND | ON/OFF_CONFIGURATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | RSV | | | PU | CMD | EN | ENPOL | Off B1 |
| Default (1Fh) | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**Bit Description (default setting in bold)**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 7 : 5 | RSV | 000b | Reserved |
| 4 | PU | 0b | Regulator powers up any time power is present regardless of state of the EN pin |
| | | **1b** | **Regulator does not power up until commanded by the CONTROLEN pin and OPERATION command** |
| 3 | CMD | 0b | Regulator ignores the “on” bit in the OPERATION command |
| | | **1b** | **Regulator responds the “on” bit in the OPERATION command** |
| 2 | EN | 0b | Regulator ignores the EN pin. Power conversion is controlled only by the OPERATION command |
| | | **1b** | **Regulator requires the EN pin to be asserted to start the unit** |
| 1 | ENPOL | 0b | EN signal is active low |
| | | **1b** | **EN signal is active high** |
| 0 | OFFB1 | 0b | Regulator turns off following the $t_{OFF\_DELAY}$ and $t_{OFF\_FALL}$ command when EN signal is used to turn off |
| | | **1b** | **Regulator turns off immediately** |

### CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SALRT ALERT# signal output if the device is asserting the SALRT ALERT# signal.

### WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device’s configuration or operation.

| COMMAND | WRITE_PROTECT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | WTPRT | | | Nouse | | | | |
| Default (00h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit Description (default setting in bold)**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 7 : 5 | WTPRT | **000b** | **Enable writes to all commands** |
| | | 100b | Disable all writes except to the WRITE_PROTECT command |
| | | 010b | Disable all writes except to the WRITE_PROTECT and OPERATION commands |
| | | 001b | Disable all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and $V_{OUT\_COMMAND}$ commands |
| 4 : 0 | Nouse | 00000b | Not used |

### STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory to the matching locations in the non-volatile User Store memory. Any items in operating memory that do not have matching locations in the User Store are ignored.

### RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the nonvolatile user store memory (NVM) to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. This feature is protected by the EEPROM_PASSWORD (DBh) command, see the section below for more information. Any items in user store that do not have matching locations in the operating memory are ignored, see the summary table for details.

### CAPABILITY (19h)

The CAPABILITY command provides a way for a host system to determine some key capabilities of the PMBus device.

This is a read only register.

| COMMAND | WRITE_PROTECT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | PEC | SPD | | ALRT | NFMT | AVS | RSV | |
| Default (D0h) | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

### Bit Description

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 7 | PEC | 1b | Packet error checking is supported |
| 6 : 5 | SPD | 10b | Maximum supported bus speed is 1 MHz |
| 4 | ALRT | 1b | The unit has ALERT# pin and supports PMBus alert response protocol |
| 3 | NFMT | 0b | Numeric data is in LINEAR11, LINEAR16, or DIRECT format |
| 2 | AVS | 0b | AVSBUS not supported |
| 1 : 0 | RSV | 00b | Reserved |

### SMBALERT_MASK (1Bh)

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SMBALERT# signal. The command format used to block a status bit or bits from causing the SMBALERT# signal to be asserted is shown in Fig. 9. The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an over temperature warning OT_WARNING (overtemperature warning) condition would be blocked from asserting SMBALERT#.

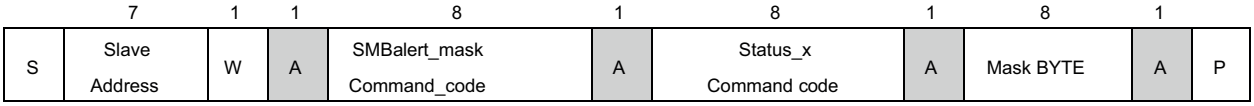
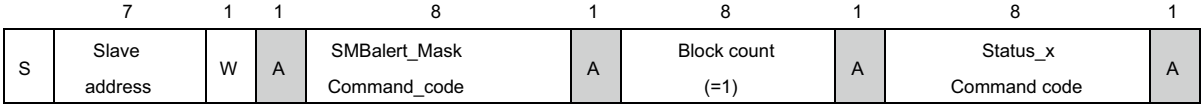



**Fig. 9 - SMBALSER_MASK Command Packet Format**

The command format used by the host to determine the SMALER_MASK setting for a given status register is shown in Fig. 10.



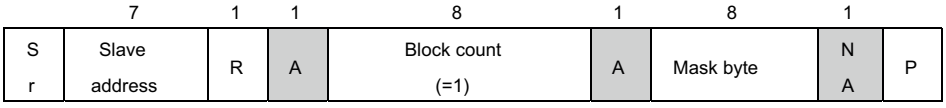




**Fig. 10 - Retrieving the SMBALSER_MASK Setting for a Given Status Register**

### VOUT_MODE (20h)

The PMBus specification dictates that the data word for the $V_{OUT\_MODE}$ command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the linear or direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are fixed and do not permit the user to change the values.

This is a read only register

| COMMAND | WRITE_PROTECT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | Mode | | | EXP | | | | |
| Default (D0h) | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 7 : 5 | Mode | 000b | The unit uses ULINEAR16 format for $V_{OUT}$ related commands |
| 4 : 0 | EXP | 10111b | 5-bit two's complement binary integer equals -9 for $V_{OUT}$ related commands |

### VOUT_COMMAND (21h)

The VOUT_COMMAND is used to directly set the output voltage using the ULINEAR16 format, which is a 16-bit unsigned integer. This is a read and write register. The output voltage, in volts, is calculated from the equation:

$$V_{OUT\_SET} = V_{OUT\_COMMAND} \times 2^{N}$$

Where:

$V_{OUT\_SET}$ is the set output voltage in volt

VOUT_COMMAND is the 16-bit unsigned binary integer specified in the command

N is a 5-bit two's complement binary integer specified in $V_{OUT}$ mode [4 : 0]

| COMMAND | $V_{OUT}$ COMMAND | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | Data byte high | | | | | | | | Data byte low | | | | | | | |
| Default (133h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

**Bit Description**

| BITS | FORMAT | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Unlinear 16 | 0133h | VOUT_COMMAND is specified as 307 x $2^{-9}$ = 0.6 V |

The output voltage's range is 0.3 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0133h equivalent to 0.6 V.

### VOUT_TRIM (22h)

The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value. This is a read and write register. The VOUT_TRIM has two data bytes formatted as a two's complement binary integer (SLINEAR16 format). It is most typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user's system.

The VOUT_TRIM command deviates from standard PMBus 1.3 specifications, at which it requires adding an integer calculating from the expected offset voltage and the VOUT_SCALE_LOOP to VOUT_TRIM's NVM register default store value varying by devices. The effect of this command on the output voltage, in volts, is calculated from the equation:

$$\Delta Voltage = \frac{\Delta V \times 2^{N}}{VOUT\_SCALE\_LOOP}$$

Where:

$\Delta$voltage is the fixed offset voltage to the output voltage in volt

$\Delta V$ is the 16-bit two's complement integer specified in VOUT_TRIM

VOUT_SCALE_LOOP is the dimensionless scale factor specified in VOUT_SCALE_LOOP command

N is a 5-bit two's complement binary integer specified in VOUT_MODE [4:0].

| COMMAND | $V_{OUT}$ TRIM | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | sign | data | | | | | | | | | | | | | | |
| Default (0000h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit Description**

| BITS | FORMAT | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Unlinear 16 | 0000h | ΔV is 0 V |

The offset voltage's range is -2 V to 2 V, resolution is 1.953 mV, and its NVM register default store value is a factory trim value varying by devices. The users need to calculate a 16-bit two's complement integer number following the above equation and add the number to the factory trim value, so as to achieve the expected offset voltage to the output voltage.

### VOUT_MAX (24h)

The VOUT_MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overvoltage protection. This is a read and write register.

The VOUT_MAX uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MAX command.

**Bit Description**

| BITS | FORMAT | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Unlinear 16 | 1C00h | The VOUT_MAX is specified as 14 V |

The VOUT_MAX range is 0.3 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 1C00h equivalent to 14 V.

### VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "margin high". This is a read and write register.

The VOUT_MARGIN_HIGH uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | FORMAT | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Unlinear 16 | 0142h | The VOUT_MARGIN_HIGH is specified as 0.63 V |

The VOUT_MARGIN_HIGH range is 0.3 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0142h equivalent to 0.63 V.

### VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to margin low. This is a read and write register.
The VOUT_MARGIN_LOW uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | FORMAT | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Unlinear 16 | 0123h | The VOUT_MARGIN_LOW is specified as 0.57 V |

The VOUT_MARGIN_LOW range is 0.3 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0123h equivalent to 0.57 V.

### VOUT_TRANSITION_RATE (27h)

The VOUT_TRANSITION_RATE command sets the rate in mV/µs at which the output voltage should change voltage when a PMBus device receives either a VOUT_COMMAND or OPERATION (margin high, margin low) that causes the output voltage to change. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off. This is a read and write register.
The VOUT_TRANSITION_RATE uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the VOUT_TRANSITION_RATE command is constant as 5'b11100, that is, -4 in decimal. The LINEAR11 format of the two data bytes is illustrated in table below.

**Table - LINEAR11 Numeric Format Data Bytes**

| COMMAND | VOUT_TRANSITION_RATE | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | EXP | | | | | MAN | | | | | | | | | | |
| Default (E002h) | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 | EXP SGN | 1b | Exponent value with negative sign |
| 14 : 11 | EXP | 1100b | Five 5-bit two's complement exponent equals -4 for VOUT_TRANSITION_RATE command |
| 10 | MAN SGN | 0b | Mantissa value with positive sign |
| 9 : 0 | MAN DATA | 00, 0000, 0010b | Eleven 11-bit two's complement mantissa equals 2 for VOUT_TRANSITION_RATE command |

The VOUT_TRANSITION_RATE range is 0.0625 - 2 mV/µs, resolution is 0.0625 mV/µs, and its NVM register default store value is E002h equivalent to 0.125 mV/µs. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command deviates from standard PMBus 1.3 specifications. The VOUT_SCALE_LOOP command is used to scale down both the VOUT_COMMAND and the sense differential output voltage at the unit input, so as to extend operational range of the PMBus unit to reach the maximum output voltage 12 V without the requirement of external resistor divider on board. This is a read and write register.
The VOUT_SCALE_LOOP uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the VOUT_SCALE_LOOP command is constant as 5'b11101, that is, -3 in decimal.

The LINEAR11 format of the two data bytes is illustrated in Table "LINEAR11 Numeric Format Data Bytes".

**Table - VOUT_SCALE_LOOP Look Up**

| SET OUTPUT VOLTAGE (V) | SCALE DOWN FACTOR (V/V) | VOUT_SCALE_LOOP BITS [15 : 0] |
|---|---|---|
| $0.3\ V < V_{OUT} < 1.8\ V$ | 1.0 | E808h |
| $1.8\ V \le V_{OUT} < 3.3\ V$ | 0.5 | E804h |
| $3.3\ V \le V_{OUT} \le 5.0\ V$ | 0.25 | E802h |
| $5.0\ V < V_{OUT} \le 12.0\ V$ | 0.125 | E801h |

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 to 0 | Linear 11 | E808h | The VOUT_SCALE_LOOP is specified as 1 V/V |

The VOUT_SCALE_LOOP offers four options of scale down factor: 1.0 V/V, 0.5 V/V, 0.25 V/V, and 0.125 V/V. When $V_{OUT}$ is set by a resistor between $V_{SET}$ pin and ground, the value of VOUT_SCALE_LOOP is automatically chosen according to the "VOUT_SCALE_LOOP look up" table. When $V_{OUT}$ is set by PMBus VOUT_COMMAND, the value of the VOUT_SCALE_LOOP shall be updated according to the "VOUT_SCALE_LOOP look up" table.

The VOUT_SCALE_LOOP NVM register default store value is E808h equivalent to 1.0 V/V. Any commands out of the valid options will be ignored and reported.

### FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of the PMBus unit. This is a read and write register. The FREQUENCY_SWITCH uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the FREQUENCY_SWITCH command is constant as 5'b00000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0258h | FREQUENCY_SWITCH is specified 600 kHz. |

The FREQUENCY_SWITCH range is 300 kHz to 1500 kHz, resolution is 50 kHz, and its NVM register default store value is 0258h equivalent to 600 kHz. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### VIN_ON (35h)

The VIN_ON command sets the value of the input voltage, in volt, at which the PMBus unit should start power conversion. This is a read and write register. The VIN_ON uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the VIN_ON command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | F814h | The VIN_ON is specified as 10 V |

The VIN_ON range is 1 V to 80 V, resolution is 0.5 V, and its NVM register default store value is F814h equivalent to 10 V. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage, in volt, at which the PMBus unit, once operation has started, should stop power conversion. This is a read and write register. The VIN_OFF uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the VIN_OFF command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | F812h | The VIN_OFF is specified as 9 V |

The VIN_OFF range is 1 V to 80 V, resolution is 0.5 V, and its NVM register default store value is F812h equivalent to 9 V. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### INTERLEAVE (37h)

The INTERLEAVE command deviates from standard PMBus 1.3 specifications. The INTERLEAVE command is used to sets the mode of switching frequency and phase, at which the PMBus unit, once operation has started, should use to generate switching frequency and phase angle. This is a read and write register.

The INTERLEAVE commands offer four modes of switching configuration: STANDALONE, MASTER, SLAVE in phase, and SALVE 180° out of phase.
The description of all four modes and the corresponding INTERLEAVE command is listed in the table below.

| INTERLEAVE COMMAND AND MODE OF SWITCHING FREQUENCY GENERATION | | |
|---|---|---|
| | DESCRIPTION | INTERLEAVE BITS [15 : 0] |
| STANDALONE | The value of unit switching frequency is set by resistance of a resistor connected to RT/SYNC unit designated pin. The setting value of the switching frequency will be overridden after the PMBus unit receiving the PMBus command FREQUENCY_SWITCH command. The RT/SYNC pin shall not be used for other purposes | 0000h |
| MASTER | The value of unit switching frequency is set by resistance of a resistor connected to RT/SYNC pin. The setting value of the switching frequency will be overridden after the PMBus unit receiving the PMBus command FREQUENCY_SWITCH command. After inside power $V_{DD}$ of the unit is above its under voltage level, the RT/SYNC pin will output a 50% duty cycle pulse signal in phase with the switching frequency, which may be used to drive other units set as the SLAVE mode by INTERLEAVE command. The RT/SYNC pin shall not be used for other purposes | 0100h |
| SLAVE in phase | The value of unit switching frequency is set by resistance of a resistor connected to RT/SYNC pin. The setting value of the switching frequency will be overridden after the PMBus unit receiving the PMBus command FREQUENCY_SWITCH command. When an external pulse switching signal is connected to the /SYNC pin, the unit will synchronize its switching frequency to the external pulse switching signal with 0° phase difference. The RT/SYNC pin shall not be used for other purpose | 0120h |
| SLAVE 180° out of phase | The value of unit switching frequency is set by resistance of a resistor connected to RT/SYNC pin. The setting value of the switching frequency will be overridden after the PMBus unit receiving the PMBus command FREQUENCY_SWITCH command. When an external pulse switching signal is connected to the /SYNC pin, the unit will synchronize its switching frequency to the external pulse switching signal with 180° phase difference. The RT/SYNC pin shall not be used for other purposes | 0121h |

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Linear 11 | 0100h | The INTERLEAVE is specified as MASTER mode |

The INTERLEAVE NVM register default store value is 0100h equivalent to MASTER mode. Any commands out of the options will be ignored and reported.

### VOUT_OV_FAULT_LIMIT (40h)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured at the sense of output pins that causes an output overvoltage fault. This is a read and write register.

The VOUT_OV_FAULT_LIMIT uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Ulinear 16 | 0161h | The VOUT_OV_FAULT_LIMIT is specified as 0.69 V |

The VOUT_OV_FAULT_LIMIT range is 0.3 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0161h equivalent to 0.69 V.

### VOUT_OV_FAULT_RESPONSE (41h)

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. This is a read and write register and the NVM register default store value is F8h.

| COMMAND | VOUT_OV_FAULT_RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | OVRSP | | OVRTY | | | OVDLY | | |
| Default (F8h) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**Supported Commands**

| OVRSP | | OVRTY | | | OVDLY | | | DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It attempts to restart continuously, without limitation, until it is commanded off (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The device continues operation |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |

### VOUT_OV_WARN_LIMIT (42h)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured at the sense of output pins that causes an output voltage high warning. This is a read and write register.

The VOUT_OV_WARN_LIMIT uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Ulinear 16 | 0151h | The VOUT_OV_WARN_LIMIT is specified as 0.66 V |

The VOUT_OV_WARN_LIMIT range is 0.3 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0151h equivalent to 0.66 V.

### VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage measured at the sense of output pins that causes an output voltage low warning. This is a read and write register.

The VOUT_UV_WARN_LIMIT uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Ulinear 16 | 0114h | The VOUT_UV_WARN_LIMIT is specified as 0.54 V |

The VOUT_UV_WARN_LIMIT range is 0 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0114h equivalent to 0.54 V.

### VOUT_UV_FAULT_LIMIT (44h)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage measured at the sense of output pins that causes an output undervoltage fault. This is a read and write register.

The VOUT_UV_FAULT_LIMIT uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Ulinear 16 | 00F5h | The VOUT_UV_FAULT_LIMIT is specified as 0.48 V |

The VOUT_UV_FAULT_LIMIT range is 0 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 00F5h equivalent to 0.48 V.

### VOUT_UV_FAULT_RESPONSE (45h)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. This is a read and write register and the NVM register default store value is B9h.

| COMMAND | VOUT_UV_FAULT_RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | UVRSP | | UVRTY | | | UVDLY | | |
| Default (B9h) | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

**Supported Commands**

| UVRSP | | UVRTY | | | UVDLY | | | DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | The device shuts down (disables the output) and attempts to restart continuously, without limitation, until it is commanded off (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. 20 ms delay |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The device continues operation |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. The device does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. The device does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. The device does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. The device does not attempt to restart. The output remains disabled until the fault is cleared |

**IOUT_OC_FAULT_LIMIT (46h)**

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in Amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. This is a read and write register. The IOUT_OC_FAULT_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the IOUT_OC_FAULT_LIMIT command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Linear 11 | F870h | The IOUT_OC_FAULT_LIMIT is 56 A for SiC450 |
| | | F846h | The IOUT_OC_FAULT_LIMIT is 35 A for SiC451 |
| | | F82Ah | The IOUT_OC_FAULT_LIMIT is 21 A for SiC453 |

The IOUT_OC_FAULT_LIMIT range is 0 A to 127 A, resolution is 0.5 A, and its NVM register default store value is F846h for SiC451 equivalent to 35 A. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

**IOUT_OC_FAULT_RESPONSE (47h)**

The IOUT_OC_FAULT_RESPONSE is used to set device over current protection response (OCP) when valley inductor current is higher than IOUT_OC_FAULT_LIMIT. This is a read and write register and the NVM register default store value is A1h.

| COMMAND | IOUT_OC_FAULT_RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | OCRSP | | OCCYCL | | | OCDLY | | |
| Default (0xA1h) | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

This command deviates from standard PMBus 1.3 specifications. It provides users 3-bit [5 : 3] setting to generate OC fault based on total number of consecutive pulse-by-pulse OC counts. It also provides users 3-bit [2 : 0] delay time option between shutdown and next restart attempt. In case of bits [5 : 3] = 111b, the device does not report OC fault and continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage.

**Supported Commands**

| OCRSP | | OCRTY | | | OCDLY | | | DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | The device continues operation for 128 consecutive OC cycles and then shut down. Waiting for 20 ms, it hiccups until the fault condition no longer exists |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The device continues operation |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | The device continues operation for 8 consecutive OC cycles and then shut down without delay |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | The device continues operation for 32 consecutive OC cycles and then shut down without delay |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | The device continues operation for 128 consecutive OC cycles and then shut down without delay. |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | The device continues operation for 512 consecutive OC cycles and then shut down without delay |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | The device continues operation and never shut down when OCP happens |

### IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in ampere, that causes an output overcurrent warning. This is a read and write register. The IOUT_OC_WARN_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the IOUT_OC_WARN_LIMIT command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 1 5: 0 | Linear 11 | F868h | The IOUT_OC_WARN_LIMIT is 52 A SiC450 |
| | | F841h | The IOUT_OC_WARN_LIMIT is 32.5 A for SiC451 |
| | | F827h | The IOUT_OC_WARN_LIMIT is 19.5 A for SiC453 |

The IOUT_OC_WARN_LIMIT range is 0 A to 127 A, resolution is 0.5 A, and its NVM register default store value is F841h for SiC451 equivalent to 32.5 A. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### OT_FAULT_LIMIT (4Fh)

The OT FAULT LIMIT command sets the temperature of the unit, in degree celsius, at which it should indicate an overtemperature fault. This is a read and write register. The OT_FAULT_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the OT_FAULT_LIMIT command is constant as 5'b00000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15:0 | Linear 11 | 007Dh | The OT_FAULT_LIMIT is specified as 125 °C |

The OT_FAULT_LIMIT range is 0 °C to 150 °C, resolution is 1 °C, and its NVM register default store value is 007Dh equivalent to 125 °C. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### OT_FAULT_RESPONSE (50h)

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an overtemperature fault. This is a read and write register and the NVM register default store value is F9h.

| COMMAND | OT FAULT RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | OTRSP | | OTRTY | | | OTDLY | | |
| Default (F9h) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

**Supported Commands**

| OTRSP | | OTRTY | | | OTDLY | | | DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It attempts to restart continuously, without limitation, until it is commanded off (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The device continues operation |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |

**OT_WARN_LIMIT (51h)**

The OT_WARN_LIMIT command sets the temperature of the unit, in degree celsius, at which it should indicate an overtemperature warning alarm. This is a read and write register. The OT_WARN_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the OT_WARN_LIMIT command is constant as 5'b00000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0069h | The OT_WARN_LIMIT is specified as 105 °C |

The OT_WARN_LIMIT range is 0 °C to 150 °C, resolution is 1 °C, and its NVM register default store value is 0069h equivalent to 105 °C. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

**VIN_OV_FAULT_LIMIT (55h)**

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage, in volt, that causes an input overvoltage fault. This is a read and write register. The VIN_OV_FAULT_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the VIN_OV_FAULT_LIMIT command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | F81Eh | The VIN_OV_FAULT_LIMIT is specified as 15 V |

The VIN_OV_FAULT_LIMIT range is 1 V to 80 V, resolution is 0.5 V, and its NVM register default store value is F81Eh equivalent to 15 V. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

**VIN_OV_FAULT_RESPONSE (56h)**

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. This is a read and write register and the NVM register default store value is B8h.

| COMMAND | VIN_OV_FAULT_RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | VIOVRSP | | VIOVRTY | | | VIOVDLY | | |
| Default (B8h) | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

**Supported Commands**

| OTRSP | | OTRTY | | | OTDLY | | | DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | This command deviates from standard PMBus 1.3 specifications. The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It does not attempt to restart. The output remains disabled until the fault is cleared |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The device continues operation |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | The device continues operation |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | The device continues operation |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. It does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |

### VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command sets the value of the input voltage, in volt, that causes an input voltage low warning. This is a read and write register. The VIN_UV_WARN_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the VIN_UV_WARN_LIMIT command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | F812h | The VIN_UV_WARN_LIMIT is specified as 9 V |

The VIN_UV_WARN_LIMIT range is 1 V to 80 V, resolution is 0.5 V, and its NVM register default store value is F812h equivalent to 9 V. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### IIN_OC_WARN_LIMIT (5Dh)

The IIN_OC_WARN_LIMIT command sets the value of the input current, in ampere, that causes an input current overcurrent Warning. This is a read and write register. The IIN_OC_WARN_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the IIN_OC_WARN_LIMIT command is constant as 5'b11111, that is, -1 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | F80Ah | The IIN_OC_WARN_LIMIT is specified as 5 A |

The IIN_OC_WARN_LIMIT range is 0 A to 127 A, resolution is 0.5 A, and its NVM register default store value is F80Ah equivalent to 5 A. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### POWER_GOOD_ON (5Eh)

The POWER_GOOD_ON command sets the value of the output voltage at which an optional power good signal should be asserted, indicating that the output voltage is valid. This is a read and write register. The POWER_GOOD_ON uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Ulinear 16 | 0114h | The POWER_GOOD_ON is specified as 0.54 V |

The POWER_GOOD_ON range is 0.24 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0114h equivalent to 0.54 V.

### POWER_GOOD_OFF (5Fh)

The POWER_GOOD_OFF command sets the value of the output voltage at which an optional power good signal should be negated, indicating that the output voltage is not valid. This is a read and write register. The POWER_GOOD_OFF uses ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Ulinear 16 | 0105h | The POWER_GOOD_OFF is specified as 0.51 V |

The POWER_GOOD_OFF range is 0.24 V to 14 V, resolution is 1.953 mV, and its NVM register default store value is 0105h equivalent to 0.51 V.

### TON_DELAY(60h)

The TON_DELAY command sets the time, in millisecond, from which a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. This is a read and write register. The TON_DELAY uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5 bit two's complement exponent of the TON_DELAY command is constant as 5'b0000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0000h | The TON_DELAY is specified as 0 ms |

The TON_DELAY range is 0 ms to 127 ms, resolution is 1 ms, and its NVM register default store value is 0000h equivalent to 0 ms. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### TON_RISE (61h)

The TON_RISE command sets the time, in millisecond, from when the output starts to rise until the voltage has entered the regulation band. This is a read and write register. The TON_RISE uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the TON_RISE command is constant as 5'b0000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0005h | The TON_RISE is specified as 5 ms |

The TON_RISE range is 0 ms to 127 ms, resolution is 1 ms, and its NVM register default store value is 0005h equivalent to 5 ms. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### TON_MAX_FAULT_LIMIT (62h)

The TON_MAX_FAULT_LIMIT command sets an upper limit, in millisecond, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. This is a read and write register. The TON_MAX_FAULT_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the TON_MAX_FAULT_LIMIT command is constant as 5'b0000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0014h | The TON_MAX_FAULT_LIMIT is specified as 20 ms |

The TON_MAX_FAULT_LIMIT range is 0 ms to 127 ms, resolution is 1 ms, and its NVM register default store value is 0014h equivalent to 20 ms. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### TON_MAX_FAULT_RESPONSE (63h)

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to an input overcurrent fault. This is a read and write register and the NVM register default store value is B9h.

| COMMAND | TON_MAX_FAULT_RESPONSE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Function | ONMXRSP | | ONMXRTY | | | ONMXDLY | | |
| Default (0xB9h) | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

**Supported Commands**

| ONMXRSP | | ONMXRTY | | | ONMXDLY | | | DESCRIPTIONS |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | The device shuts down (disables the output). It attempts to restart continuously, without limitation, until it is commanded off (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. 20 ms delay |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | The device shuts down (disables the output). It does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | The device shuts down (disables the output). It does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | The device shuts down (disables the output). It does not attempt to restart. The output remains disabled until the fault is cleared |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | The device shuts down (disables the output). It attempts to restart 1 time. No delay |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | The device shuts down (disables the output). It attempts to restart 1 time. 20 ms delay |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | The device shuts down (disables the output). It attempts to restart 1 time. 30 ms delay |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | The device shuts down (disables the output). It attempts to restart 1 time. 40 ms delay |

**TOFF_DELAY (64h)**

The TOFF_DELAY command sets the time, in millisecond, from when a stop condition is received until the unit stops transferring energy to the output. This is a read and write register. The TOFF_DELAY uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the TOFF_DELAY command is constant as 5'b0000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0000h | The TOFF_DELAY is specified as 0 ms |

The TOFF_DELAY range is 0 ms to 127 ms, resolution is 1 ms, and its NVM register default store value is 0000h equivalent to 0 ms. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

**TOFF_FALL (65h)**

The TOFF_FALL command sets the time, in millisecond, from the end of the turn-off delay time until the voltage is commanded to zero. Note that this command can only be used with a device whose output can sink enough current to cause the output voltage to decrease at a controlled rate. This is a read and write register. The TOFF_FALL uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5-bit two's complement exponent of the TOFF_FALL command is constant as 5'b0000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 0005h | The TOFF_FALL is specified as 5 ms |

The TOFF_FALL range is 0 ms to 127 ms, resolution is 1 ms, and its NVM register default store value is 0005h equivalent to 5 ms. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

**TOFF_MAX_WARN_LIMIT (66h)**

The TOFF_MAX_WARN_LIMIT command sets an upper limit, in millisecond, on how long the unit can attempt to power down the output without reaching 12.5 % of the output voltage programmed at the time the unit is turned off. This is a read and write register. The TOFF_MAX_WARN_LIMIT uses LINEAR11 format, which has two data bytes with an 11-bit two's complement mantissa and a 5-bit two's complement exponent (scaling factor). The 5- bit two's complement exponent of the TOFF_MAX_WARN_LIMIT command is constant as 5'b0000, that is, 0 in decimal. The LINEAR11 format of the two data bytes is illustrated in Table - "LINEAR11 Numeric Format Data Bytes".

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 : 0 | Linear 11 | 003Ch | The TOFF_MAX_WARN_LIMIT is specified as 60 ms |

The TOFF_MAX_WARN_LIMIT range is 0 ms to 127 ms, resolution is 1 ms, and its NVM register default store value is 003Ch equivalent to 60 ms. Any commands out of the valid range or with incorrect resolution will be ignored and reported.

### STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. The STATUS_BYTE message content is described in the table below. This is a read register.

**Table - STATUS_BYTE Message Contents**

| BIT | STATUS BIT NAME | MEANING |
|---|---|---|
| 7 | BUSY | A fault was declared because the device was busy and unable to respond |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled |
| 5 | VOUT_OV_FAULT | An output overvoltage fault has occurred |
| 4 | IOUT_UV_FAULT | An output overcurrent fault has occurred |
| 3 | VIN_UV_FAULT | An input undervoltage fault has occurred |
| 2 | Temperature | A temperature fault or warning has occurred |
| 1 | CML | A communications, memory or logic fault has occurred |
| 0 | None of the above | A fault or warning not listed in bits (7 to 1) has occurred |

### STATUS_WORD (79h)

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the status word is the same register as the STATUS_BYTE command. The STATUS_WORD message content is described in the following table. This is a read register.

| BYTE | BIT | STATUS BIT NAME | MEANING |
|---|---|---|---|
| Low | 7 | Busy | A fault was declared because the device was busy and unable to respond |
| | 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled |
| | 5 | VOUT_OV_FAULT | An output overvoltage fault has occurred |
| | 4 | IOUT_UV_FAULT | An output overcurrent fault has occurred |
| | 3 | VIN_UV_FAULT | An input undervoltage fault has occurred |
| | 2 | Temperature | A temperature fault or warning has occurred |
| | 1 | CML | A communications, memory or logic fault has occurred |
| | 0 | None of the above | A fault or warning not listed in bits [7 : 1] has occurred |
| High | 7 | $V_{OUT}$ | An output voltage fault or warning has occurred |
| | 6 | $I_{OUT}$ / $P_{OUT}$ | An output current or output power fault or warning has occurred |
| | 5 | Input | An input voltage, input current, or input power fault or warning has occurred |
| | 4 | MFR specific | A manufacturer specific fault or warning has occurred |
| | 3 | $P_G$ status # | The power good signal, if present, is negated |
| | 2 | Fans | Not available |
| | 1 | Other | Not available |
| | 0 | Unknown | Not available |

### STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one byte with contents described in the following table. This is a read register.

| BIT | MEANING |
|---|---|
| 7 | $V_{OUT}$ OV fault (output overvoltage fault) |
| 6 | $V_{OUT}$ OV warning (output overvoltage warning) |
| 5 | $V_{OUT}$ UV warning (output undervoltage warning) |
| 4 | $V_{OUT}$ OV fault (output undervoltage fault) |
| 3 | $V_{OUT}$ max. min. (an attempt has been made to set the output voltage toa value higher than allowed by the $V_{OUT}$ max. or lower than the limited allowed by the $V_{OUT}$ min.) |
| 2 | $t_{ON}$ max. fault |
| 1 | $t_{OFF}$ max. warning |
| 0 | Not available |

### STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one byte with contents described in the following table. This is a read register.

| BIT | MEANING |
|---|---|
| 7 | $I_{OUT}$ OC fault (output overcurrent fault) |
| 6 | Not available |
| 5 | $I_{OUT}$ OC warning (output overcurrent warning) |
| 4 | Not available |
| 3 | Not available |
| 2 | Not available |
| 1 | Not available |
| 0 | Not available |

### STATUS_INPUT (7Ch)

The STATUS_INPUT command returns one byte with contents described in the following table. This is a read register.

| BIT | MEANING |
|---|---|
| 7 | $V_{IN}$ OV fault (input overvoltage fault) |
| 6 | Not available |
| 5 | $V_{IN}$ UV warning (input undervoltage warning) |
| 4 | Not available |
| 3 | Unit off for insufficient input voltage |
| 2 | Not available |
| 1 | $I_{IN}$ OC warning (input overcurrent warning) |
| 0 | Not available |

### STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one byte with contents described in the following table. This is a read register.

| BIT | MEANING |
|---|---|
| 7 | OT fault (overtemperature fault) |
| 6 | OT warning (overtemperature warning) |
| 5 to 0 | Not available |

### STATUS_CML (7Eh)

The STATUS_CML command returns one byte with contents described in the following table. This is a read register.

| BIT | MEANING |
|---|---|
| 7 | Invalid or unsupported command received |
| 6 | Invalid or unsupported data received |
| 5 | Packet error check failed |
| 4 | Memory fault detected |
| 3 | Not available |
| 2 | Reserved |
| 1 | A communication fault other than the ones listed in this table has occurred |
| 0 | Not available |

### STATUS_MFR Specific (80h)

The STATUS_MFR specific command returns one byte with contents described in the following table. This is a read register.

| BIT | MEANING |
|---|---|
| 7 to 4 | Not available |
| 3 | IL master fault |
| 2 | YF verify fault |
| 1 | YF erase fault |
| 0 | YF PGM fault |

**READ_VIN (88h)**

The READ_VIN command returns the input voltage in volt. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**READ_IIN (89h)**

The READ_IIN command returns the input current in ampere. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**READ_VOUT (8Bh)**

The read $V_{OUT}$ command returns the actual, measured output voltage in volt. The two data bytes are encoded in ULINEAR16 format, which is a 16-bit unsigned integer according to the setting of the VOUT_MODE command. This is a read register.

**READ_IOUT (8Ch)**

The READ_IOUT command returns the measured output current in ampere. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**READ_TEMPERATURE (8Dh)**

The READ_TEMPERATURE command returns the measured temperature of the PMBus unit in degree celsius. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**READ_DUTY_CYCLE (94h)**

The READ_DUTY_CYCLE command returns the duty of the PMBus unit’s power conversion in percent. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**READ_POUT (96h)**

The READ_POUT command returns the output power, in watt, of the PMBus unit. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**READ_PIN (97h)**

The READ_PIN command returns the input power, in watt, of the PMBus unit. The two data bytes are encoded in LINEAR11 format. The LINEAR11 format of the two data bytes is illustrated in Table - “LINEAR11 Numeric Format Data Bytes”. This is a read register.

**PMBus_REVISION (98h)**

The PMBUS_REVISION command stores or reads the revision of the PMBus to which the device is compliant. The command has one data byte. Bits (7 to 4) indicate the revision of PMBus specification Part I to which the device is compliant. Bits (3 to 0) indicate the revision of PMBus specification part II to which the device is compliant. The permissible values are shown in the table below. This is a read register.

**Table - PMBUS_REVISION DATA Byte Contents**

| BITS (7 TO 4) | PART I REVISION | BIT (3 TO 0) | PART II REVISION |
|---|---|---|---|
| 0000b | 1.0 | 0000b | 1.0 |
| 0001b | 1.1 | 0001b | 1.1 |
| 0010b | 1.2 | 0010b | 1.2 |
| 0011b | 1.3 | 0011b | 1.3 |

**MFR_SERIAL (9Eh)**

The MFR_SERIAL command is used to store user’s customized information. This is a read and write 16-bit block register.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 to 0 | Block | 0000h | A block register to store user’s customized information |

### IC_DEVICE_ID (ADh)

The IC_DEVICE_ID command is used to either set or read the type or part number of an IC embedded within a PMBus that is used for the PMBus interface. Each manufacturer uses the format of their choice for the IC device identification. IC_DEVICE_ID is typically only set once, at the time of manufacture.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 to 0 | Block | 0000h | The part number of the unit |

### MFR_BASE_ADDRESS (D7h)

The MFR_BASE_ADDRESS command is used to read or set the unit's PMBus address when a designated voltage setting resistor is assembled between $V_{SET}$ pin of the PMBus unit and ground. The four least significant bits (LSB) [3 : 0] of the MFR_BASE_ADDRESS are set by resistance of the resistor assembled between ADDR pin and ground. The three most significant bits (MSB) [6 : 4] of the MFR_BASE_ADDRESS are set by the MSB [6 : 4] 3-bit of the MFR_BASE_ADDRESS NVM register store value. The default store value of MFR_BASE_ADDRESS NVM register is 10h. This is a read and write register.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 6 to 0 | Pins program | 10h | NVM register of MFR_BASE_ADDRESS default store value is 10h. Thus, MSB 3-bit [6 : 4] of MFR_BASE_ADDRESS is 001b. When a 0.845 kΩ resistor is connected between ADDR pin and ground and a Vout setting resistor is connected between $V_{SET}$ pin and ground, the LSB 4-bit [3 : 0] of MFR_BASE_ADDRESS is 0000b. |

### EEPROM_PASSWORD (DBh)

The EEPROM_PASSWORD command will unlock write access to the internal NVM. This command must be sent before the STORE_USER_ALL command. Access to the NVM can be disabled by sending any other data and will be automatically disabled on each power-cycle.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 15 to 0 | Block | 1234h | Default password for unlocking access to the NVM before the STORE_USER_ALL command |

### MFR_BASE_ADDRESS_2 (E2h)

The MFR_BASE_ADDRESS_2 command is used to read or set the unit's PMBus address when there is no voltage setting resistor assembled between $V_{SET}$ pin of the PMBus unit and ground. The four least significant bits (LSB) [3 : 0] of the MFR_BASE_ADDRESS_2 are set by resistance of the resistor assembled between ADDR pin and ground. The MSB [6 : 4] 3-bit of the MFR_BASE_ADDRESS_2 are set by the MSB [6 : 4] 3-bit of MFR_BASE_ADDRESS_2 NVM register store value. The default store value of MFR_BASE_ADDRESS_2 NVM register is 50h. This is a read and write register.

**Bit Description**

| BITS | SYMBOL | VALUE | ACTION |
|---|---|---|---|
| 6 to 0 | Pins program | 50h | NVM register of MFR_BASE_ADDRESS_2 default store value is 50h. Thus, MSB 3-bit [6 : 4] of MFR_BASE_ADDRESS_2 is 101b. When a 0.845 kΩ resistor is connected between ADDR pin and ground and there is not a $V_{OUT}$ setting resistor assembled between $V_{SET}$ pin and ground, the LSB 4-bit [3 : 0] of MFR_BASE_ADDRESS_2 is 0000b. |

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC453 (15 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

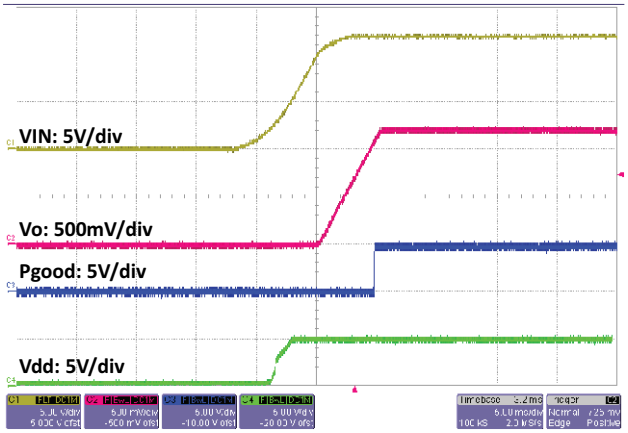



**Fig. 11 - SiC453 Startup with $V_{IN}$, t = 5 ms/div**

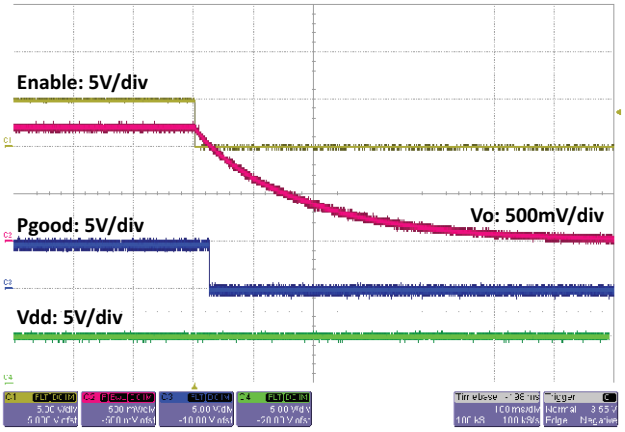



**Fig. 14 - SiC453 Shut down with EN, t = 100 ms/div**

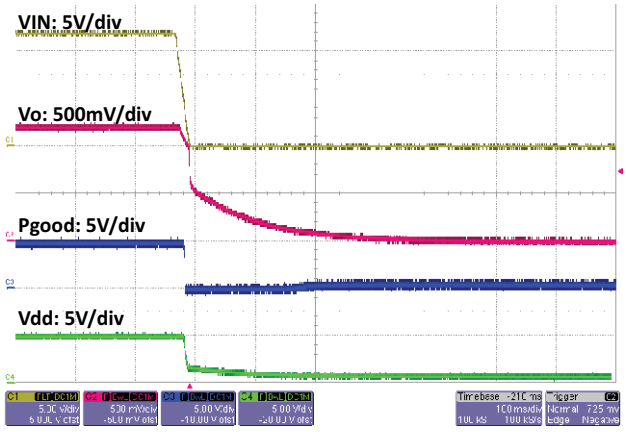



**Fig. 12 - SiC453 Shut Down with $V_{IN}$, t = 100 ms/div**

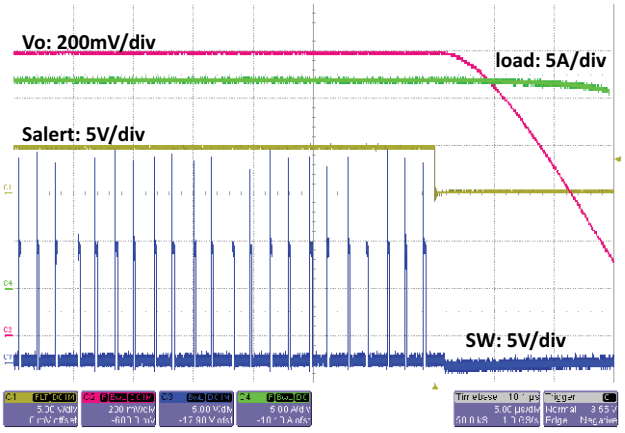



**Fig. 15 - SiC453 OCP**

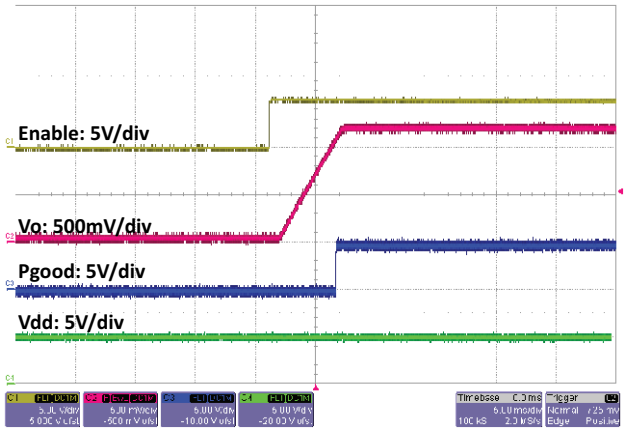



**Fig. 13 - SiC453 Startup with EN, t = 5 ms/div**

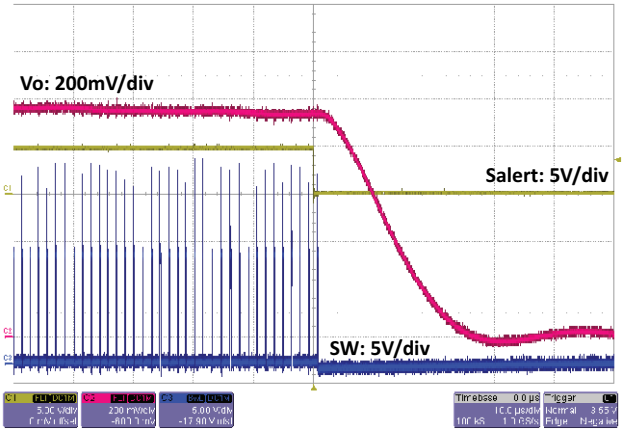



**Fig. 16 - SiC453 UVP**

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC453 (15 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

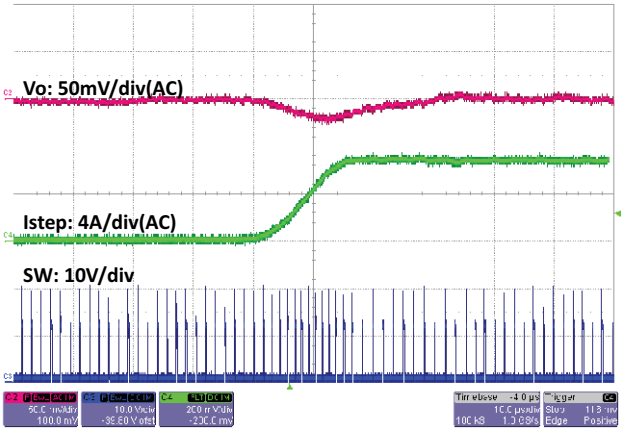



**Fig. 17 - SiC453 Load Step, 7.5 A to 15 A, 1 A/µs, t = 10 µs/div**

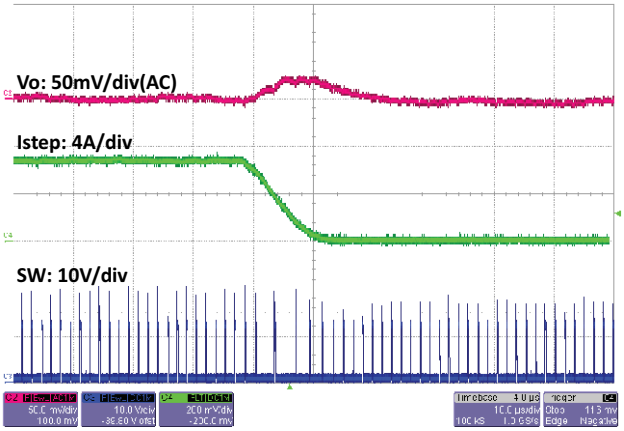



**Fig. 20 - SiC453 Load Step, 0 A to 7.5 A, 1 A/µs, t = 10 µs/div**

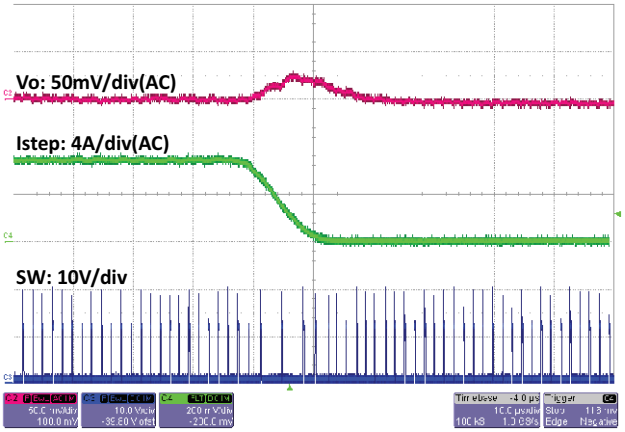



**Fig. 18 - SiC453 Load Step, 15 A to 7.5 A, 1 A/µs, t = 10 µs/div**

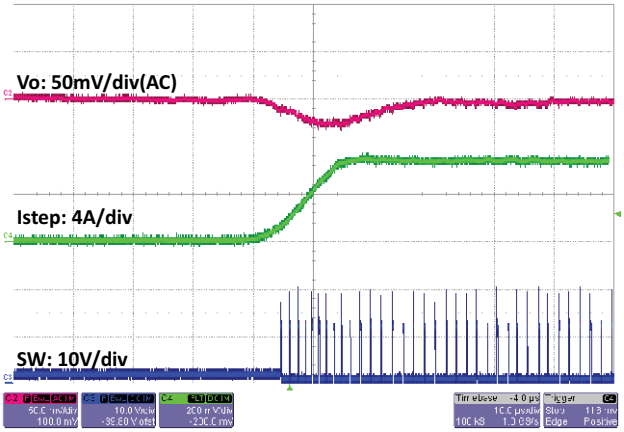



**Fig. 21 - SiC453 Load Step, 0 A to 7.5 A, 1 A/µs, t = 10 µs/div Skip Mode Enabled**

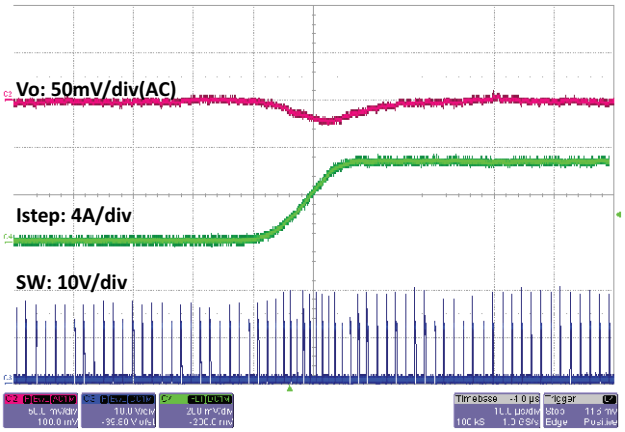



**Fig. 19 - SiC453 Load Step, 0 A to 7.5 A, 1 A/µs, t = 10 µs/div**

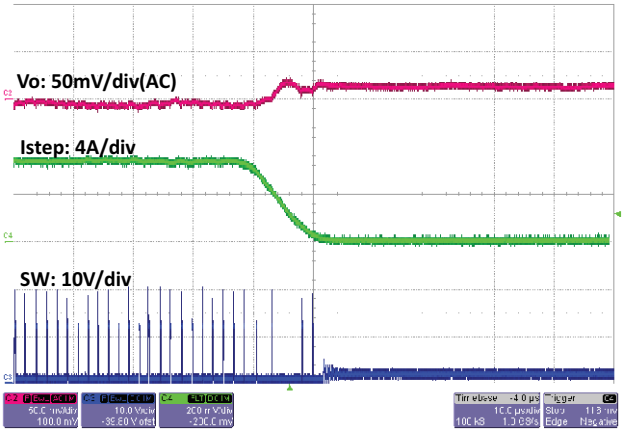



**Fig. 22 - SiC453 Load Step, 7.5 A to 0 A, 1 A/µs, t = 10 µs/div Skip Mode Enabled**

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC453 (15 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

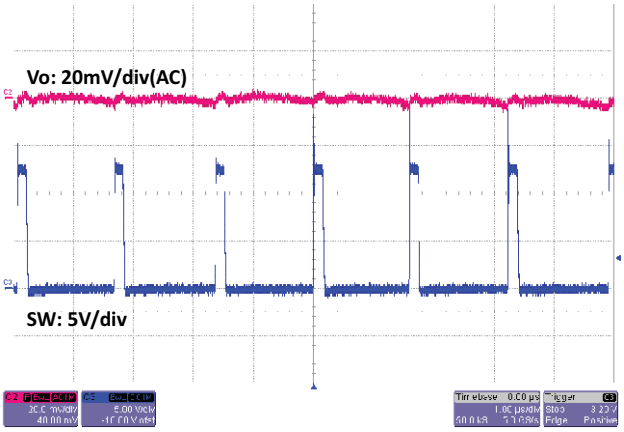



**Fig. 23 - SiC453 Output Ripple, 0.01 A, t = 1 µs/div Forced Continuous Conduction Mode**

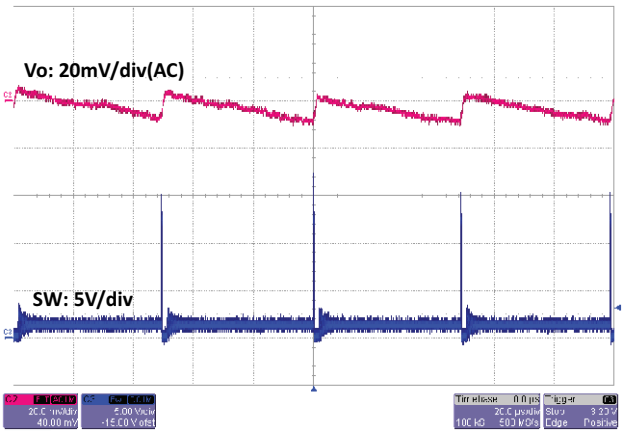



**Fig. 24 - SiC453 Output Ripple, 0.01 A, t = 20 µs/div DCM Mode**

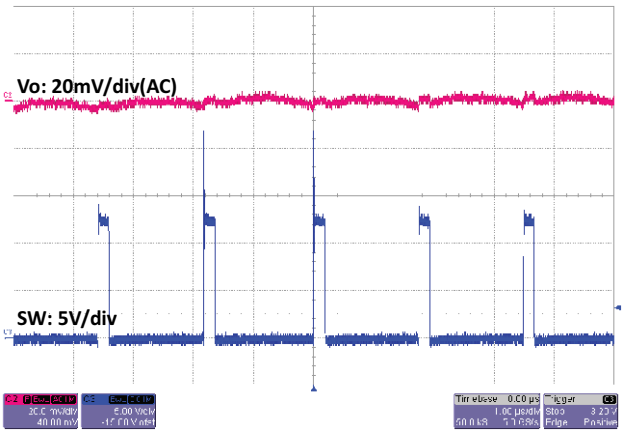



**Fig. 25 - SiC453 Output Ripple, 7.5 A, t = 1 µs/div**

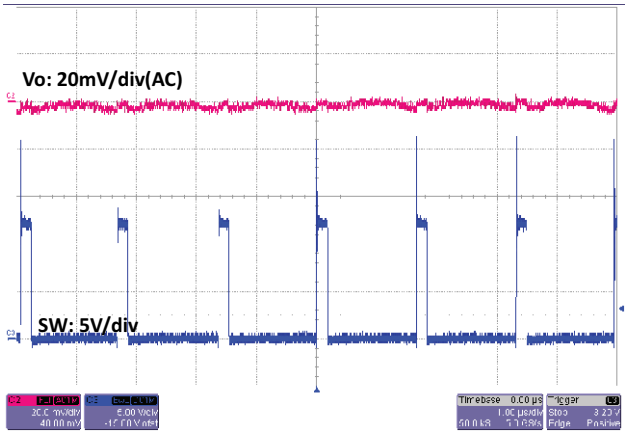



**Fig. 26 - SiC453 Output Ripple, 15 A, t = 1 µs/div**

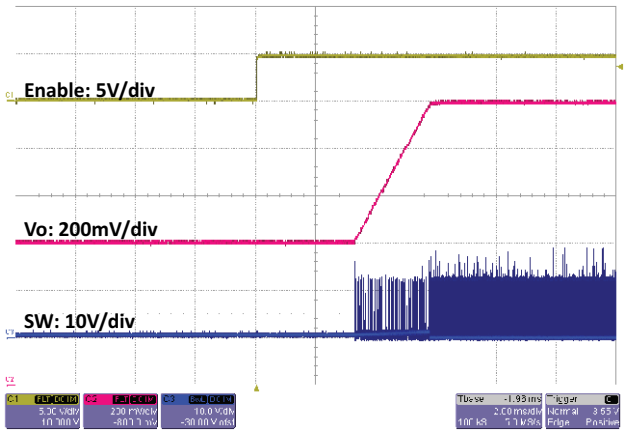



**Fig. 27 - SiC453 Prebias Startup**

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC451 (25 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

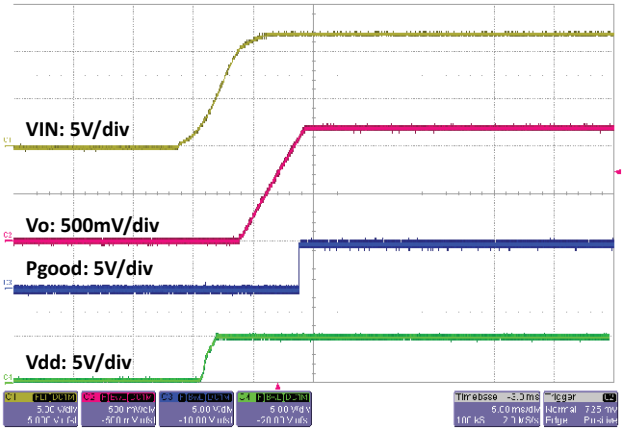



Fig. 28 - SiC451 Startup with $V_{IN}$, t = 5 ms/div

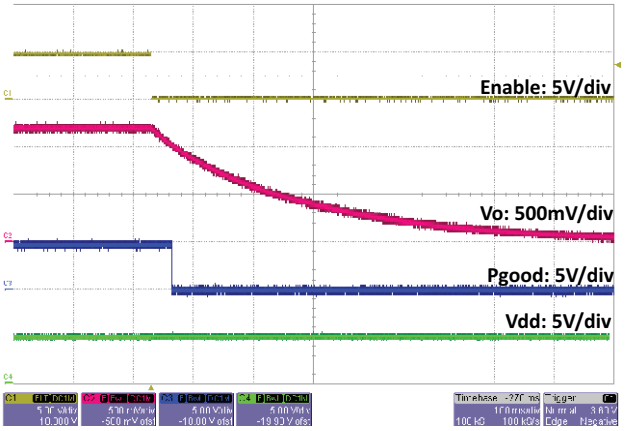



Fig. 31 - SiC451 Shut down with EN, t = 100 ms/div

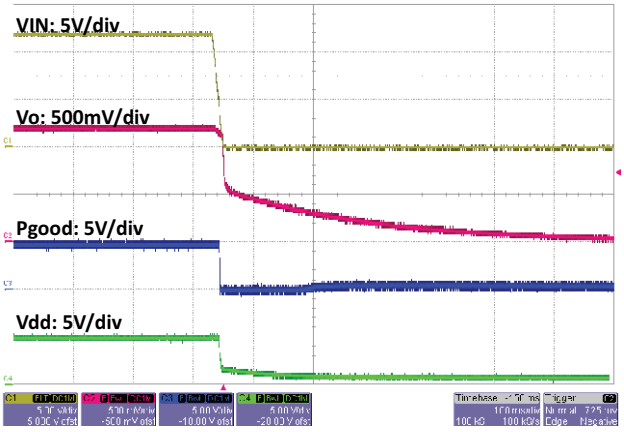



Fig. 29 - SiC451 Shut Down with $V_{IN}$, t = 100 ms/div

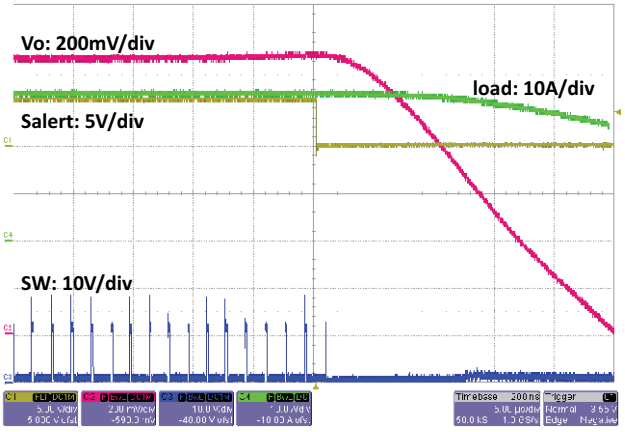



Fig. 32 - SiC451 OCP

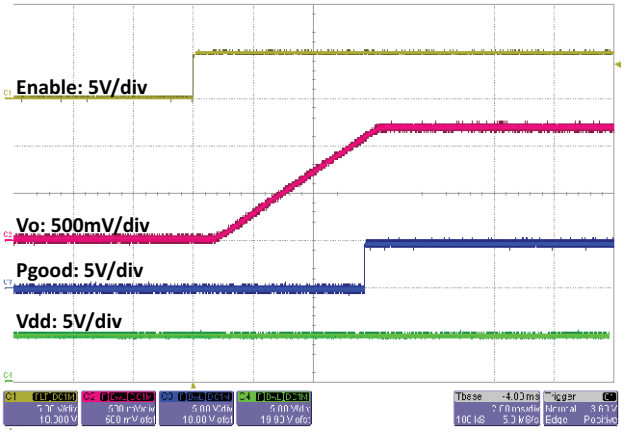



Fig. 30 - SiC451 Startup with EN, t = 2 ms/div

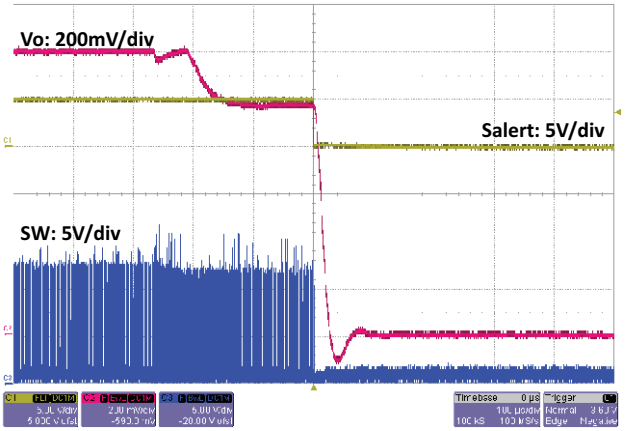



Fig. 33 - SiC451 UVP

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC451 (25 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

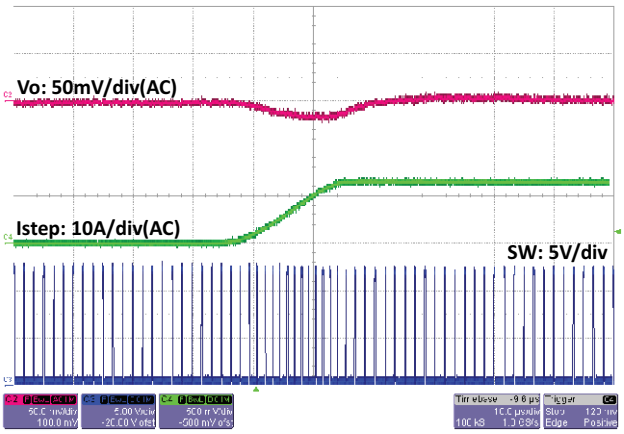



**Fig. 34 - SiC451 Load Step, 12.5 A to 25 A, 10 A/µs, t = 10 µs/div**

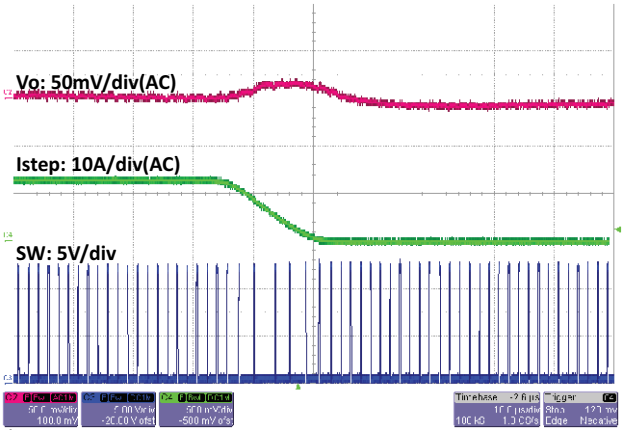



**Fig. 35 - SiC451 Load Step, 25 A to 12.5 A, 1 A/µs, t = 10 µs/div**

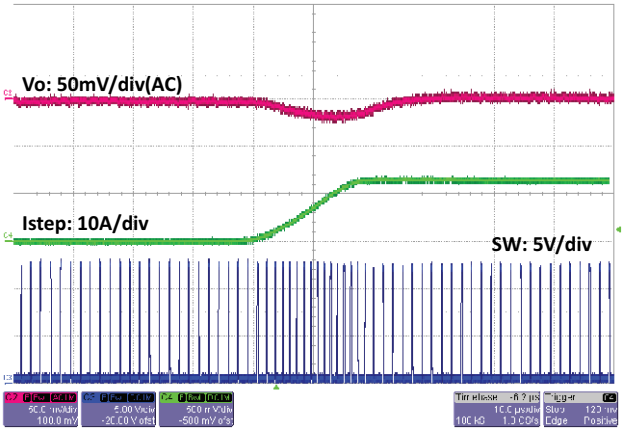



**Fig. 36 - SiC451 Load Step, 0 A to 12.5 A, 1 A/µs, t = 10 µs/div**

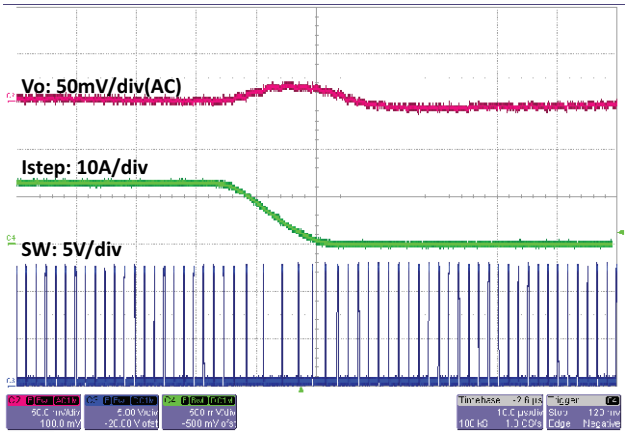



**Fig. 37 - SiC451 Load Step, 12.5 A to 0 A, 1 A/µs, t = 10 µs/div**

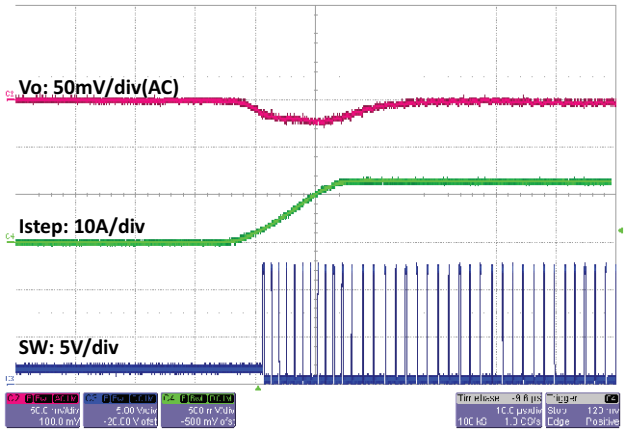



**Fig. 38 - SiC451 Load Step, 0 A to 12.5 A, 1 A/µs, t = 10 µs/div Skip Mode Enabled**

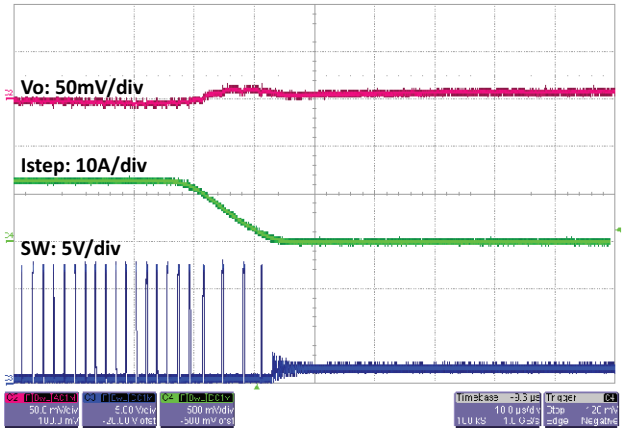



**Fig. 39 - SiC451 Load Step, 12.5 A to 0 A, 1 A/µs, t = 10 µs/div Skip Mode Enabled**

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC451 (25 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

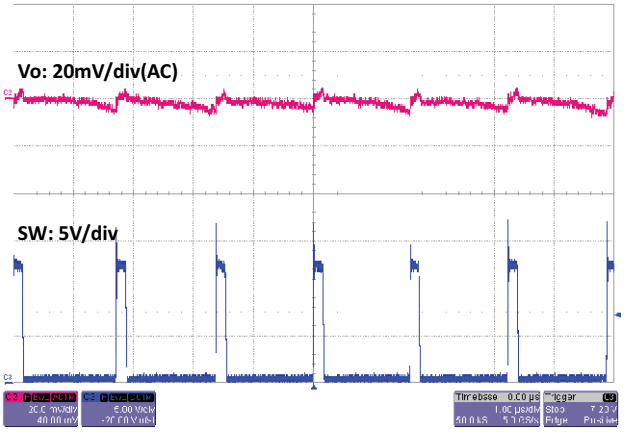



**Fig. 40 - SiC451 Output Ripple, 0.01 A, t = 1 µs/div Forced Continuous Conduction Mode**

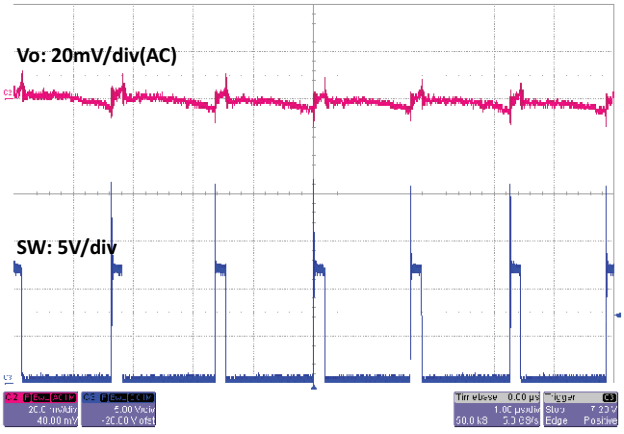



**Fig. 43 - SiC451 Output Ripple, 25 A, t = 1 µs/div Forced Continuous Conduction Mode**

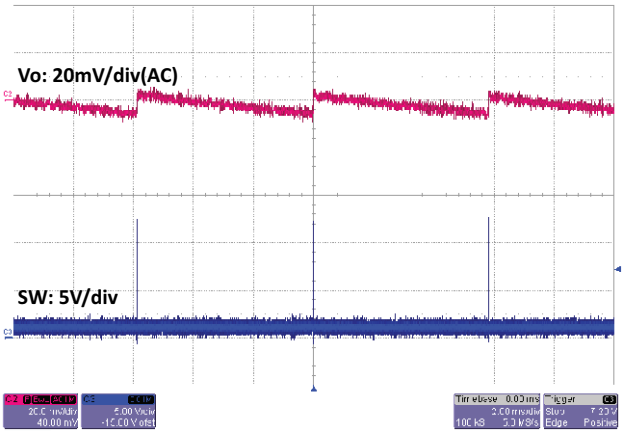



**Fig. 41 - SiC451 Output Ripple, 0.01 A, t = 2 ms/div DCM Mode**

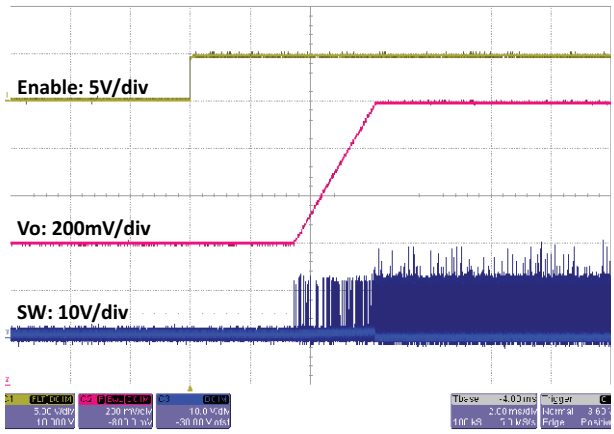



**Fig. 44 - SiC451 Prebias Startup**

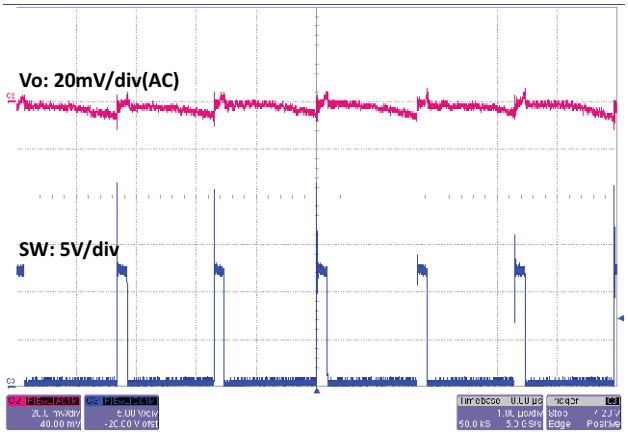



**Fig. 42 - SiC451 Output Ripple, 12.5 A, t = 1 µs/div Forced Continuous Conduction Mode**

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC450 (40 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

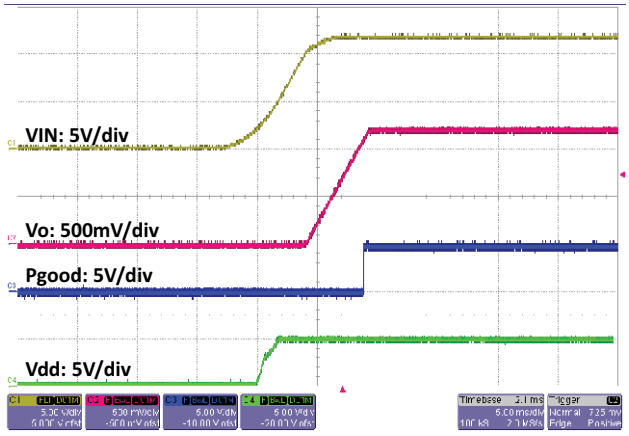



Fig. 45 - SiC450 Startup with $V_{IN}$, t = 5 ms/div

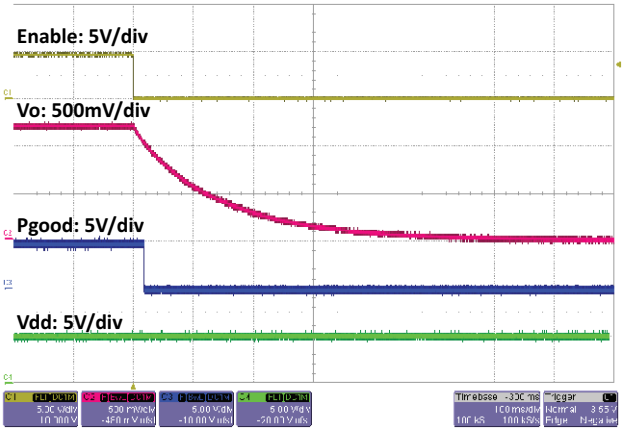



Fig. 48 - SiC450 Shut down with EN, t = 100 ms/div

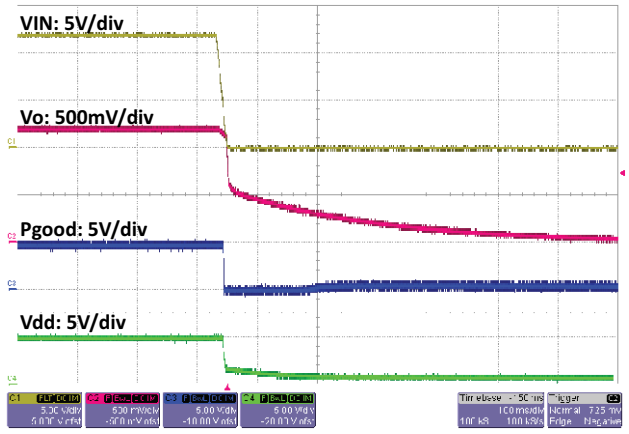



Fig. 46 - SiC450 Shut Down with $V_{IN}$, t = 100 ms/div

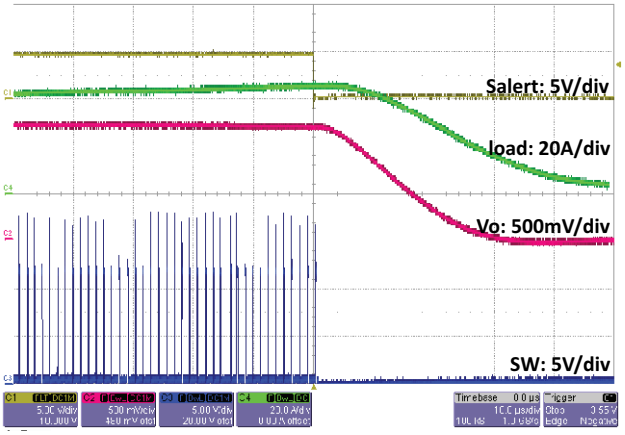



Fig. 49 - SiC450 Overcurrent Protection Behavior, t = 10 µs

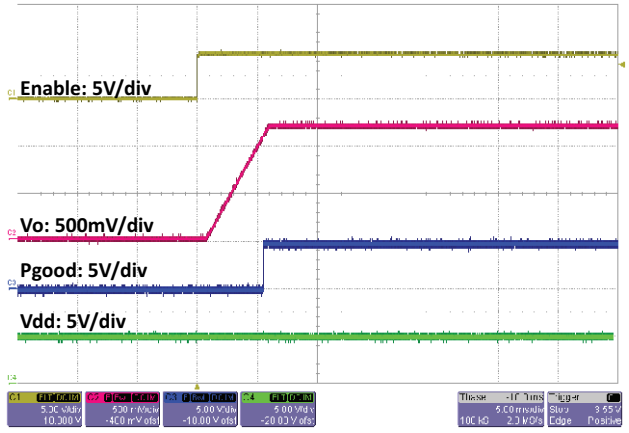



Fig. 47 - SiC450 Startup with EN, t = 5 ms/div

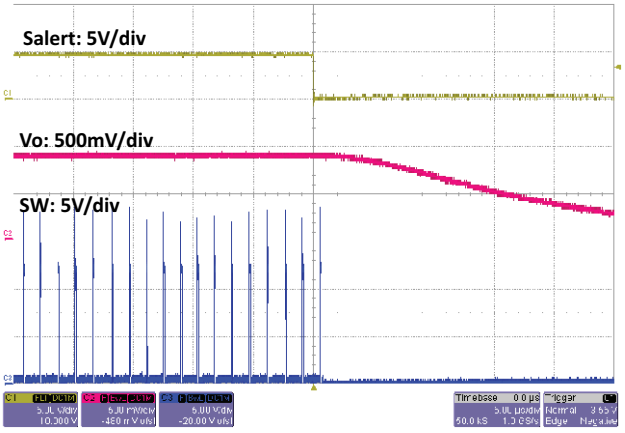



Fig. 50 - SiC450 Output Undervoltage Protection Behavior, t = 5 µs/div

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC450 (40 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

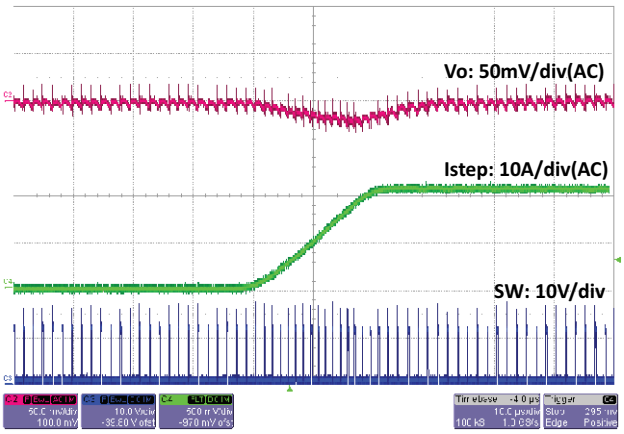



Fig. 51 - SiC450 Load Step, 20 A to 40 A, 1 A/µs, t = 10 µs/div

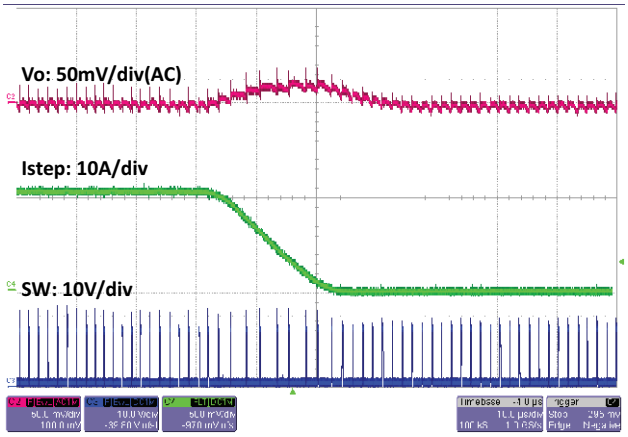



Fig. 54 - SiC450 Load Step, 20 A to 0 A, 1 A/µs, t = 10 µs/div

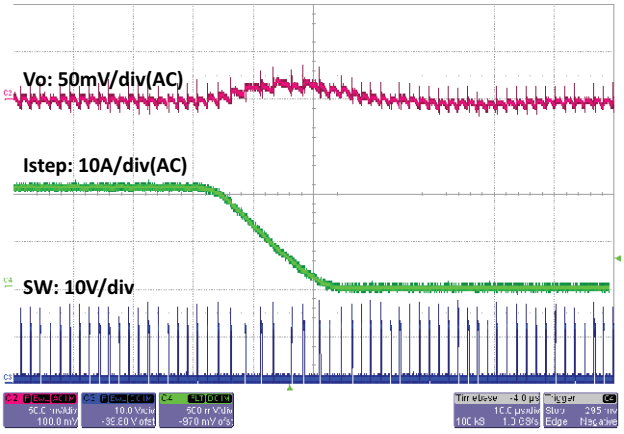



Fig. 52 - SiC450 Load Step, 40 A to 20 A, 10 A/µs, t = 10 µs/div

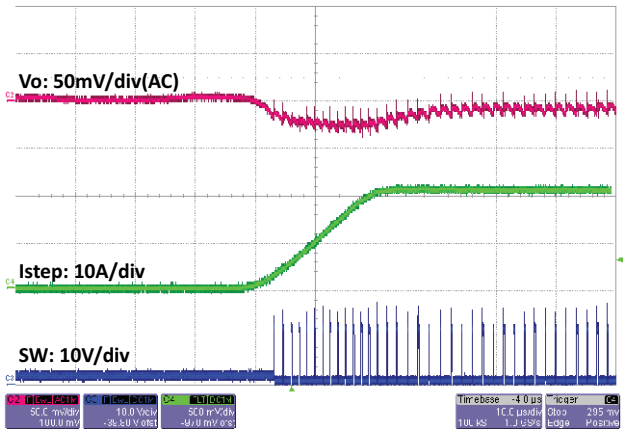



Fig. 55 - SiC450 Load Step, 0 A to 20 A, 1 A/µs, t = 10 µs/div
Skip Mode Enabled

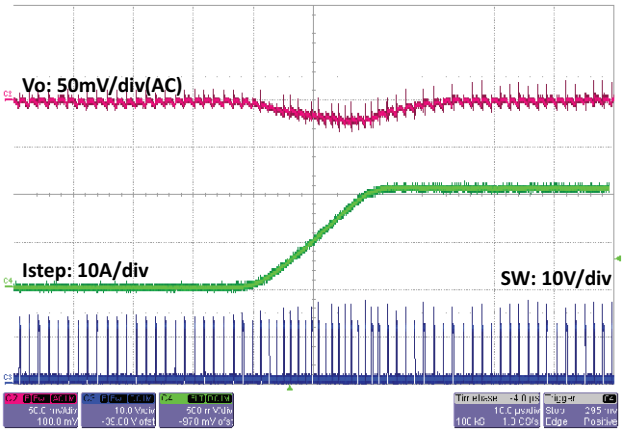



Fig. 53 - SiC450 Load Step, 0 A to 20 A, 1 A/µs, t = 10 µs/div

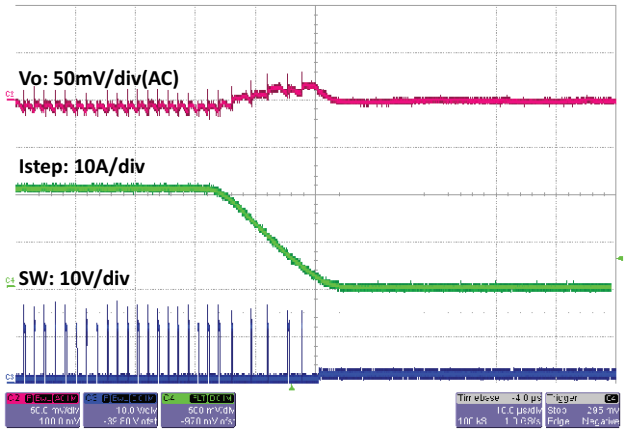



Fig. 56 - SiC450 Load Step, 20 A to 0 A, 1 A/µs, t = 10 µs/div
Skip Mode Enabled

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $f_{sw}$ = 600 kHz, SiC450 (40 A), $C_{IN}$ = 2.2 µF x 3, $C_{OUT}$ = 47 µF x 12, unless otherwise noted)

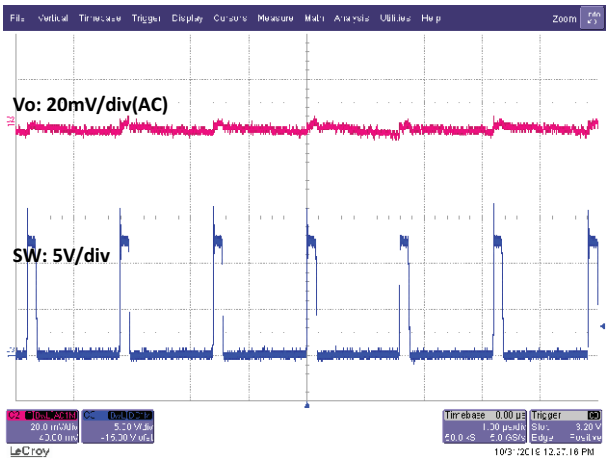



**Fig. 57 - SiC450 Output Ripple, 0.01 A, t = 1 µs/div Forced Continuous Conduction Mode**

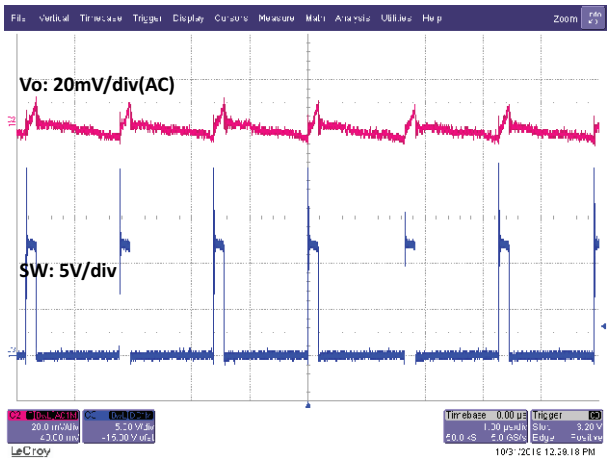



**Fig. 60 - SiC450 Output Ripple, 40 A, t = 1 µs/div Forced Continuous Conduction Mode**

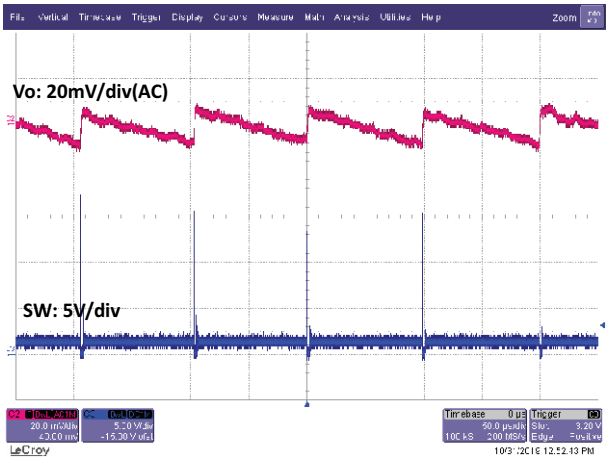



**Fig. 58 - SiC450 Output Ripple, 0.01 A, t = 50 µs/div DCM Mode**

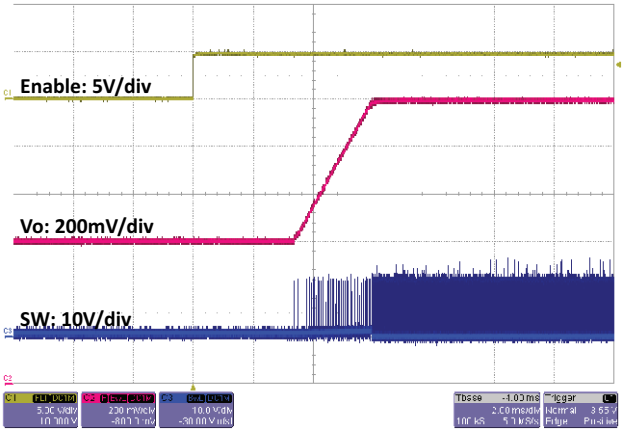



**Fig. 61 - SiC450 Prebias Startup**

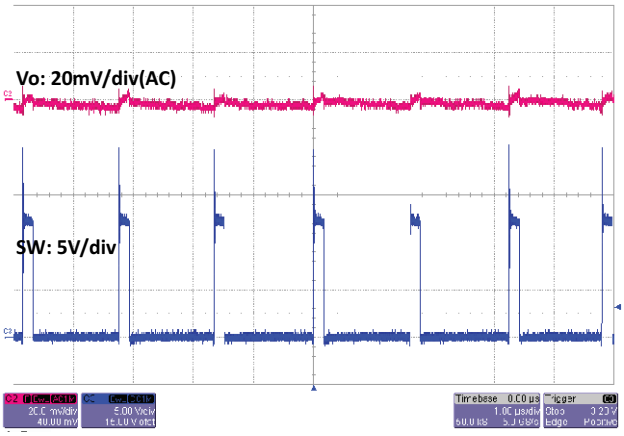



**Fig. 59 - SiC450 Output Ripple, 20 A, t = 1 µs/div Forced Continuous Conduction Mode**

## PCB LAYOUT RECOMMENDATIONS

### Step 1: $V_{IN}$/GND Planes and Decoupling

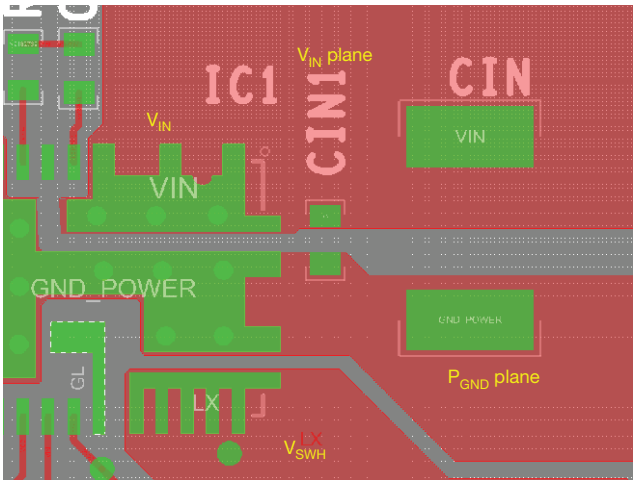



**Fig. 62**

1. Layout $V_{IN}$ and $P_{GND}$ planes as shown above
2. Ceramic capacitors should be placed right between $V_{IN}$ and $P_{GND}$, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 and 0603
4. Smaller capacitance value, closer to device $V_{IN}$ pin(s) - better high frequency noise absorbing

### Step 2: $V_{IN}$ Pin

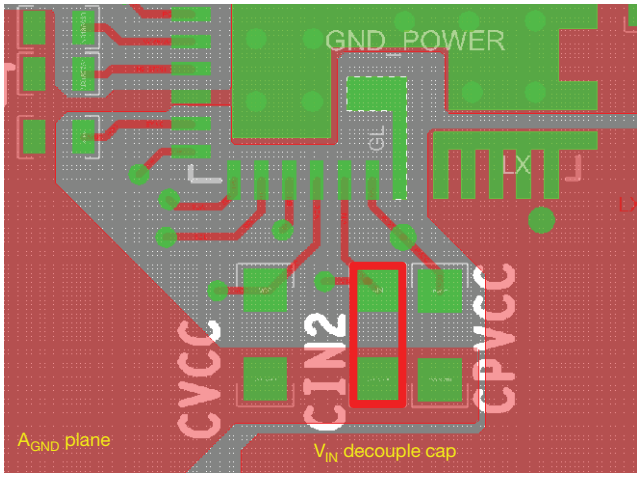



**Fig. 63**

1. $V_{IN}$ (pin 23) is the input pin for both internal LDO and $t_{ON}$ block. $t_{ON}$ time varies based on input voltage. It is necessary to put a decouple cap close to this pin

### Step 3: $V_{SWH}$ Plane

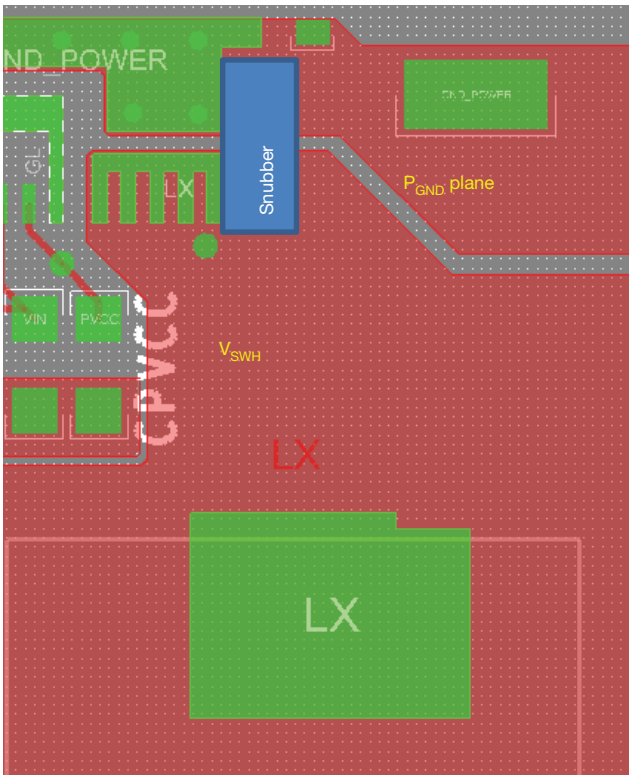



**Fig. 64**

1. Connect output inductor to SiC45x with large plane to lower the resistance
2. If any snubber network is required, place the components on the bottom side as shown above

### Step 4: $V_{DD}$/$PV_{CC}$ Input Filter

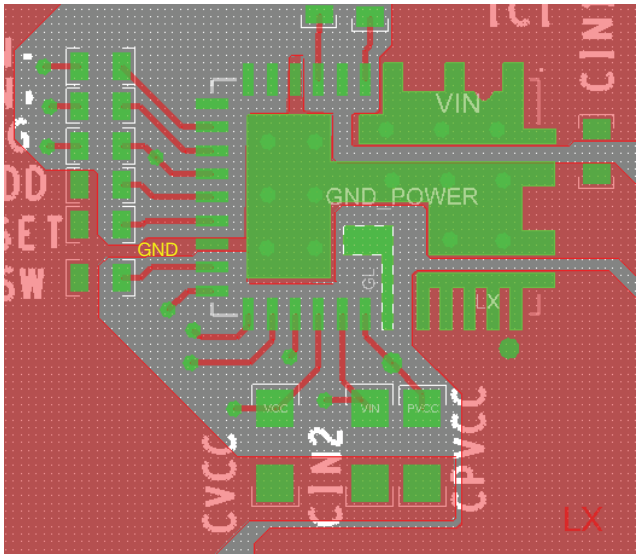



**Fig. 65**

1. $C_{VDD}$ and $C_{PVCC}$ caps should be placed close to the IC to filter noise and provide maximum instantaneous driver current for low side MOSFET during switching cycle

### Step 5: BOOT Resistor and Capacitor Placement

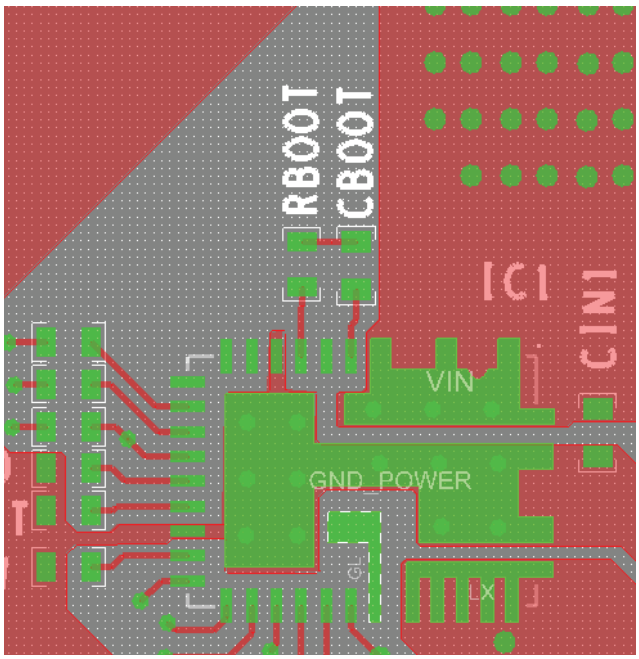



**Fig. 66**

1. These components need to be placed very close to SiC45x, right between PHASE (pin 4) and BOOT (pin 6)
2. To reduce parasitic inductance, chip size 0402 can be used

### Step 6: Signal Routing

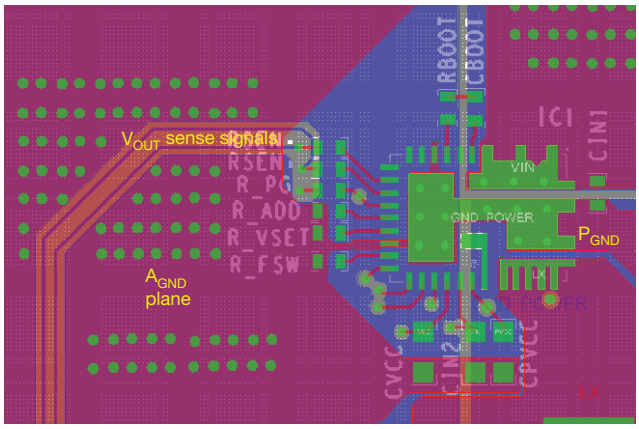



**Fig. 67**

1. Separate the small analog signal from high current path. As shown above, the high current paths with high dv/dt, di/dt are placed on the right side of the IC, while the small control signals are placed on the left side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. Pin 16 is considered as IC analog ground, which should have single connection to power ground. The $A_{GND}$ ground plane connected with pin 16 helps to keep $A_{GND}$ quite and improve noise immunity
3. $V_{sen+}$ / $V_{sen-}$ differential analog signal pair should layout using minimum clearance. Also, the differential pair should be far away from $V_{SWH}$ node and other signals throughout the length of the trace. Ground shield is highly recommended

**Step 7: Adding Thermal Relief Vias and Duplicate Power Path Plane**

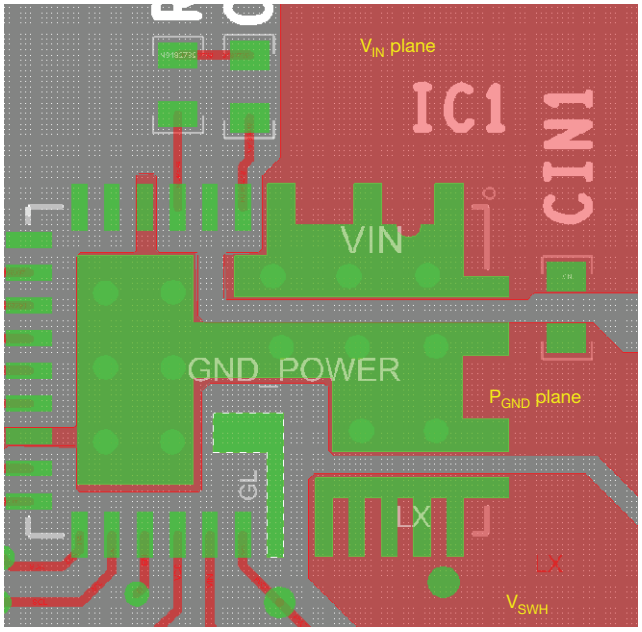



**Fig. 68**

1. Thermal relief Vias can be added on the $V_{IN}$ and $P_{GND}$ pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional Vias can be put on $V_{IN}$ plane and $P_{GND}$ plane. It is also necessary to duplicate the $V_{IN}$ and ground plane at bottom layer to maximize the power dissipation capability from PCB
3. $V_{SWH}$ pad is a noise source and not recommended to put Vias on this pad
4. 8 mil drill for pads and 10 mils drill for plane can be the optional Via size. The Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

**Step 8: Ground Layer**

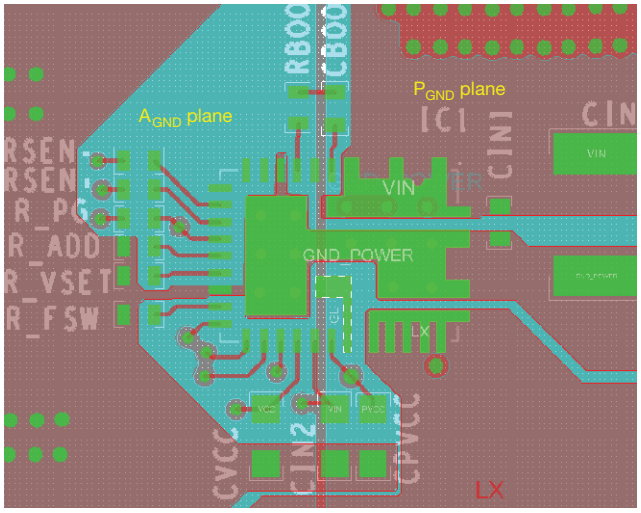



**Fig. 69**

1. It is recommended to make the whole inner 1 layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer
3. The ground plane can be broken into two section as power ground and analogue ground

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| Part number | SiC450 | SiC451 | SiC453 |
| Description | 4.5 V to 20 V input 40 A microBUCK DC/DC converter with PMBus | 4.5 V to 20 V input 25 A microBUCK DC/DC converter with PMBus | 4.5 V to 20 V input 15 A microBUCK DC/DC converter with PMBus |
| Input voltage min. (V) | 4.5 | 4.5 | 4.5 |
| Input voltage max. (V) | 20 | 20 | 20 |
| Output voltage min. (V) | 0.3 | 0.3 | 0.3 |
| Output voltage max. (V) | 12 | 12 | 12 |
| Continuous current (A) | 40 | 25 | 15 |
| Switch frequency min. (kHz) | 300 | 300 | 300 |
| Switch frequency max. (kHz) | 1500 | 1500 | 1500 |
| Pre-bias operation (yes / no) | yes | yes | yes |
| Internal bias reg. (yes / no) | yes | yes | yes |
| Compensation | internal | internal | internal |
| Enable (yes / no) | yes | yes | yes |
| $P_{GOOD}$ (yes / no) | yes | yes | yes |
| Over current protection | yes | yes | yes |
| Protection | OVP, OCP, UVP/SCP, OTP, UVLO | OVP, OCP, UVP/SCP, OTP, UVLO | OVP, OCP, UVP/SCP, OTP, UVLO |
| Light load mode | yes | yes | yes |
| Peak efficiency (%) | 96 | 96 | 96 |
| Package type | PowerPAK MLP34-57 | PowerPAK MLP34-57 | PowerPAK MLP34-57 |
| Package size (W, L, H) (mm) | 5.0 x 7.0 x 0.75 | 5.0 x 7.0 x 0.75 | 5.0 x 7.0 x 0.75 |
| Status code | 1 | 1 | 1 |
| Product type | microBUCK | microBUCK | microBUCK |
| Applications | Computer, industrial, networking | Computer, industrial, networking | Computer, industrial, networking |

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