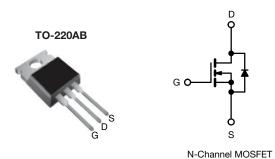


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	80	00		
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	6.5		
Q _g max. (nC)	3	8		
Q _{gs} (nC)	5.0			
Q _{gd} (nC)	2	1		
Configuration	Sin	igle		

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFBE20PbF
Lead (Pb)-free and halogen-free	IRFBE20PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_{\rm C}$	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	800	V		
Gate-source voltage		V_{GS}	± 20	v		
Continuous duein suurent	V -1.40.V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$		1.8		
Continuous drain current	V _{GS} at 10 V	T _C = 100 °C	I _D	1.2	А	
Pulsed drain current ^a			I _{DM}	7.2		
Linear derating factor				0.43	W/°C	
Single pulse avalanche energy b		E _{AS}	180	mJ		
Repetitive avalanche current a		I _{AR}	1.8	А		
Repetitive avalanche energy ^a		E _{AR}	5.4	mJ		
Maximum power dissipation $T_C = 25 ^{\circ}C$		P_{D}	54	W		
Peak diode recovery dV/dt ^c		dV/dt	2.0	V/ns		
Operating junction and storage temperature range	ating junction and storage temperature range T _J , T _{stg} -55 to +150		- °C			
Soldering recommendations (peak temperature) ^d For 10 s				300		
Mounting towns	6.22.0*1	10 00000		10	10 lbf ⋅ in	
Mounting torque	6-32 or M3 screw			1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 104 mH, R_g = 25 Ω , I_{AS} = 1.8 A (see fig. 12)
- c. $I_{SD} \le 1.8$ A, $dI/dt \le 80$ A/ μ s, $V_{DD} \le 600$, $T_{J} \le 150$ °C
- d. 1.6 mm from case

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THERMAL RESISTANCE RAT	INGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	2.3	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$) V, I _D = 250 μA	800	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	0.98	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V$	/ _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _G	$V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
	,	$V_{DS} = 800 \text{ V}, V_{GS} = 0 \text{ V}$		-	-	100	μΑ
Zero gate voltage drain current	I _{DSS}	V _{DS} = 640 V, \	V _{DS} = 640 V, V _{GS} = 0 V, T _J = 125 °C		-	500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	_	-	-	6.5	Ω
Forward transconductance	9 _{fs}	V _{DS} = 10	00 V, I _D = 1.1 A b	0.80	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 V$,		-	530	-	
Output capacitance	C _{oss}	V _I	_{DS} = 25 V,	-	150	-	рF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	90	-	1 .
Total gate charge	Qg		I _D = 1.8 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	38	nC
Gate-source charge	Q _{gs}	V _{GS} = 10 V		-	-	5.0	
Gate-drain charge	Q _{gd}			-	-	21	
Turn-on delay time	t _{d(on)}		1	-	8.2	-	
Rise time	t _r	$V_{DD} = 400 \text{ V}, I_D = 1.8 \text{ A},$ $R_g = 18 \ \Omega, R_D = 230 \ \Omega, \text{ see fig. } 10^{\text{ b}}$		-	17	-	ns
Turn-off delay time	t _{d(off)}			-	58	-	
Fall time	t _f			-	27	-	
Gate input resistance	Rg	f = 1 MHz, open drain		0.6	-	4.2	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	-11
Internal source inductance	L _S			-	7.5	-	- nH
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	1.8	- A
Pulsed diode forward current ^a	I _{SM}			-	-	7.2	
Body diode voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 1.8 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	1.4	V
Body diode reverse recovery time	t _{rr}	T 05 00 1	1 0 A AI/At 100 A/h	-	380	570	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 1.8 \text{A}, dI/dt = 100 \text{A/}\mu\text{s}^{\text{b}}$		-	0.94	1.4	μC
Forward turn-on time	t _{on}	Intrinsic turn	-on time is negligible (turn	-on is do	minated b	by L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

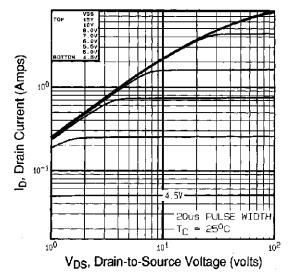


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

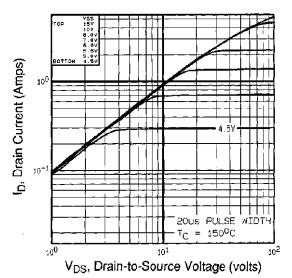


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

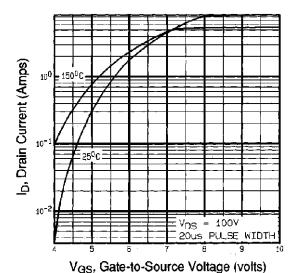


Fig. 3 - Typical Transfer Characteristics

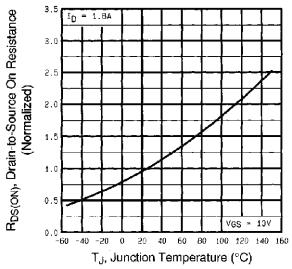


Fig. 4 - Normalized On-Resistance vs. Temperature



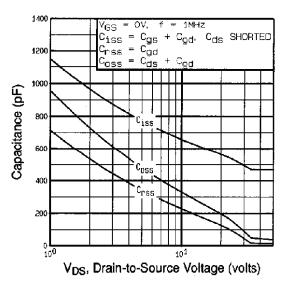


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

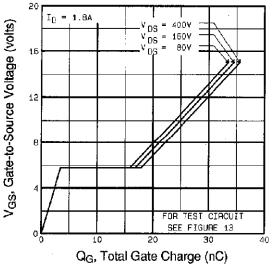


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

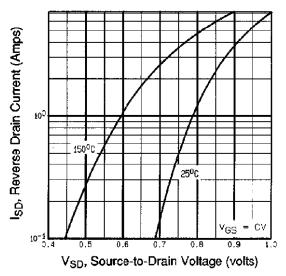


Fig. 7 - Typical Source-Drain Diode Forward Voltage

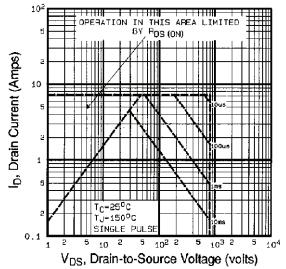


Fig. 8 - Maximum Safe Operating Area



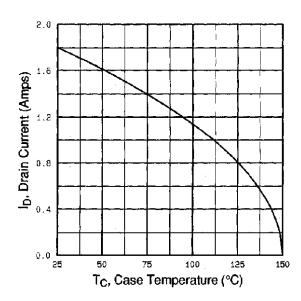


Fig. 9 - Maximum Drain Current vs. Case Temperature

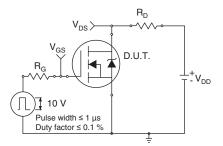


Fig. 10a - Switching Time Test Circuit

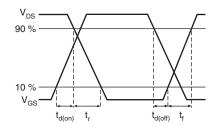


Fig. 10b - Switching Time Waveforms

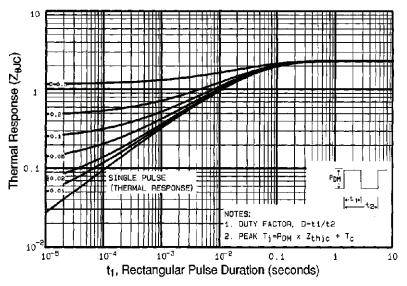


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

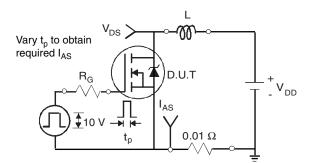


Fig. 12a - Unclamped Inductive Test Circuit

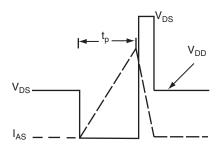


Fig. 12b - Unclamped Inductive Waveforms



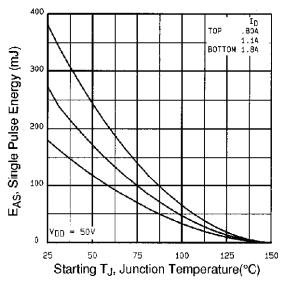


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

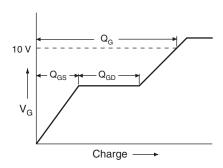


Fig. 13a - Basic Gate Charge Waveform

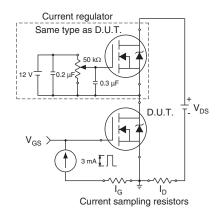
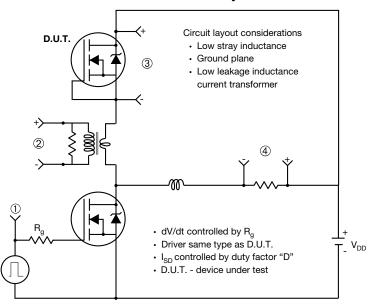


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



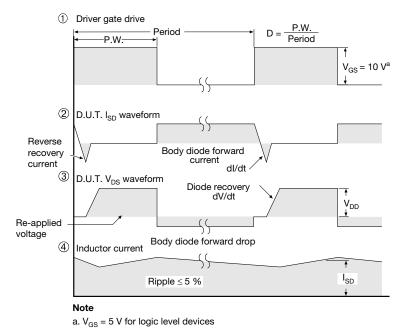


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIM	METERS	INC	HES
	MIN.	MAX.	MIN.	MAX.
Α	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
С	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
Е	9.96	10.52	0.392	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
ØP	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

Note

DWG: 6031

• $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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