Keywords: SerDes, LVDS, Eye Template, Eye Diagram, Serializer, Deserializer, Link performance, Link Margin, Deterministic Jitter, Sinusoid Jitter, Random Jitter, Bit Error Rate, Differential Link

APPLICATION NOTE 4099

Evaluate Serializer-Deserializer (SerDes) Performance by Creating Eye Pattern Templates

Jul 22, 2008

Abstract: Maxim has developed a family of serializer and deserializer products for high-speed, serial data interconnection in video display and digital image sensing. Today's designers are very interested in the performance measurement and margin of a serial data link established by a serializer and deserializer (SerDes) chipset. This application note presents an experimental approach first to measure the eye template of a serial link, then to use that measurement to derive the link performance margin.

Introduction

Maxim's high-speed LVDS serializer and deserializer (SerDes) products have been used in the automotive and telecom industries for video display, image sensing, and data transmissions. When using a SerDes chipset for high-speed data interconnection, the users expect to know the performance of the SerDes link and the margin for reliable data transmission. Designers typically use an eye diagram and an eye template to describe the performance and margin of a serial link.[1,2] There is, however, no clear and convincing methodology for determining the eye template based on experimental data.

This application note presents a systematic approach to determine an eye template from the measured eye diagrams and bit-error rates of the serial link. To illustrate the process, eye templates and link margins for the MAX9217 and MAX9250 SerDes chipset were generated. The system temperatures for the tests were +25°C, +95°C and +105°C, and cables of various lengths were used.

Note: the results obtained from the MAX9250 in this test system also apply to the MAX9248 deserializer. Except for spread-spectrum parallel outputs, the MAX9248 is the same receiving circuit as the MAX9250.

Test Setup

The test setup consists of the following instruments:

- Agilent 86130A Bit Analyzer
- Agilent 83752A Synthesizer Sweeper
- Agilent 70820A Microwave Transition Analyzer
- Agilent 3325A Function Generator

The physical link between the MAX9217 serializer and the MAX9250 deserializer is established through a shielded high-quality cable (Part Number: PT1482) provided by MD Elektronik GmbH,[3] which connects two Rosenberger[4] receptacles (Part Number: D4S20D-40ML5-Y, waterblue) mounted on the transmitter

(MAX9217) and receiver (MAX9250) side of the evaluation board. Website details/links for Rosenberger are available in the References at the end of this application note.

Figure 1 demonstrates the general instrument setup for this test.

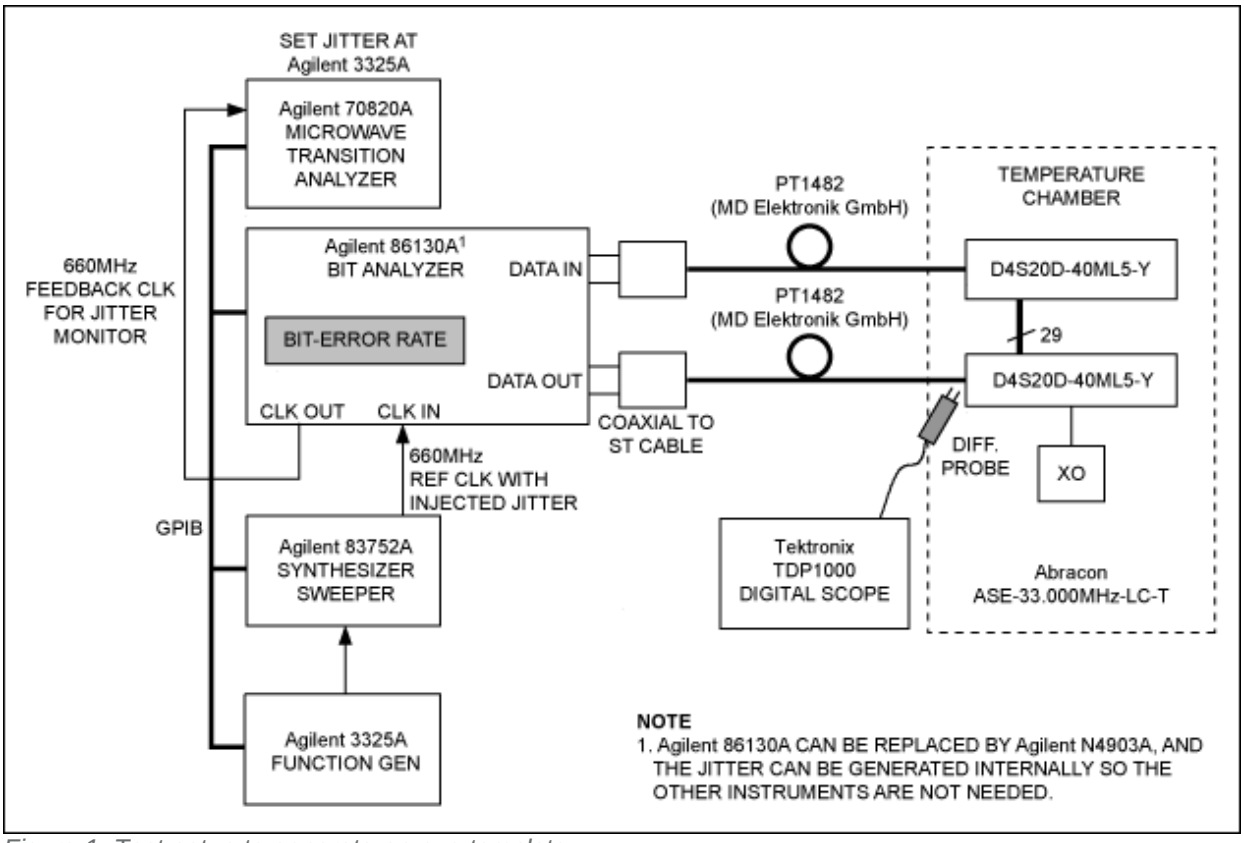

Figure 1. Test setup to generate an eye template.

The bit analyzer generates a serial signal feed to the MAX9250 deserializer, and measures the bit error rate of the serial signal transmitted by the MAX9217. The cable connects the serial output from the bit analyzer and the serial input to the MAX9250. In this test, the cable and connectors are provided by MD Electronik and Rosenberger; all components are specified to meet the stringent requirements of an automotive environment.

Different cable lengths of the PT1482 have been utilized for this test (see **Tables 1** through **3** for test results). The parallel outputs from the MAX9250 are connected to the parallel inputs to the MAX9217. The MAX9217's serial output is connected to the serial input of the bit analyzer. In this configuration, we use the serial bit analyzer to analyze the bit error rate of the SerDes link.

The synthesizer sweeper generates the serial bit clock for the bit analyzer's serial output signal. The microwave transition analyzer controls the function generator to create a sinusoid modulation on the phase of the serial bit clock. The serial bit clock, in turn, inserts the jitter to the serial data transmitted from the bit analyzer. The frequency of the sinusoid modulation is set at 5MHz, which is approximately 10x the loop-filter bandwidth of the MAX9250's receiver PLL. This selection converts the sinusoid modulation into phase jitter to the deserializer, and not a slow-frequency draft that can be tracked by the receiver PLL.

The differential voltage swing of the data output can also be set by the bit analyzer. **Figures 2a** and **2b** show the variations of jitter and voltage swing at the bit analyzer's serial data output.

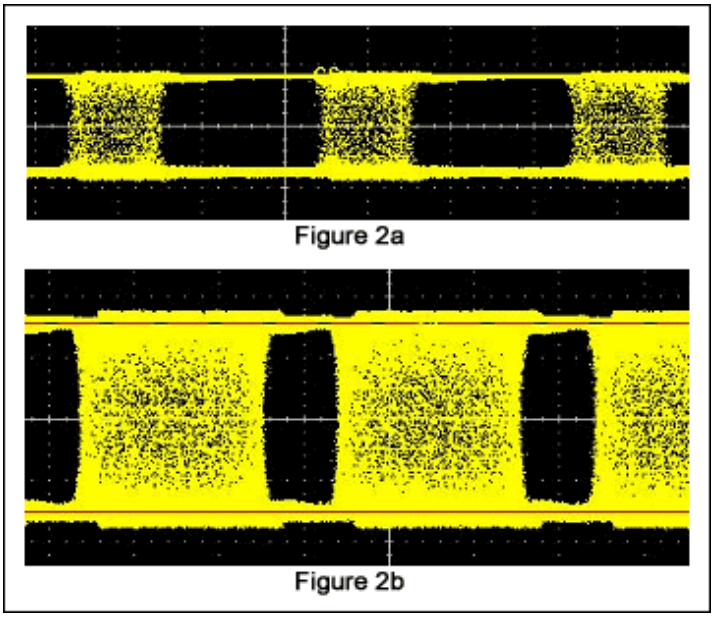

Figure 2. Variation of injected jitter and output swing amplitude. Figure 2a shows bit-analyzer output with injected jitter and reduced swing. Figure 2b shows bit-analyzer output with more injected jitter and normal swing.

Having generated the variable jitter and differential swing, it was time to test the performance of the link. The parallel data rate was fixed at 33Mbps, the serial data rate at 660Mbps. The total jitter inserted into the deserializer input was the sum of the injected sinusoid jitter and the deterministic jitter generated by the limited-frequency bandwidth of the link.

Generating the Eye Template

As a performance measure of a SerDes link, the eye template provides a limit, or a boundary, for the eye diagram measured at the input of the deserializer. When the eye diagram is bigger than the eye template, the deserializer will recover the serial data reliably.

To date, however, there was no well-accepted method for generating such an eye template. The main difficulty has been that the shape of eye template depends on the cable characteristics, signal swing, jitter, and temperature. Consequently, the challenge is to generate a specific eye template under given cable specifications and temperature. It is equally important to somehow decouple the correlation between signal swing and jitter.

To generate the eye template, we started by observing the deserializer eye diagram. When signal "swing" was larger than an observed threshold, jitter principally determined the deserializer's performance. We then did a series of tests on a 5m cable at a 660Mbps serial data rate, and determined the maximum jitter that the deserializer could tolerate for each given signal-amplitude swing. If the deserializer had no error bit for two minutes, we concluded that it tolerated the injected jitter. Statistically, finding no bit error for two minutes is equivalent to saying with 99.9% confidence that the link bit-error rate is less than 10^{-10}. **Figure 3** shows the plot between a given signal swing and the tolerable jitter for +25°C and +95°C, where the tolerable jitter is presented in as UI (Unit Interval). In this case, 1 UI = 1/660MHz = 1.515ns.

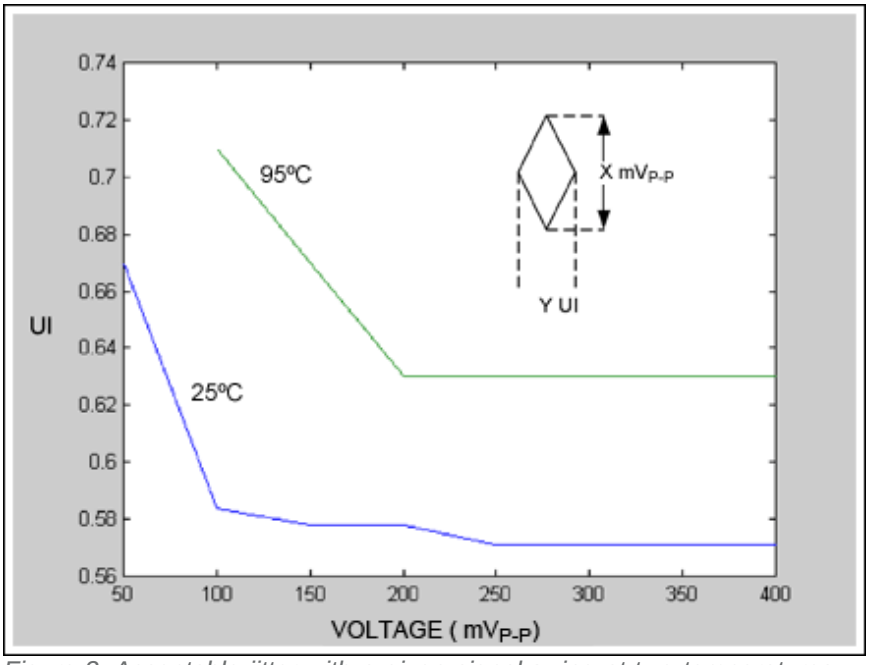

Figure 3. Acceptable jitter with a given signal swing at two temperatures.

The Figure 3 data show that, once the signal swing is larger than a threshold of 100mV$_{P-P}$ at +25°C, the swing minimally affects performance. The same result is observed at +95°C with a threshold value of 200mV$_{P-P}$. Therefore, to measure the eye template, we conservatively fixed the signal swing at 200mV$_{P-P}$, and varied the amount of injected jitter until the link failed. In this manner, we experimentally generate an eye template that guarantees link integrity once the eye diagram is bigger than the template.

Measuring the Eye Template of a Given Link

With the method for generating eye templates defined, we measured the eye templates of given links with different cable lengths and at different temperatures. In the test setup in Figure 1, we adjusted the output amplitude so that the signal swing at the deserializer input was 200mV$_{P-P}$. This adjustment confirmed the eye template's vertical length ("x" in Figure 3) of 200mV$_{P-P}$. We then varied the amount of injected jitter to determine the horizontal length ("y" in Figure 3) of the eye template. The horizontal length is measured with the maximum injected jitter at which the link had no error for two minutes. Table 1 shows the horizontal lengths of the eye templates for various experimental conditions. The unit of the horizontal length is UI.

Table 1. The Horizontal Lengths (UI) of Eye Templates

Test Board No.	0m Cable	5m* Cable PT1482	10m* Cable PT1482
	+25°C	+25°C	+25°C
1	0.597	0.551	0.525
2	0.604	0.578	0.545
3	0.604	0.551	0.525
	+95°C	+95°C	+95°C
1	0.657	0.630	0.597
2	0.644	0.644	0.591

3	0.637	0.624	0.597
	+105°C	**+105°C**	**+105°C**
1	0.663	0.630	0.670
2	0.604	0.611	0.683
3	0.597	0.591	0.637

*Note: For a 5m cable, there is one connector at 2.5m. For a 10m cable, there are three connectors at 2.5m, 5m, and 8m.

Figure 4 shows the eye diagrams obtained from two test cases.

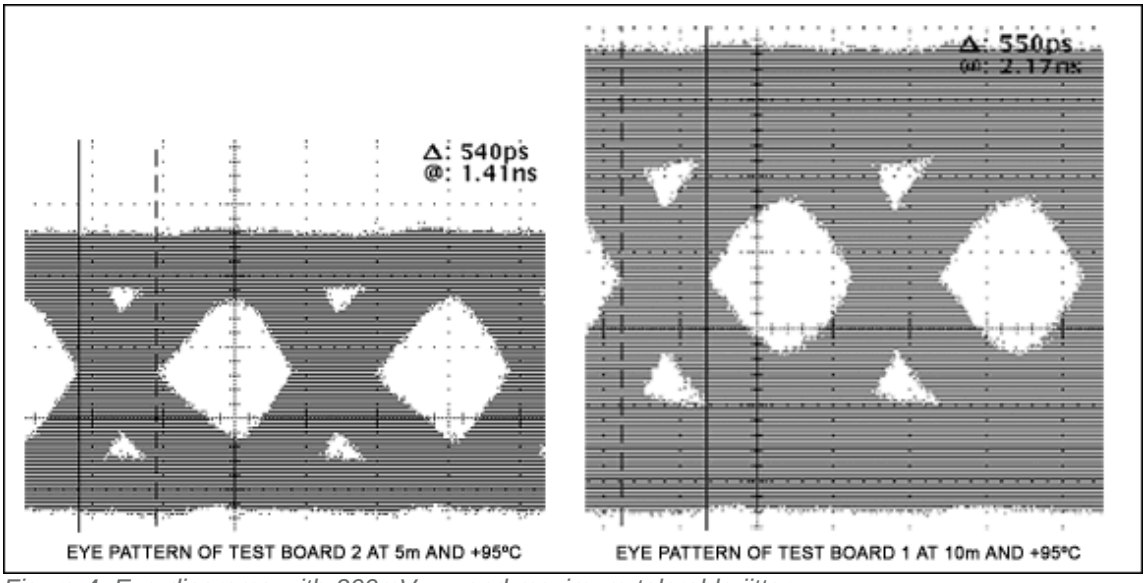

Figure 4. Eye diagrams with 200mV$_{P-P}$ and maximum tolerable jitter.

It should be noted that most scope differential probes cannot sustain the high chamber temperature. We therefore had to measure the eye diagram at the room temperature with the same signal swing and injected jitter. We expected the eye diagrams measured at room temperature to be very similar to those measured at the high temperature. This proved true because the deserializer's input has high impedance and the input pins are terminated by external precision resistors to form the 100Ω differential load that is barely affected by temperature.

Deriving the Link Margin from the Eye Template

It is a straightforward task to derive link margins from the eye templates. The setup in **Figure 5** measures the eye diagrams at the deserializer input with the same cable lengths and temperatures used to generate the templates in Table 1.

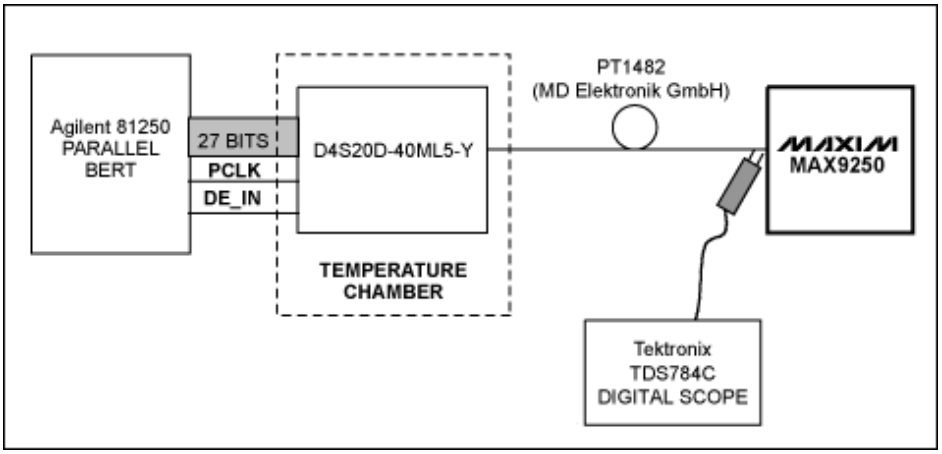

Figure 5. Setup for measuring a link eye diagram.

We put the MAX9250 deserializer outside the temperature chamber to prevent the probe damage from high temperature. **Table 2** shows the two-dimension lengths of the eye diagrams at different cable lengths and temperatures.

Table 2. Measured Link Eye Diagrams

Test Board No.	0m Cable		5m Cable PT1482		10m Cable PT1482	
	Eye Open (Hor., UI)	Eye Open (Ver., mV_{P-P})	Eye Open (Hor., UI)	Eye Open (Ver., mV_{P-P})	Eye Open (Hor., UI)	Eye Open (Ver., mV_{P-P})
	+25°C	+25°C	+25°C	+25°C	+25°C	+25°C
1	0.894	480	0.815	374	0.670	226
2	0.881	464	0.815	372	0.716	236
3	0.894	504	0.809	368	0.696	228
	+95°C	+95°C	+95°C	+95°C	+95°C	+95°C
1			0.815	380	0.710	220
2			0.802	388	0.723	210
3			0.842	404	0.729	248
	+105°C	+105°C	+105°C	+105°C	+105°C	+105°C
1			0.795	376	0.696	204
2			0.782	380	0.716	206
3			0.822	400	0.716	230

Now we can compare the measured eye diagrams in Table 2 with the eye templates in Table 1 to generate the margin for each link. As **Table 3** shows, the margins are calculated in the vertical direction by dB and in the horizontal direction by UI.

Table 3. Link Margins of Different Cable Lengths and Temperatures

Test Board No.	0m Cable		5m Cable PT1482		10m Cable PT1482	
	Eye Margin	Eye Margin	Eye Margin	Eye Margin	Eye Margin	Eye Margin

	(Hor., UI)	(Ver., dB)	(Hor., UI)	(Ver., dB)	(Hor., UI)	(Ver., dB)
	+25°C	+25°C	+25°C	+25°C	+25°C	+25°C
1	0.297	7.6	0.264	5.4	0.145	1.1
2	0.277	7.3	0.238	5.4	0.172	1.4
3	0.290	8.0	0.257	5.3	0.172	1.1
	+95°C	+95°C	+95°C	+95°C	+95°C	+95°C
1			0.185	5.6	0.112	0.8
2			0.158	5.8	0.132	0.4
3			0.218	6.1	0.132	1.9
	+105°C	+105°C	+105°C	+105°C	+105°C	+105°C
1			0.165	5.5	0.026	0.2
2			0.172	5.6	0.033	0.3
3			0.231	6.0	0.079	1.2

To compare the eye template and the eye diagrams graphically, the eye template is drawn inside the eye diagram for two examples, shown in **Figure 6**.

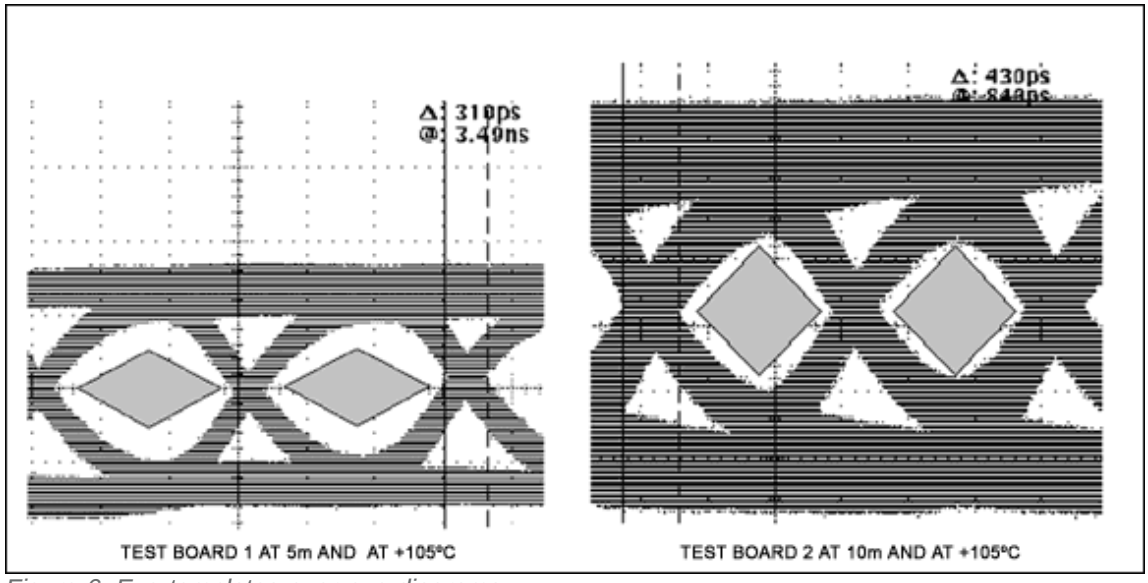

Figure 6. Eye templates over eye diagrams.

The following observations can be made from the data in Table 3.

1. The eye template is a function of multiple factors, such as cable type, length, connector type, temperature, data rate, and chip-to-chip variation.

2. For a 5m cable, the MAX9217/MAX9250 SerDes chipset has enough margins both vertically and horizontally to provide a reliable serial link at the 660Mbps data rate.

3. For a 10m cable, the MAX9217/MAX9250 SerDes chipset has very limited margins in both directions.

4. The eye templates obtained in Test 1 (see Table 1) are relatively conservative for determining the horizontal dimension of the eye template. If the operation is always in room temperature, for example,

the signal swing threshold can be chosen as 100mV$_{P-P}$, and this will result in smaller eye templates and bigger vertical margins.

Summary

This application note presents an experimental approach for generating the eye template of a SerDes chipset. The new approach decouples the signal swing from jitter tolerance by determining the threshold over which the signal swing has insignificant effect on link performance. The technique uses the threshold as the vertical dimension of the eye template, and the maximum tolerable jitter to determine the template's horizontal dimension. Using the resultant eye templates, the link margins from the measured eye diagrams can be determined.

A similar article appeared in the *Test and Measurement World* magazine website on February 12, 2008.

Reference

1. Agilent, Inc., Application Note, "Calibrated Jitter, Jitter Tolerance Test and Jitter Laboratory with the Agilent J-BERT N4903A."
2. Agilent, Inc., White Paper, "Comparison of Different Jitter Analysis Techniques with a Precision Jitter Transmitter."
3. MD Elektronik GmbH, PT1482 cable information.
4. Rosenberger, Inc., Technical Data Sheet for Right Angle PCB Plug, D4S20D-40ML5-Y.

Related Parts		
MAX9217	27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer	Free Samples
MAX9218	27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer	Free Samples
MAX9247	27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Serializer	Free Samples
MAX9248	27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 4099: http://www.maximintegrated.com/an4099
APPLICATION NOTE 4099, AN4099, AN 4099, APP4099, Appnote4099, Appnote 4099