Keywords: TFT display, automotive, serial link, TFT bias, led backlight, power supply, power, analog, switching regulator, buck, boost, step up DC-DC, step down DC-DC, DC-DC, high-voltage, battery powered, LVDS, HDMI, I2C, embedded, software

APPLICATION NOTE 6632

HOW TO DESIGN AN AUTOMOTIVE TFT DISPLAY SYSTEM

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Abstract: Modern cars embed multiple displays, increasing the need for compact display driver system. This application note presents a complete automotive, high-voltage, TFT display system reference design along with test results under automotive operating conditions.

Introduction

This application note guides the reader through the design of a TFT display system for automotive applications. After describing the system architecture, each individual block is analyzed and dimensioned to meet the display specification and automotive constraints. Finally, a reference design PCB is presented along with layout recommendations, embedded software, and test results.

Defining the System Specifications

Figure 1 provides a top-level view of a complete automotive TFT display system. The very first step in designing one is to establish system requirements, such as display power supply needs, display video format, and system input voltage operating range. A good start would be to go through the display data sheet and take note of all requirements concerning power supply rails and video signals. We chose an off-the-shelf 10-inch TFT-LCD display with 1280 x 800 resolution as an example for the system. The display exposes a single low voltage differential signaling (LVDS) port with four channels (24 bits pixel color depth), architecture, and test results.

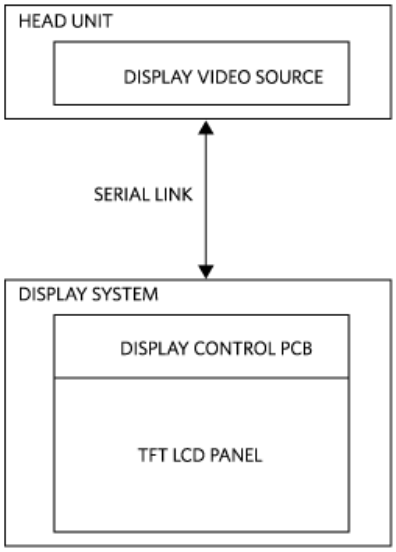

Figure 1. Automotive display system.

Input Voltage Range

Because the display system is intended for automotive applications, it is powered directly from a 12V lead acid battery, so its entire circuitry must be able to withstand common automotive operating conditions. This results in an input voltage operating range that falls between 4.5V and 18V, guaranteeing a fully functional display, even during cold crank events. The system must also survive common automotive faults such as reverse battery connections and 42V Load Dump conditions. To achieve these targets all the circuitry connected directly to the battery voltage must be high-voltage capable, and a Schottky diode connected in series with the main battery connector provides protection against reverse battery faults.

Display Power Supply Requirements

Inspecting the data sheet, it is possible to group the TFT display bias requirements in terms of voltage rail requirements, current demand on each rail, and power-up and power-down sequencing.

The selected display requires a 3.3V logic rail for the LVDS interface plus the usual AVDD, VGON, and VGOFF rails to drive the TFT cells. A VCOM rail for the display backplane is also needed.

Table 1 summarizes all the voltage rails that the display needs to operate correctly.

Table 1. Display Bias Requirements

Voltage Rail		Min	Typ	Max	Unit
Logic Supply Voltage (DIS_VCC)	Voltage	3.0	3.3	3.6	V
	Current	-	56	100	mA
Analog Supply Voltage (AVDD)	Voltage	12.35	13	13.65	V
	Current	-	26	102	mA
Gate On Voltage (VGON)	Voltage	22	23	24	V
	Current	-	0.64	0.9	mA
Gate Off Voltage (VGOFF)	Voltage	-8	-7	-6	V
	Current	-	0.64	0.9	mA
Vcom Voltage (VCOM)	Voltage	4.6	5.1	5.6	V
	Current	-	-	1	mA

Respect the power-up and power-down sequence of the voltage rails to protect the LCD display from exposure to any DC voltage and guarantee reliability. **Figure 2** shows the power-up and power-down sequence that the TFT bias controller must generate.

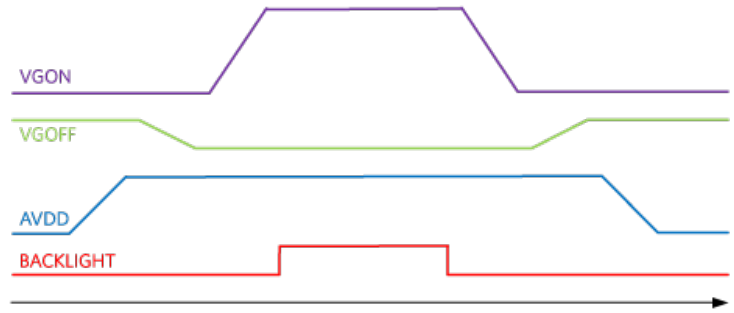

Figure 2. TFT bias sequencing.

The design incorporates the MAX20067 IC as a complete TFT bias solution for automotive applications. The MAX20067 can generate all the voltage rails that the display needs and offers flexible power-up sequencing through an I^2C interface. The MAX20067 is a low-voltage device, so a front-end, high-voltage, step-down regulator is needed. The MAX20003 buck converter supplies a 3.3V regulated rail, using its fixed output 3.3V version. The MAX20003 provides the logic supply for the display (DIS_VCC), the input supply for the TFT bias circuitry (MAX20067), and the power supply for the deserializer.

LED Backlight Requirements

The display's data sheet usually reports the number of LED strings that the backlight system uses, together with the electrical specification of the LED strings. The main parameters of interest are the forward voltage range of the string over temperature and the forward current range of the string. These parameters are used to dimension the backlight DC-DC controller.

In the case of the selected display, the backlight is generated with six strings, each comprising eight LEDs, resulting in the electrical specification reported below.

Table 2. LED Backlight Requirements

Parameter	Min	Typ	Max	Unit
Forward Voltage	21.6	24.24	27.2	V
Forward Current	-	90	100	mA

The design uses the MAX20446 backlight driver IC to drive the display LED strings, offering a built-in boost/single-ended primary-inductor converter (SEPIC) controller that is ideal for automotive applications. The MAX20446 also controls up to six channels (LED strings) through programmable constant current sinks.

Moreover, the MAX20446 includes a feature called internal dimming, which is the ability to set the dimming for each channel through I^2C without requiring an external PWM signal.

Video Signal Requirements

The display has a single-port 4-channel LVDS input that the display system must drive. The display's data sheet states a maximum pixel clock frequency that the LVDS source requires, based on the display resolution, frame rate, and frame synchronization timing. In this case, the maximum frequency is 78MHz, so the LVDS source must be capable of generating a pixel clock frequency of up to 78MHz.

The design includes the MAX9278A as the LVDS source output, because the Gigabit Multimedia Serial Link (GMSL) deserializer is capable of a maximum pixel clock frequency of 104MHz—more than enough for the selected display. The MAX9278A deserializer is paired with the MAX9291 serializer on the Head Unit side. The physical link between the deserializer and serializer is made by a coaxial cable. The MAX9291 serializer exposes an HDMI input that can be connected to a standard HDMI source and an I^2C interface that a general-purpose microcontroller on the Head Unit side can control.

Miscellaneous Features

To reduce EMI and component size, all the switching regulators are designed to operate at 2.2MHz using frequency spread spectrum modulation. The serial link can also be used to carry I^2C commands, enabling MAX20067 and MAX20446 control from the Head Unit side of the link, where the serializer resides.

LED backlight dimming can be also controlled from the Head Unit using the MAX20446 internal dimming feature. Alternatively, the CNTL2 input pin of the MAX9291 serializer can be driven from the Head Unit end. In fact, the CNTL2 signal is carried over the serial link and is reflected on the CNTL2 output pin of the MAX9278A, which is connected to the DIM pin of the MAX20446.

The MAX9278A has also two GPIO pins programmable through I^2C that can be used to drive the MAX20446 enable pin and the enable pin of the display itself, if provided.

The MAX20446 and MAX20067 provide an open-drain fault pin that can be logically ORed by shorting the two fault pins together (and providing a common pull-up resistor).

The MAX9278A and MAX9291 provide a GPI/GPO feature that enables fault-interrupt signaling over the serial ink. Hooking up the fault signal to the MAX9278A GPI, the state of the fault signal itself is reflected on the GPO pin of the MAX9291 at the Head Unit end. This signal can be used as an interrupt source by a Head Unit microcontroller.

The entire system can be placed in Sleep mode, reducing overall power consumption. This can be achieved by disabling the MAX20446 through the MAX9278A GPIO, disabling the MAX20067 through the I^2C interface, and configuring the MAX9278A in Sleep mode.

Figure 3 illustrates the system architecture after identifying all the components needed to achieve the established requirements.

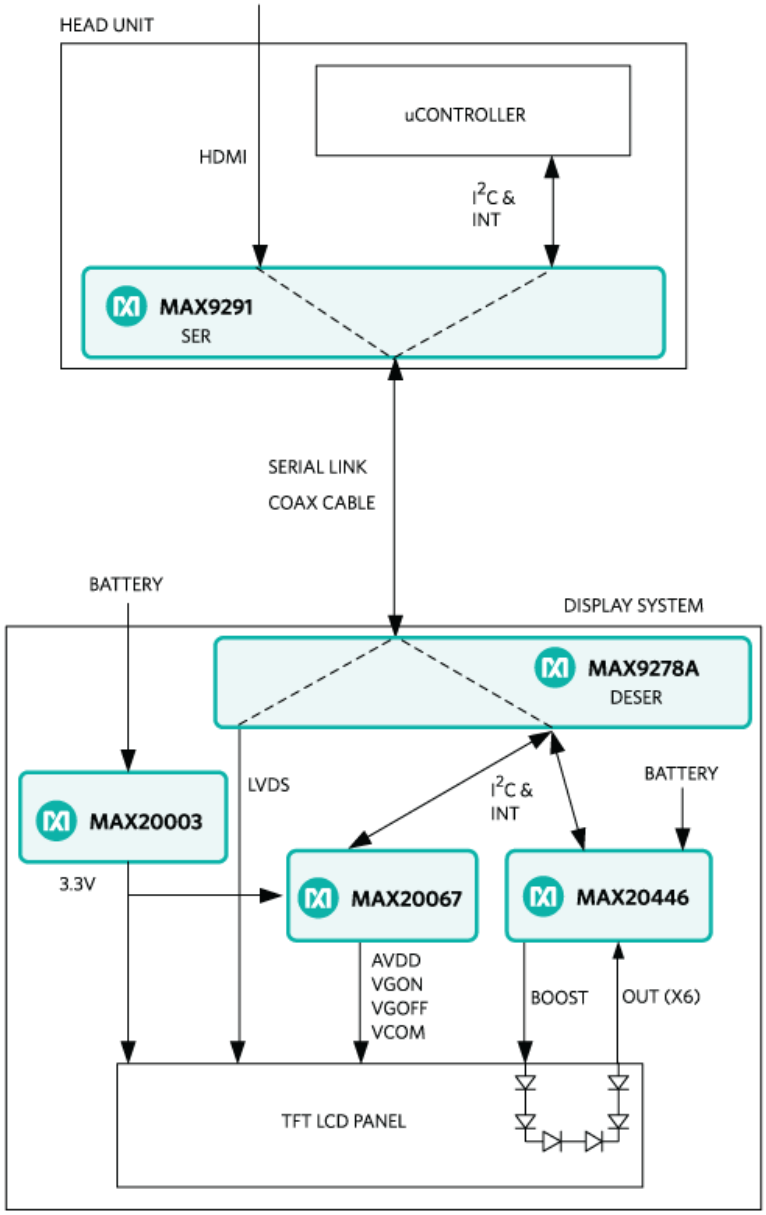

Figure 3. System block diagram.

Front-End Step-Down Regulator Design

The design incorporates the MAX20003 as a front-end high-voltage step-down converter, providing fixed output voltage of 3.3V (MAX20003ATPB/V+). To size the external components of the MAX20003 buck controller, estimate the maximum current that the 3.3V rail needs, which must supply the MAX9278A deserializer, the MAX20067 TFT bias, and the display itself. The MAX9278A deserializer and display total current are stated in the respective data sheet; TFT bias current demand, on the other hand, must be estimated.

The MAX20067 boost circuitry must provide the supply to all TFT bias rails (AVDD, VGON, VGOFF, VCOM). The total output power of the boost can be estimated with the following formulas:

$$I_{OUT\_BOOST\_BIAS} = (I_{AVDD} + I_{VCOM} + (3 \times I_{VGON}) + (2 \times I_{VGOFF}) \cong 107mA$$

$$POUT_{BOOST\ BIAS} = V_{AVDD} \times I_{BOOST\ BIAS} \cong 1.4W$$

assuming a two-stage charge pump for either VGON and VGOFF rail.

Referring to the typical operating conditions listed in the MAX20067 data sheet, the boost efficiency, under this particular load condition, is estimated to be approximately 82% (η). Therefore, the TFT bias circuitry current demand can be calculated as follows:

$$I_{IN\_BOOST\_BIAS} \frac{P_{OUT}}{\eta \times V_{IN\ BOOST\ BIAS}} \cong 520mA$$

With this result, it is possible to accurately estimate the output current of the MAX20003 step-down converter as follows:

$$I_{OUT\_BUCK} = I_{IN\_BOOST\_BIAS} + I_{MAX9278A} + I_{DISPLAY} = 520mA + 294mA + 100mA \cong 920mA$$

Table 3 summarizes the operating condition of the MAX20003, considering a 20% margin on the estimated output current needed for the 3.3V rail:

Table 3. MAX20003 Operating Condition

Parameter	Min	Typ	Max	Unit
Input Voltage Range	4.5	12	18	V
Output Current Range	-	920	1100	mA
Switching Frequency		2200		kHz
Allowed Input Voltage Ripple			50	mV
Allowed Output voltage ripple			10	mV

The inductor can be sized defining a target ratio of the inductor peak-to-peak AC current to the average DC current (output current of the buck). This parameter is called the inductor current ripple ratio, or LIR. A 0.5 LIR is set as the target, being a good compromise between efficiency and size. Once the target LIR has been established, it is possible to estimate the required minimum inductance value, as follows:

$$L_{MIN} = \frac{(V_{BATT} - V_{OUT\ BUCK}) \times D}{F_{SW} \times I_{OUTBUCK} \times LIR} \cong 2\mu H$$

$$V_{OUT\ BUCK} + 3.3V$$

where D is the duty cycle, as follows:

$$D = \frac{V_{OUTBUCK}}{V_{BATT}} \cong 0.275$$

The design includes a 2.2µH inductor with a saturation current and rated current higher than the forecast buck converter maximum output current. The inductor peak-to-peak AC current is equal to the following:

$$I_{BUCK\ PP} = \frac{(V_{BATT} - V_{OUT\ BUCK}) \times D}{L \times F_{SW}} \cong 0.5A$$

Assuming a 50mV maximum input voltage ripple across the input capacitor, and to divide equally the ripple contribution between the equivalent series resistance (ESR) and the capacitance of the input capacitor, the minimum ESR and capacitance can be defined.

To keep charge balance at steady state, at every PWM cycle the input capacitor is charged and discharged the same charge amount, so the voltage drop due to the capacitance can be estimated during either the off or on time.

During the off time the input capacitor is charged with the entire buck input current, so to limit the voltage increase to less than 25mV, the input capacitance must be higher than the following:

$$C_{IN\ BUCK\ MIN)} = \frac{I_{IN\ BUCK} \times (1 - D)}{25mV \times F_{SW}} \cong 4\mu F$$

where the input current of the buck is equal to the following:

$$I_{IN\_BUCK} = I_{OUT\_BUCK} \times D$$

At the end of the on time, the current provided by the input capacitor reaches its peak, with the highest drop across the ESR. An estimate of this current peak can be used to determine the maximum allowed capacitor ESR as follows:

$$ESR_{IN\_BUCK\_MAX} = \frac{25mV}{(I_{OUT\ BUCK} - I_{IN\ BUCK}) + \frac{I_{BUCK\ PP}}{2}} \cong 24m\Omega$$

The design uses the Murata GRM32ER71H475KA88 4.7µF capacitor, having 4.4µF effective capacitance at 12V DC bias and 3m½ ESR at 2.2MHz.

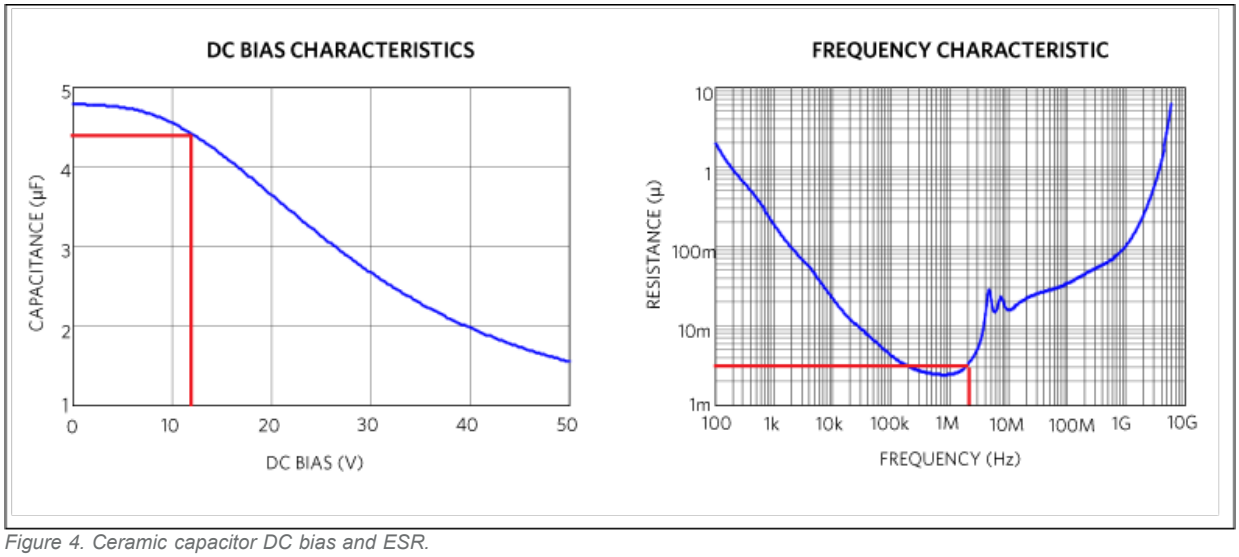

Figure 4. Ceramic capacitor DC bias and ESR.

Assuming we use an output capacitor with high capacitance, the capacitor ESR dominates the voltage ripple on the output. The output capacitor experiences the maximum current while the regulator is transitioning from the full-load condition to the no-load condition, imposing a maximum ESR value given a target maximum voltage ripple.

$$ESR_{OUT\ BUCK\ MAX} = \frac{10mV}{I_{OUT\ BUCK} + \frac{I_{LPP}}{2}} \cong 7m\Omega$$

The design uses the Murata GRM32ER71A226K for output capacitors, which has an ESR of 5m½ at 2.2MHz. As an extra safe margin, two of these capacitors have been placed in parallel, reducing the overall ESR to 2.5m½.

Refer to the MAX20003 data sheet for information regarding compensation components selection.

Switching frequency is set through the external resistor between the FOSC pin and ground. A 12.1k resistor has been selected to operate the converter at 2.2MHz.

The SPS pin is connected to BIAS, enabling the spread spectrum feature.

The FSYNC pin is connected to ground, enabling Skip mode operation and reducing even further the system sleep current.

TFT Display Bias Design

The boost converter is the first section to dimension for the MAX20067 circuitry. The boost converter must directly regulate the AVDD rail and provide input supply for VCOM, VGON, and VGOFF regulators.

MAX20067 Boost Design

Like the MAX20003 converter, the inductor targets a 0.5 LIR, but with the following difference: being a boost converter, the average inductor current is equal to the input current of the converter ($I_{IN\ BOOST\ BIAS}$).

$$L_{MIN} = \frac{V_{BUCK\ OUT} \times D}{F_{SW} \times I_{IN\_BOOST\_BIAS} \times LIR} \cong 4.4\mu H$$

where D is the duty cycle:

$$D = 1 - \left(\frac{V_{BUCK\ OUT}}{V_{AVDD}}\right) \cong 0.75$$

$$V_{AVDD} = 13V$$

A 10µH inductor with saturation current and rated current higher than I_(IN_BOOST_BIAS) has been selected. The inductor peak-to-peak AC current is equal to the following:

$$I_{BOOST\_BIAS\_PP} = \frac{V_{BUCK\ OUT} \times D}{L \times F_{SW}} \cong 112mA$$

According to the display specification, the AVDD rails must be 13V ±5%, the MAX20067 boost accuracy is 2%, and using a feedback resistor divider with 1% tolerance adds another error equal to the following:

$$E_{EXT\_RES\_\%} = 2 \times TOL_{EXT\_RES} \times \left(1 - \frac{V_{REF\ BIAS}}{V_{AVDD}}\right) \cong 1.8\%$$

$$V_{REF\ BIAS} = 1.25V$$

This leads to a total accuracy of 3.8%, which leaves 1.2% (156mV) of room for the voltage ripple on the output capacitor.

Allowing a 15mV maximum output voltage ripple across the output capacitor and equally dividing the ripple contribution between the ESR and capacitance of the output capacitor defines the minimum ESR and capacitance needed.

To keep charge balance at steady state, during every PWM cycle the output capacitor is charged and discharged the same charge amount, so the voltage drop due to the capacitance can be estimated during either the off time or on time.

During the on time, the output capacitor is discharged with the entire boost output current, so to drop the output voltage less than

7.5mV the output capacitance must be higher than the following:

$$C_{OUT\_BOOST\_BIAS\_MIN} = \frac{\left(I_{OUT\ BOOST\ BIAS}\right) \times (D)}{75mV \times F_{SW}} \cong 0.5\mu F$$

At the beginning of the off time, the current provided by the output capacitor reaches its peak, with the highest drop across the ESR. Estimating this current peak can be used to determine the maximum capacitor ESR allowed:

$$ESR_{OUT\_BOOST\_MAX} = \frac{75mV}{\left(I_{IN\ BOOST\ BIAS} - I_{OUT\ BOOST\ BIAS}\right) + \frac{I_{BOOST\ BIAS\ PP}}{2}} \cong 150m\Omega$$

The design incorporates a combination of the Murata GRM31CR71E106KA12 10µF capacitor on the HVINP pin and the Murata GRM21BR61H475KE51 4.7µF capacitor on the AVDD pin, resulting in a 5µF effective capacitance at 13V bias and 2.5m½ ESR at 2.2MHz.

Assuming the use of an input capacitor with high capacitance, the capacitor ESR dominates the voltage ripple on the input. The input capacitor experiences the maximum current while the regulator is transitioning from the no-load condition to a full-load condition, imposing a maximum ESR value given a target maximum voltage ripple—assumed to be 10mV.

$$ESR_{IN\ BOOST\ MAX} = \frac{10mV}{I_{IN\ BOOST\ BIAS} + \frac{I_{BOOST\ BIAS\ PP}}{2}} \cong 17m\Omega$$

The design incorporates the Murata GRM32ER71A226K output capacitor, which has an ESR of 5m½ at 2.2MHz. Two of these capacitors are placed in parallel to add an extra safe margin, reducing the overall ESR to 2.5m½.

By default, the MAX20067 switching frequency is set to 2.2MHz with spread spectrum enabled.

MAX20067 VCOM Buffer

The AVDD rail supplies the MAX20067 VCOM buffer, with the default VCOM output value V_{AVDD}/ 2. To set the typical VCOM voltage required by the display data sheet, it is necessary to bias the VCOM buffer positive input (VCINH) to the desired VCOM voltage through a resistor divider between AVDD, VCINH, and ground. The resistor divider is composed of R8 and R9 (10k½ and 15.8k½, respectively) resulting in a VCOM default voltage of 5.04V. The VCOM voltage can be further adjusted through I^2C with steps of 19.5mV.

MAX20067 Charge Pumps Design

The VGON and VGOFF rails are both generated with charge pumps, and the number of stages needed for each rail is specified by the following formulas:

$$N_{STAGES\ VGON\ CP} \geq (V_{VGON} - V_{AVDD} + 0.6V) \times (V_{AVDD} - 2 \times V_{DIODE}) \geq 0.92$$

$$N_{STAGES\ VGOFF\ CP} \geq (-V_{VGOFF} + 0.6V) \times (V_{AVDD} - 2 \times V_{DIODE}) \geq 0.65$$

assuming the use of normal diodes for both charge pumps.

The design incorporates two-stage charge pumps to make the design more flexible, even if single-stage charge pumps would be sufficient.

According to the display specification, the VGON rail must be 23V±4.3% and VGOFF rail must be -7V±14%. The MAX20067 charge pump accuracy is 2%. Using a feedback resistor divider with 1% tolerance adds another error equal to the following:

$$E_{EXT\_RES\_\%} = 2 \times TOL_{EXT\ RES} \times \left(1 - \frac{V_{REF\ POS\ CP}}{V_{VGON}}\right) \cong 1.9\%$$

This leads to a total accuracy of 3.9%, which leaves 0.4% (92mV) room for the voltage ripple on the output capacitor for the positive charge pump. The negative charge pump instead has plenty of margin.

The charge pump control scheme is based on a simple skipping strategy; when the output of the charge pump is below the reference, a PWM pulse with 50% duty cycle is generated at 440kHz. Using a ceramic capacitor on the output of the charge pumps the voltage ripple is dominated by the capacitor discharge during the 50% duty cycle on time. Considering this last point and targeting a voltage ripple of 50mV, the minimum value for the output capacitance is set by the following equation:

$$C_{OUT\ VGON\ MIN} = \frac{\left(I_{VGON}\right) \times (0.5)}{50mV \times 440kHz} \cong 0.23\mu F$$

The design uses a Murata GRM188R61H225KE11 2.2µF capacitor, resulting in a 0.36µF effective capacitance at 23V DC bias.

The same capacitor has been used for the VGOFF charge pump, amply respecting the output voltage accuracy requirement and optimizing the system BOM at the same time.

MAX20067 Programming

The MAX20067 can be used in Stand Alone mode or I^2C mode. When used in I^2C mode, the device behavior is regulated through I^2C register settings. I^2C mode is selected by connecting the MAX20067 SEQ pin to ground.

The MAX20067 provides an autosequencing feature that enables all the rails following a fixed power-up sequence. The feature can be enabled by setting the EN_AUTOSEQ bit in the CONFIGURATIONS register.

Programming the AUTO_SEQUENCING_CTRL1/2 registers, it is possible to set the power-up and power-down sequence and timing for the AVDD, VCOM, VGON, and VGOFF rails.

By default, the VCOM rail powers up simultaneously with the AVDD rail as also required by the display used in this design. It is always possible to control VCOM independently, enabling the rail through I^2C and creating a custom power-up sequence through software if needed.

The AUTOSEQ_ROW1/2/3 bit fields must be set to power on AVDD rail first, then VGL, and finally VGH:

- AUTOSEQ_ROW_1 = 0b001 (AVDD)
- AUTOSEQ_ROW_2 = 0b100 (VGON)
- AUTOSEQ_ROW_3 = 0b010 (VGOFF)

The power-up and power-down sequences can be triggered by respectively setting or clearing the AUTOSEQ_CTRL bit in the REGULATOR_CONTROL register.

After the power-down sequence has been executed, the MAX20067 automatically enters Shutdown mode, reducing power consumption to its minimum.

LED Backlight Driver Design

The MAX200446 supplies the LED strings directly from the battery voltage and can be used in boost or SEPIC configurations, depending on the ranges of the forward LED strings voltage and input voltage.

In this case, the input voltage (4.5V to 18V) is always lower than the LED string forward voltage (21.6V to 27.2V), so a boost configuration has been selected.

MAX20446 Boost Design

The MAX20446 features an adaptive scheme that regulates the output of the boost converter so that the voltages on all the enabled OUT pins are in a range between 0.7V and 1.1V. This allows enough headroom to control the string current but at the same time reduces power dissipation.

Table 4 summarize the operating conditions of the MAX20446 boost regulator.

Table 4. MAX20446 Operating Conditions

Parameter	Min	Typ	Max	Unit
Input Voltage Range	4.5	12	18	V
Output Voltage Range (LED String Forward Voltage + OUT Headroom)	22.2	25.14	28.3	V
Output Current Range (6x LED String Current)		500	600	mA
Switching Frequency		2200		kHz
Allowed Input Voltage Ripple			50	mV
Allowed Output voltage ripple			50	mV

The current mode boost voltage feedback is derived through a resistor divider connected to the BSTMON pin, which is regulated in a voltage range between 0.6V and 1.23V, depending on the required boost output voltage. In case of an open LED string fault, the control loop raises the output voltage until the BSTMON pin reaches the 1.23V threshold. This triggers the open LED fault, which in turn disables that specific channel.

The BSTMON resistor divider, therefore, must be chosen to trigger the open string fault with a boost output voltage ($V_{OUT\ BSTMON}$) higher than the maximum boost output operating voltage. Taking a 10% margin, the $V_{OUT\ BSTMON}$ must be higher than 31.1V. At the same time the BSTMON resistor divider should guarantee a feedback voltage higher than 0.6V when the boost output voltage is at its minimum operating range, which is achieved by limiting $V_{OUT\ BSTMON}$ to be lower than two times the minimum boost output voltage (44.4V).

$$31.1V < V_{OUT\ BSTMON} < 44.4V$$

Selecting R35 and R34 to be 10k and 270k, respectively, $V_{OUT\ BSTMON}$ is dimensioned to 34.4V. The boost regulator input current, under typical operating conditions, can be estimated with the following formula, assuming an overall efficiency of 85%.

$$I_{IN\ BOOST\ LED\_TYP} = \frac{I_{LEDTYP} \times V_{OUT\ BOOST\ TYP}}{\lambda \times V_{BATT\ TYP}} \cong 1.33A$$

Like with the MAX20067 boost, the required inductor is dimensioned targeting a 0.5 LIR, as follows:

$$L_{MIN} \quad \frac{V_{BATT\ TYP} \times D}{F_{SW} \times I_{IN\ BOOST\ LED\ TYP} \times LIR} \cong 4.26\mu H$$

where D is the duty cycle:

$$D = 1 - \left(\frac{V_{BATT\_TYP}}{V_{OUT\ BOOST\ TYP}}\right) \cong 0.52$$

The inductor carries maximum current during a cold crank event, when the input voltage is at its minimum, resulting in an inductor average current as follows:

$$I_{IN\_BOOST\_LED\_MAX} = \frac{I_{LED\ MAX} \times V_{OUT\ BOOST\ MAX}}{\eta \times V_{BATT\ MIN}} \cong 4.4A$$

The design uses a Coilcraft MSS1246T-472ML 4.7µH inductor, considering its maximum rated current of 6A. The selected inductor determines the current peak-to-peak value:

$$I_{BOOST\ LED\ TYP\ PP} = \frac{V_{BATT\ TYP} \times D}{L \times F_{SW}} \cong 603mA$$

The MAX20446 has similar considerations to the MAX20067 boost regarding the input and output capacitors:

$$C_{OUT\ BOOST\ LED\ MIN} = \frac{I_{LED\ TYP} \times D}{25mV \times F_{SW}} \cong 51\mu F$$

$$ESR_{OUT\_BOOST\_LED\_MAX} = \frac{25mV}{\left(I_{IN\ BOOST\ LED\ TYP} - I_{LED\ TYP}\right) + \frac{I_{BOOST\ LED\ TYP\ PP}}{2}} \cong 23m\Omega$$

$$ESR_{IN\_BOOST\_LED\_TYP} = \frac{50mV}{I_{IN\ BOOST\ LED\ TYP} + \frac{I_{BOOST\ LED\ TYP\ PP}}{2}} \cong 30m\Omega$$

To achieve these requirements a combination of low ESR ceramic capacitors (GRM32ER71H475KA88K 4.7µF) and an electrolytic capacitor (47µF) is used as an output capacitor tank to provide a high-enough capacitance, even with 28.3V DC bias, while keeping the ESR under the estimated limit.

Refer to the MAX20446 data sheet for information regarding compensation components selection. Switching frequency is set through an external resistor between the RT pin and ground. The design uses the Venkel 13.3k resistor at R36 to operate the converter at 2.2MHz.

The spread spectrum feature is enabled by default on the MAX20446.

The EN pin is connected to the MAX9278A GPIO1 pin, enabling remote shutdown of the MAX20446.

MAX20446 Programming

The LED string regulated current can be set through the ISET bit field in the ISET register. For the selected display, the current must be set to 90mA (0b1001); the phase-shift feature is enabled by default, reducing the output current ripple.

As discussed previously, the design uses the internal dimming feature of the MAX20446, enabling remote dimming of the LED strings. The internal dimming PWM frequency can be set by configuring the FPWM bitfield in the SETTING register.

Each individual channel has its own register set to configure the on time, which is represented on 18 bits with a bit weight of 50ns. As an example, channel 1 uses the TONH1 register for the first eight MSBs, the TONL1 register for the second eight MSBs, and the PWM1 bitfield in the TON1-4LSB register for the last two LSBs.

Assuming the use of a 203Hz internal dimming frequency (FPWM 0b001), the equivalent period is 49.261ms, corresponding to 98,522 slots of 50ns. In the case of a 50% dimming duty cycle, 98,522/2 slots of 50ns should be selected, which is equal to 0xC06D. Representing this last number in 18 bits and assigning the corresponding bitfield to the TON_ registers, the following registers assignments are obtained: TONH1 = 0x30, TONL1 = 0x1B, TON1-4LSB.PWM1 = 0b01.

Finally, to enable internal dimming and start driving the LEDs, the DIM_EXT bit must be cleared and the ENA bit must be set.

MAX9278A Deserializer Design

As discussed earlier, the MAX9278A is powered directly from the 3.3V rail, although a dedicated PI filter stage has been added for each specific MAX9278A power supply rail (AVDD, DVDD, and IOVDD).

MAX9278A Serial Link Configuration

The MAX9278A deserializer works in tandem with the Head Unit serializer, so many of the settings of the MAX9278A must be replicated on the serializer side.

As shown in the block diagram (Figure 1) a coaxial cable between the display and the Head Unit is the physical link to transport the video signal, I^2C commands and fault status. To configure the link with these settings, the MAX9278A CX/TP pin and I2CSEL pin must be pulled high and the MS pin pulled low.

The serial link is set to operate in 32-bit mode with high data rate, enabling a pixel clock up to 78MHz and a pixel color depth of 24 bits (BWS is pulled high and DRS is pulled low).

MAX9278A Programming

The default configuration of the MAX9278A is fine for this application. When data over the coaxial cable is detected, the deserializer can establish two types of links with the serializer: a configuration link that only enables I^2C bridge functionality or a complete serial link that carries both I^2C and the video signal over the coaxial cable. It is possible to configure the deserializer in Sleep mode, reducing its own power consumption by setting the SLEEP bit through the configuration or serial link.

The serializer can wake up the deserializer by sending an enable link command over the coaxial cable.

PCB Design and Testing

Figure 5 shows a reference four-layer PCB, 10cm × 10cm, which has been built and tested against all operating conditions. This section presents general layout recommendations, software architecture, and test results.

Figure 5. Reference PCB.

Layout Recommendations

As a general procedure, the switching converter AC current loops should be kept as short and compact as possible.

Placing all power components on the top and having a solid ground plane directly underneath on inner layer two can ease this task. Use inner three layer and the bottom layer for general routing.

MAX9278A circuitry is kept away from power circuitry. Serial data line and LVDS lines have been impedance-matched as detailed in the data sheet. Differential pairs of LVDS lines have been routed constraining the maximum track length difference to route all the pairs with similar trace length.

For specific IC layout recommendations refer to the respective data sheets.

Software Architecture

Once the system is powered up and the serializer on the Head Unit side is powered as well, a configuration link can be established enabling MAX9278A programming.

After properly configuring the MAX9278A, the Head Unit side microcontroller configures the MAX20067 and MAX20446 in Shutdown mode and sends a Sleep command to the deserializer, reducing the system power consumption to its minimum. When the user commands a power-up action, the Head Unit side microcontroller wakes up the deserializer and starts configuring the MAX20067 and MAX20046. A serial link is also established, enabling video data to be transferred over the coaxial cable.

A power-up sequence is initiated after the configuration stage, first enabling the MAX20067 rails and then the MAX20446 backlight driver. After the power-up sequence the video data is displayed on the screen.

While the display is turned on, the Head Unit side microcontroller polls the GPO serializer pin, which reflects the global fault pin of the display system. If at any time the GPO pin reads low, meaning there's a fault on the display side, the microcontroller acquires all the fault registers of the MAX20067 and MAX20446 to track down the source of the fault.

When the user triggers a Power Down command, a series of actions similar to the power-up sequence is executed but in reverse order. After the power-down is complete, the Head Unit side microcontroller configures the MAX20067 and MAX20446 in Shutdown mode and sends a Sleep command to the deserializer, reducing the system power consumption to its minimum.

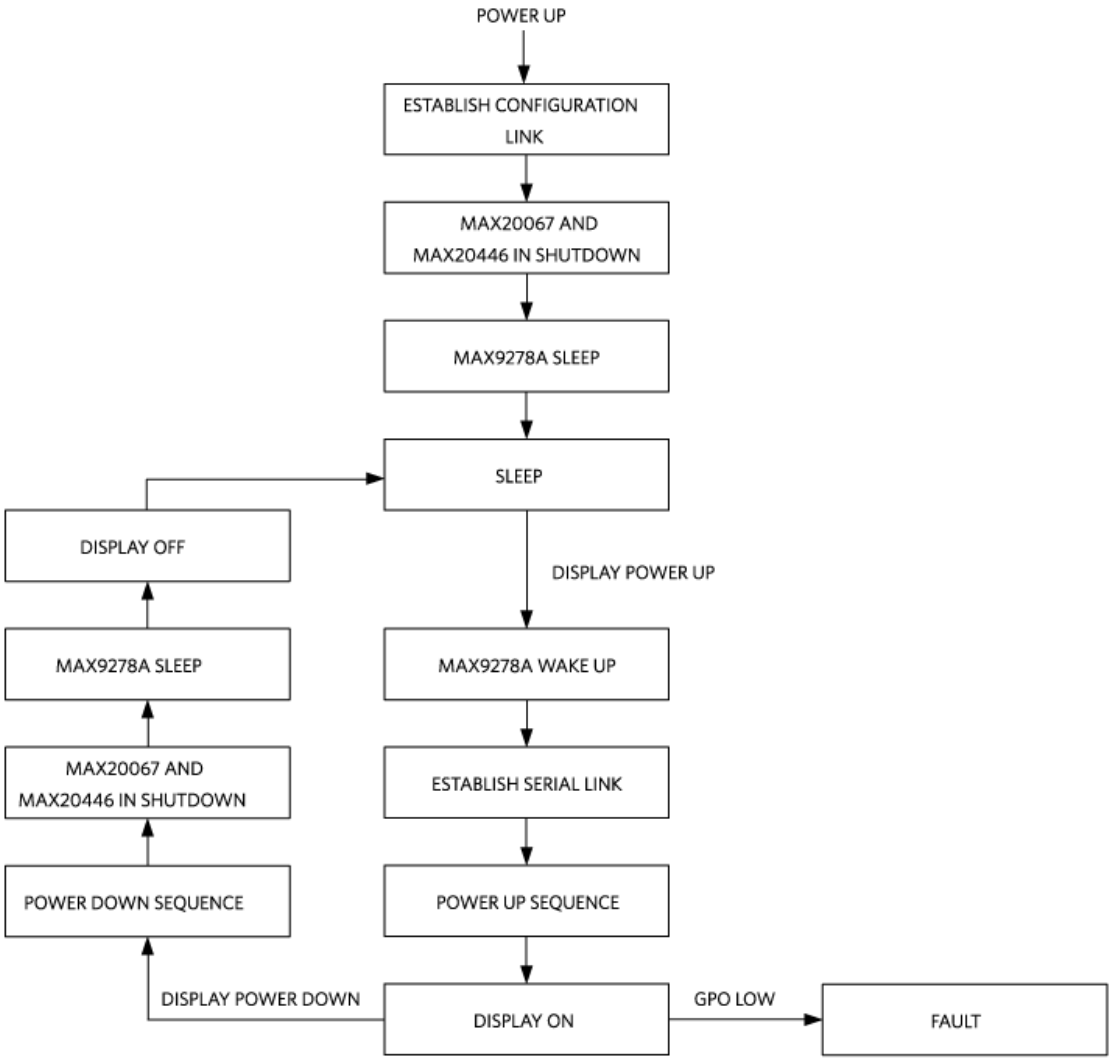

Figure 6. Software flowchart.

Design Resources

Download the complete set of Design Resources including schematics, bill of materials, and to the following files attached to this data sheet for component information, schematic, PCB layout, and test files:

All Design Files

Download All Design Files

Hardware Files:
Schematic
Bill of Materials (BOM)
PCB Layout
Test Results

Related Parts		
MAX20003	36V, 220kHz to 2.2MHz, 2A/3A Fully Integrated Step-Down Converters with 15µA Operating Current	Free Samples
MAX20067	Automotive 3-Channel Display Bias IC with VCOM Buffer, Level Shifter, and I^2C Interface	Free Samples
MAX20446	Automotive 6-Channel Backlight Driver with Boost/SEPIC Controller and I^2C Interface	Free Samples
MAX9278A	3.12Gbps GMSL Deserializers for Coax or STP Input and LVDS Output	Free Samples
MAX9291	3.12Gbps GMSL Serializer for Coax or STP Output and HDMI Input	Free Samples

More Information
For Technical Support: https://www.maximintegrated.com/en/support
For Samples: https://www.maximintegrated.com/en/samples
Other Questions and Comments: https://www.maximintegrated.com/en/contact

Application Note 6632: https://www.maximintegrated.com/en/an6632
APPLICATION NOTE 6632, AN6632, AN 6632, APP6632, Appnote6632, Appnote 6632
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