MOSFET – Power, N-Channel, UltraFET

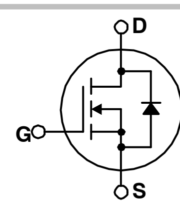
55 V, 75 A, 7 mΩ

HUF75345G3, HUF75345P3, HUF75345S3S

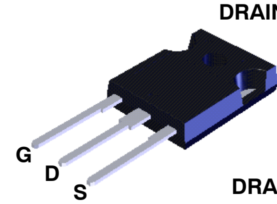
ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
55 V	7 mΩ	75 A

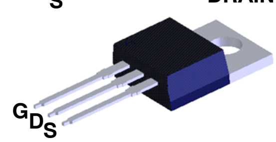


DRAIN (TAB)



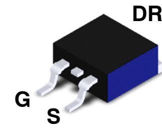
TO–247–3
CASE 340CK

DRAIN (FLANGE)



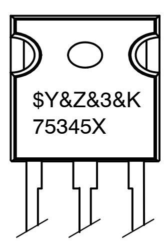
TO–220–3
CASE 340AT

DRAIN (FLANGE)



D2PAK–3
CASE 418AJ

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
75345X	= Specific Device Code X = G/P/S

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

These N–Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on–resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low–voltage bus switches, and power management in portable and battery–operated products.

Features

- 75 A, 55 V
- Simulation Models
  – Temperature Compensated PSPICE™ and SABER® Models
  – Thermal Impedance SPICE and SABER Models
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- These Devices are Pb−Free

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Package	Brand
HUF75345G3	TO−247−3	75345G
HUF75345P3	TO−220−3	75345P
HUF75345S3ST	D2PAK−3	75345S

MOSFET MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage (Note 1)		55	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20 kΩ) (Note 1)		55	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	− Continuous (Figure 2)	75	A
I_{DM}	Drain Current	− Pulsed	Figure 4	
E_{AS}	Pulsed Avalanche Rating		Figure 6	
P_D	Power Dissipation	(T_C = 25°C)	325	W
		− Derate Above 25°C	2.17	W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to +175	°C
T_L	Maximum Temperature for Soldering Leads at 0.063 in (1.6 mm) from Case for 10 s		300	°C
T_{pkg}	Maximum Temperature for Soldering Leads Package Body for 10 s		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. T_J = 25°C to 150°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF STATE CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V (Figure 11)	55			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			1	μA
		V_{DS} = 45 V, V_{GS} = 0 V, T_C = 150°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V			±100	nA
ON STATE CHARACTERISTICS						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA (Figure 10)	2		4.0	V
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 75 A, V_{GS} = 10 V (Figure 9)		0.006	0.007	Ω
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance Junction to Case	(Figure 3)			0.46	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	TO−247			30	°C/W
	Thermal Resistance Junction to Ambient	TO−220, D2PAK			62	°C/W
SWITCHING CHARACTERISTICS (V_{GS} = 10 V)						
t_{ON}	Turn-On Time	V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, V_{GS} = 10 V, R_{GS} = 2.5 Ω			195	ns
$t_{d(ON)}$	Turn-On Delay Time			14		ns
t_r	Rise Time			118		ns
$t_{d(OFF)}$	Turn-Off Delay Time			42		ns
t_f	Fall Time			26		ns
t_{OFF}	Turn-Off Time				98	ns
GATE CHARGE CHARACTERISTICS						
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 V to 20 V, V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, $I_{g(REF)}$ = 1.0 mA (Figure 13)		220	275	nC
$Q_{g(10)}$	Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, $I_{g(REF)}$ = 1.0 mA (Figure 13)		125	165	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V, V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, $I_{g(REF)}$ = 1.0 mA (Figure 13)		6.8	10	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 30 V, I_D = 75 A, R_L = 0.4 Ω, $I_{g(REF)}$ = 1.0 mA (Figure 13)		14		nC
Q_{gd}	Gate to Drain "Miller" Charge			58		nC
CAPACITANCE CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 Mhz (Figure 12)		4000		pF
C_{oss}	Output Capacitance			1450		pF
C_{rss}	Reverse Transfer Capacitance			450		pF
SOURCE TO DRAIN DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 75 A			1.25	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75 A, dI_{SD}/dt = 100 A/μs			55	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 75 A, dI_{SD}/dt = 100 A/μs			80	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE CURVES

T_C = 25°C unless otherwise noted

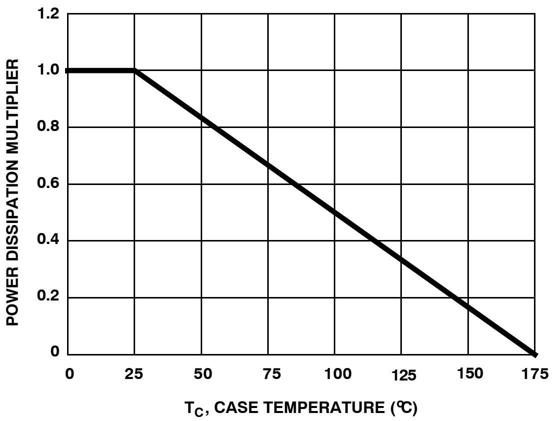


Figure 1. Normalized Power Dissipation vs. Case Temperature

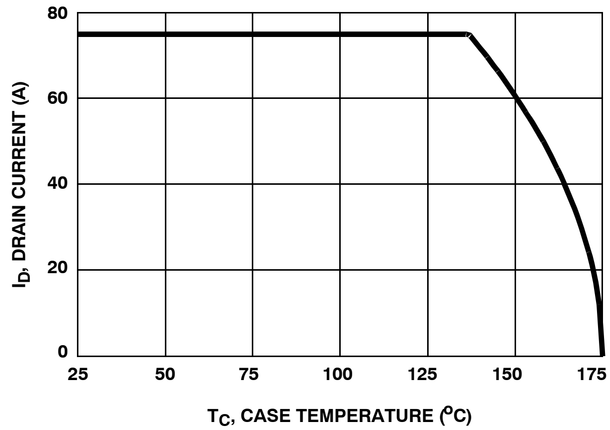


Figure 2. Maximum Continuous Drain Current vs Case Temperature

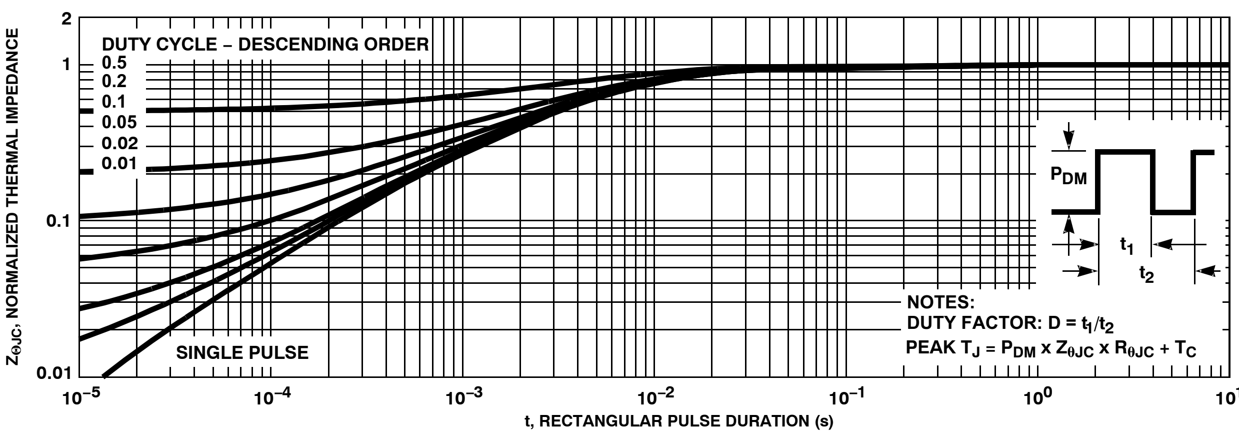


Figure 3. Normalized Maximum Transient Thermal Impedance

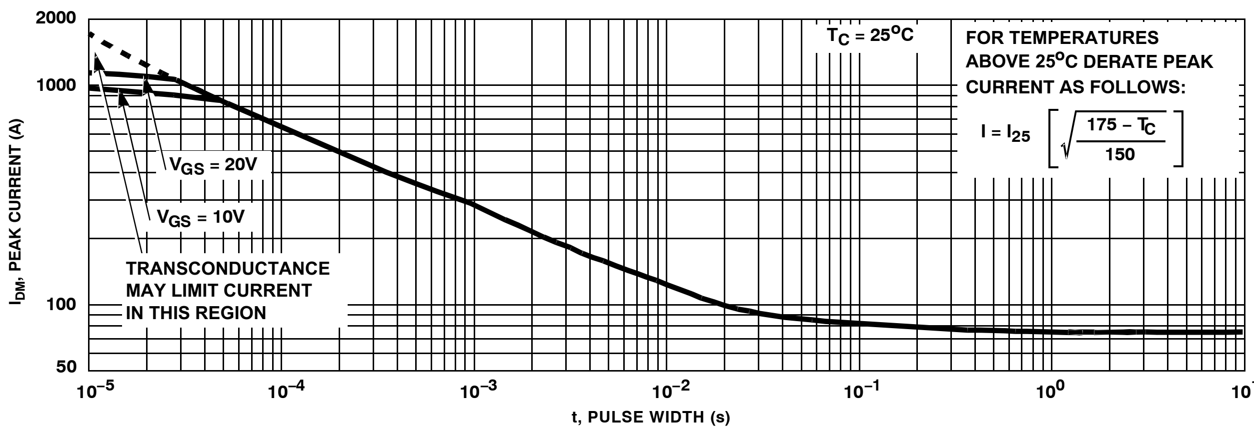


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (Continued)

T_C = 25°C unless otherwise noted

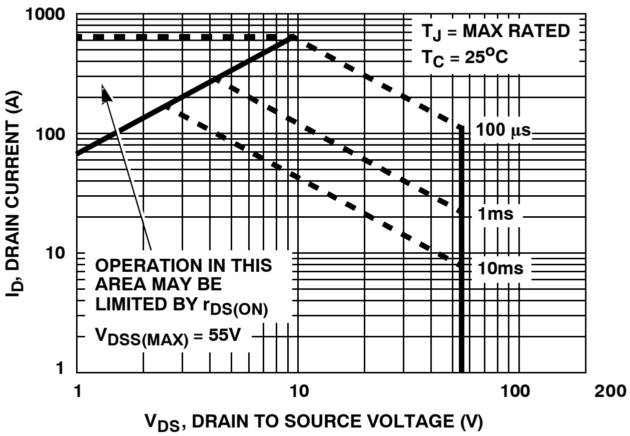


Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to ON Semiconductor Application Notes AN−7514 and AN−7515

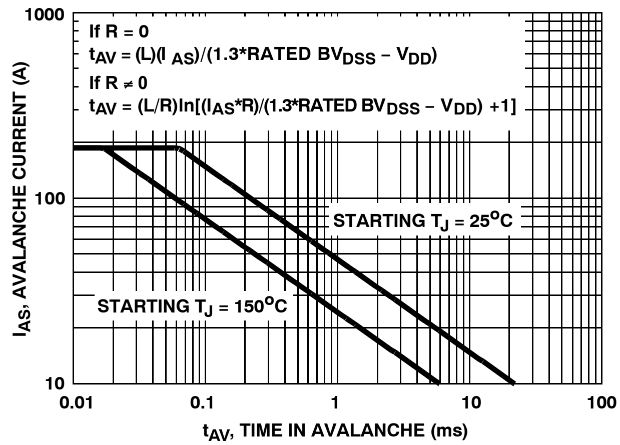


Figure 6. Unclamped Inductive Switching Capability

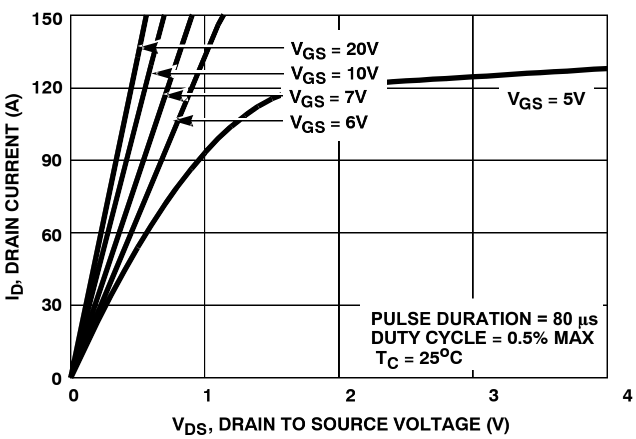


Figure 7. Saturation Characteristics

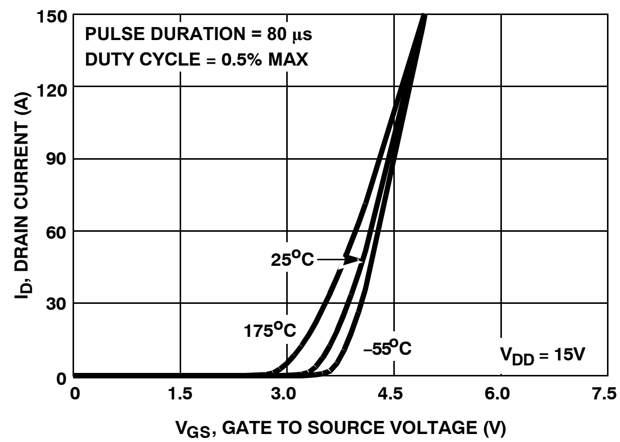


Figure 8. Transfer Characteristics

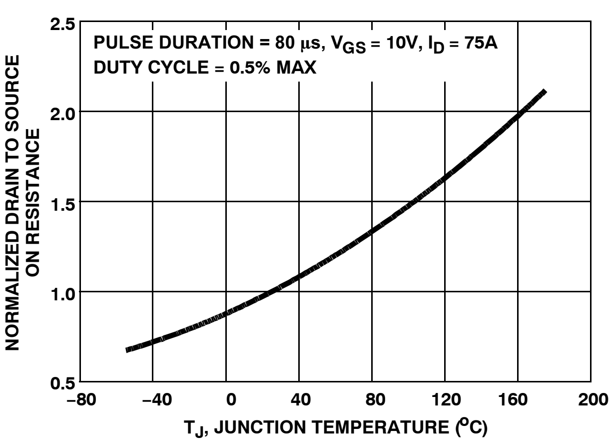


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

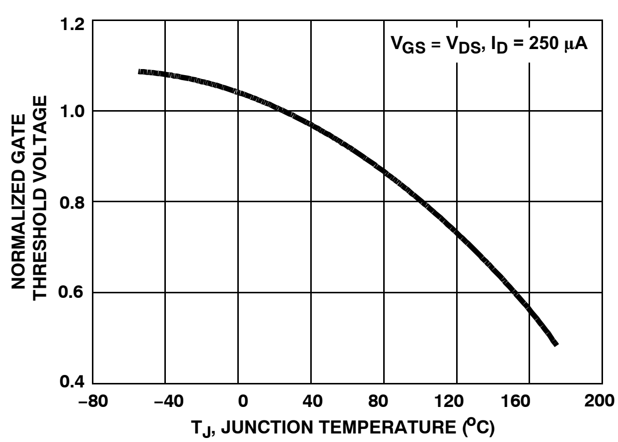


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

TYPICAL CHARACTERISTICS (Continued)

T_C = 25°C unless otherwise noted

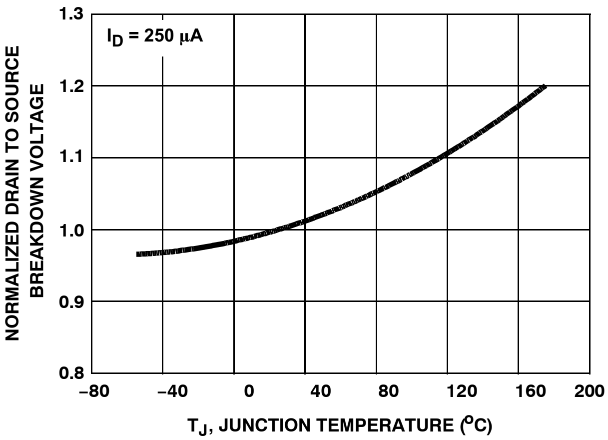


Figure 11. Normalized Drain to Source Breakdown vs. Junction Temperature

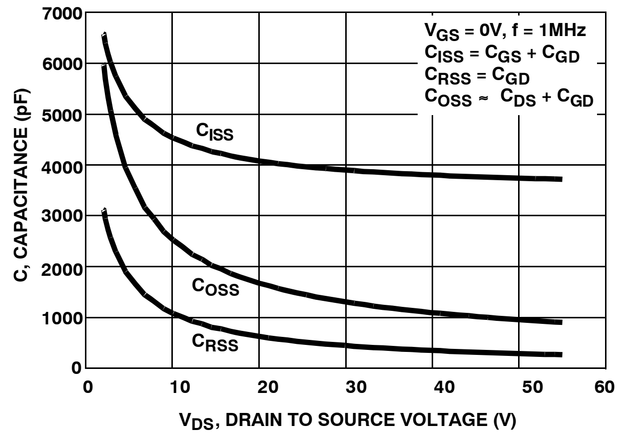


Figure 12. Capacitance vs. Drain to Source Voltage

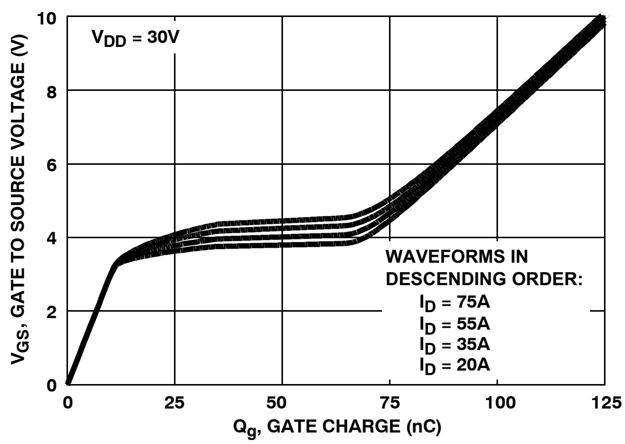


Figure 13. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS WAVEFORMS

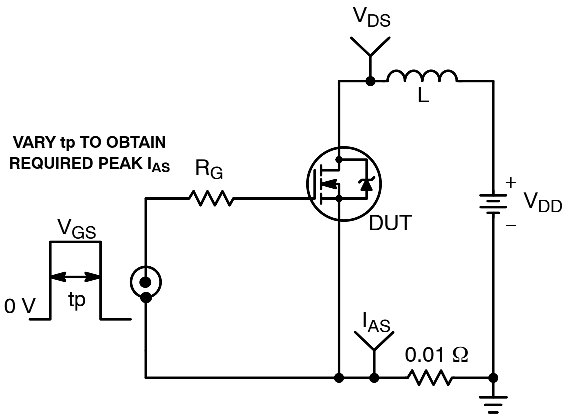


Figure 14. Unclamped Energy Test Circuit

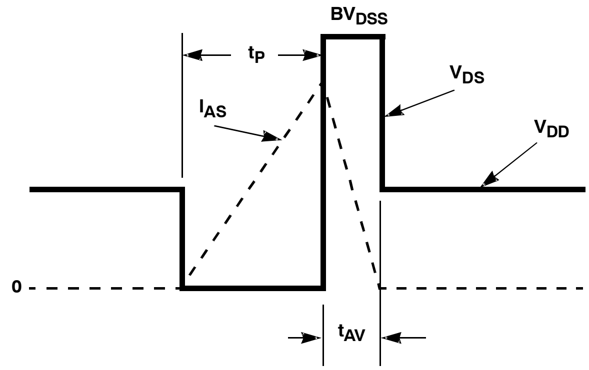


Figure 15. Unclamped Energy Waveforms

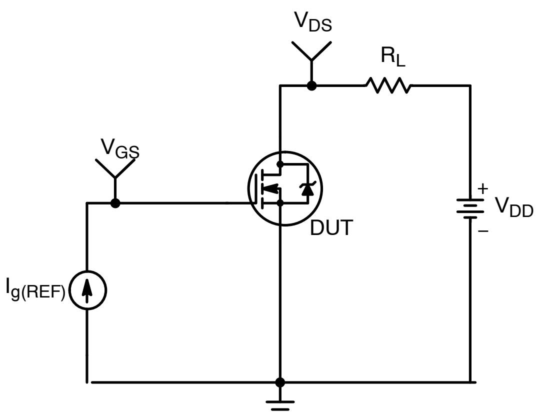


Figure 16. Gate Charge Test Circuit

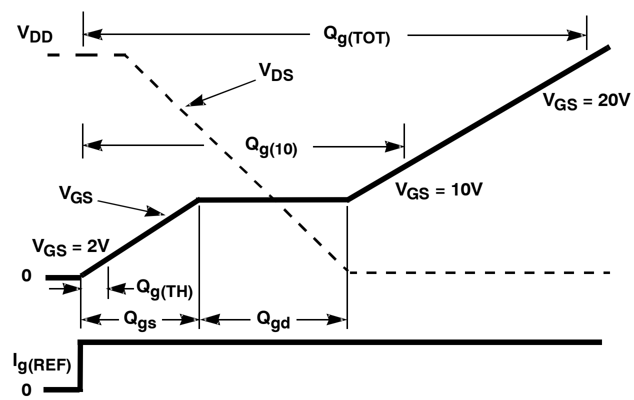


Figure 17. Gate Charge Waveforms

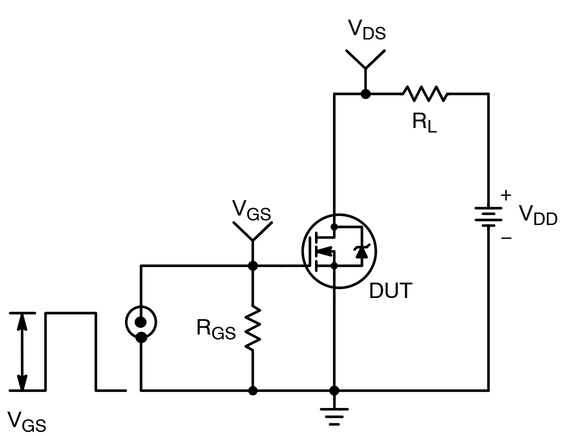


Figure 18. Switching Time Test Circuit

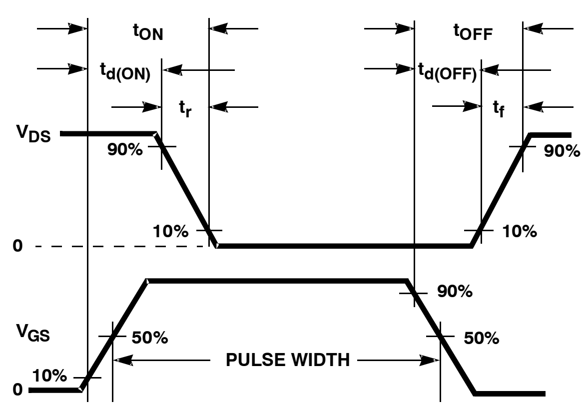


Figure 19. Resistive Switching Waveforms

PSPICE Electrical Model

```
.SUBCKT HUF75345 2 1 3 ; rev 3 Feb 99

CA 12 8 5.55e−9
CB 15 14 5.55e−9
CIN 6 8 3.45e−9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 56.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e−9
LGATE 1 9 2.6e−9
LSOURCE 3 7 1.1e−9
KGATE LSOURCE LGATE 0.0085

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1e−4
RGATE 9 20 0.36
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e−6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3.15e−3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e−6*500),3.5))}

.MODEL DBODYMOD D (IS = 6e−12 RS = 1.4e−3 IKF = 20 XTI = 5 TRS1 = 2.75e−3 TRS2 = 5.0e−6 CJO = 5.5e−9 TT =
5.9e−8 M = 0.5 VJ = 0.75)
.MODEL DBREAKMOD D (RS = 2.8e−2 IKF = 30 TRS1 = −4.0e−3 TRS2 = 1.0e−6)
.MODEL DPLCAPMOD D (CJO = 6.75e−9 IS = 1e−30 M = 0.88 VJ = 1.45 FC = 0.5)
.MODEL MMEDMOD NMOS (VTO = 2.93 KP = 13.75 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.36)
.MODEL MSTROMOD NMOS (VTO = 3.23 KP = 96 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u Lambda = 0.06)
.MODEL MWEAKMOD NMOS (VTO = 2.35 KP =0.02 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.6)
.MODEL RBREAKMOD RES (TC1 = 8.0e−4 TC2 = 4.0e−6)
.MODEL RDRAINMOD RES (TC1 = 1.5e−1 TC2 = 6.5e−4)
```

.MODEL RSLCMOD RES (TC1 = 1.0e−4 TC2 = 1.05e−6)
.MODEL RSOURCEMOD RES (TC1 = 1.0e−3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = −1.5e−3 TC2 = −2.6e−5)
.MODEL RVTEMPMOD RES (TC1 = −2.75e−3 TC2 = 1.45e−6)

.MODEL S1AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −9.00 VOFF= −4.00)
.MODEL S1BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −4.00 VOFF= −9.00)
.MODEL S2AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = 0.00 VOFF= 0.50)
.MODEL S2BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = 0.50 VOFF= 0.00)

.ENDS

NOTE: For further discussion of the PSPICE model, consult A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

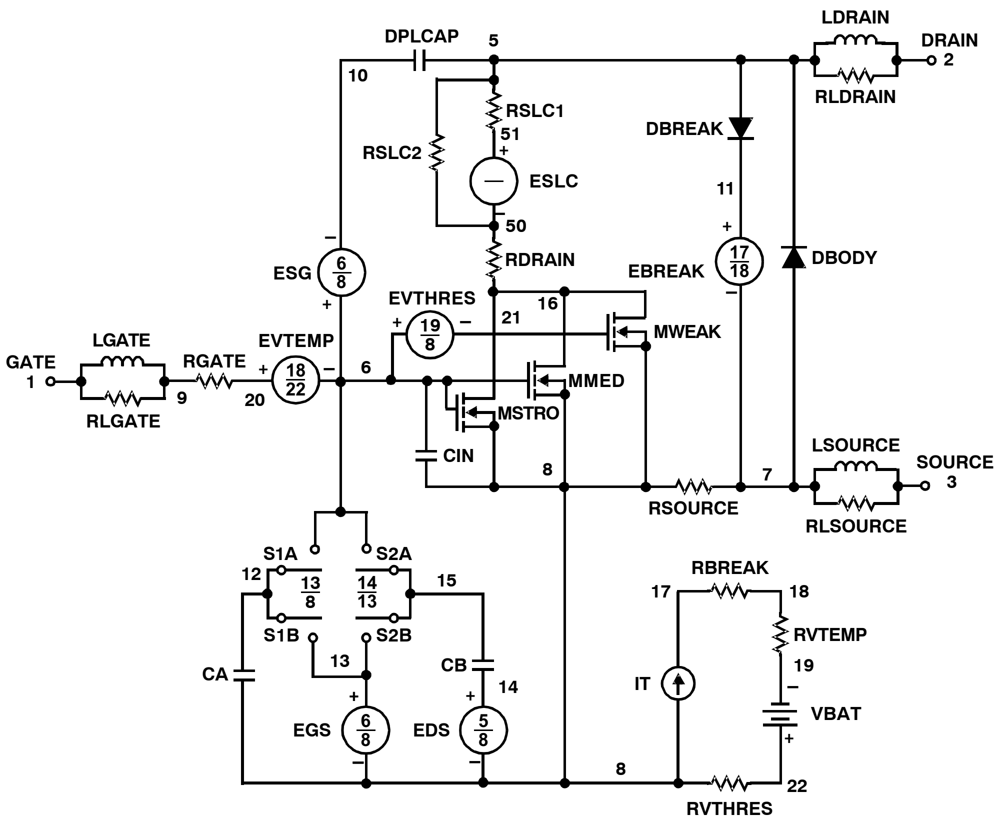


Figure 20. PSPICE Electrical Model

SABER Electrical Model

REV 3 February 1999

```
template huf75345 n2, n1, n3
electrical n2, n1, n3
{
var i iscl
d..model dbodymod = (is = 6e−12, xti = 5, cjo = 5.5e−9, tt = 5.9e−8, m=0.5, vj=0.75)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 6.75e−9, is = 1e−30, m = 0.88, vj = 1.45,fc=0.5)
m..model mmedmod = (type=_n, vto = 2.93, kp = 13.75, is = 1e−30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.23, kp = 96, is=1e−30,tox=1,
lambda = 0.06)
m..model mweakmod = (type=_n, vto = 2.35, kp = 0.02, is = 1e−30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e−5, roff = 0.1, von = −9, voff = −4)
sw_vcsp..model s1bmod = (ron = 1e−5, roff = 0.1, von = −4, voff = −9)
sw_vcsp..model s2amod = (ron = 1e−5, roff = 0.1, von = 0, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e−5, roff = 0.1, von = 0.5, voff = 0)

c.ca n12 n8 = 5.55e−9
c.cb n15 n14 = 5.55e−9
c.cin n6 n8 = 3.45e−9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e−9
l.lgate n1 n9 = 2.6e−9
l.lsource n3 n7 = 1.1e−9
k.k1 i(l.lgate) i(l.lsource) = l(l.lgate), l(l.lsource), 0.0085

m.mmed n16 n6 n8 n8 = model=mmedmod, l = 1u, w = 1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l = 1u, w = 1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l = 1u, w = 1u

res.rbreak n17 n18 = 1, tc1 = 8e−4, tc2 = 4e−6
res.rdbody n71 n5 = 1.4e−3, tc1 = 2.75e−3, tc2 = 5e−6
res.rdbreak n72 n5 = 2.8e−2, tc1 = −4e−3, tc2 = 1e−6
res.rdrain n50 n16 = 1e−4, tc1 = 1.5e−1, tc2 = 6.5e−4
res.rgate n9 n20 = 0.36
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rlsource n3 n7 = 11
res.rslc1 n5 n51 = 1e−6, tc1 = 1e−4, tc2 = 1.05e−6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 3.15e−3, tc1 = 1e−3, tc2 = 0
res.rvtemp n18 n19 = 1, tc1 = −2.75e−3, tc2 = 1.45e−6
res.rvthres n22 n8 = 1, tc1 = −1.5e−3, tc2 = −2.6e−5

spe.ebreak n11 n7 n17 n18 = 56.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc = 1

equations {
i (n51−>n50) + = iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/500))** 3.5))
}
}

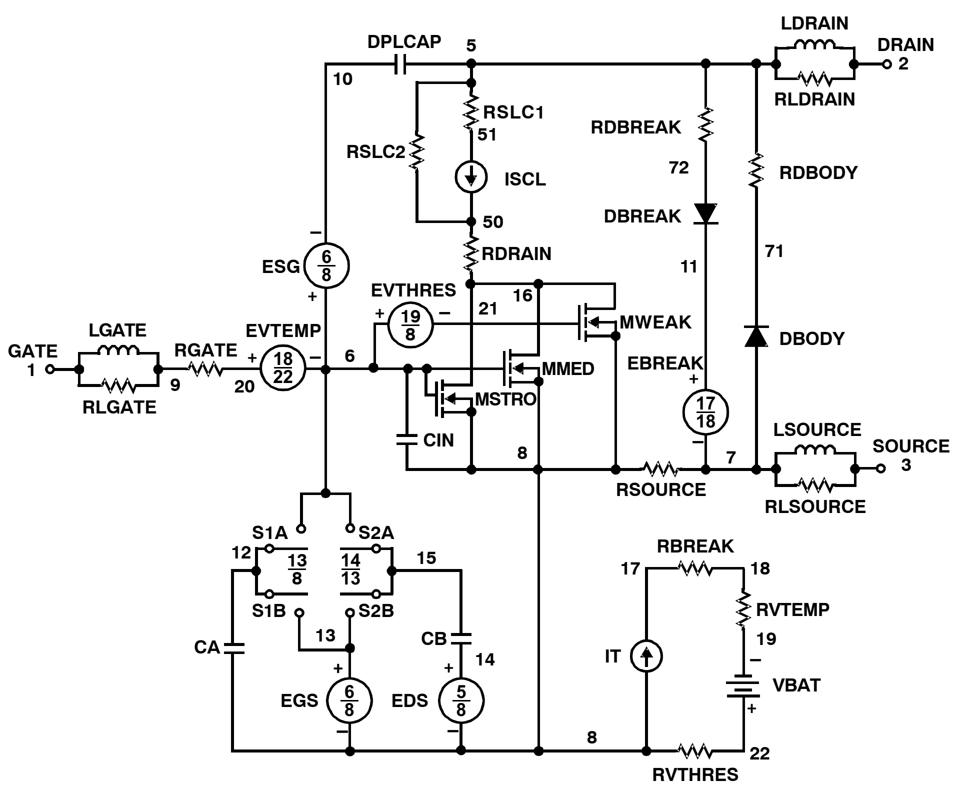


Figure 21. SABER Electrical Model

SPICE Thermal Model

REV 5 February 1999

HUF75345

CTHERM1 th 6 6.3e−3
CTHERM2 6 5 1.5e−2
CTHERM3 5 4 2.0e−2
CTHERM4 4 3 3.0e−2
CTHERM5 3 2 8.0e−2
CTHERM6 2 tl 1.5e−1

RTHERM1 th 6 5.0e−3
RTHERM2 6 5 1.8e−2
RTHERM3 5 4 5.0e−2
RTHERM4 4 3 8.5e−2
RTHERM5 3 2 1.0e−1
RTHERM6 2 tl 1.1e−1

SABER Thermal Model

SABER thermal model HUF75345

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 6.3e−3
ctherm.ctherm2 6 5 = 1.5e−2
ctherm.ctherm3 5 4 = 2.0e−2
ctherm.ctherm4 4 3 = 3.0e−2
ctherm.ctherm5 3 2 = 8.0e−2
ctherm.ctherm6 2 tl = 1.5e−1

rtherm.rtherm1 th 6 = 5.0e−3
rtherm.rtherm2 6 5 = 1.8e−2
rtherm.rtherm3 5 4 = 5.0e−2
rtherm.rtherm4 4 3 = 8.5e−2
rtherm.rtherm5 3 2 = 1.0e−1
rtherm.rtherm6 2 tl = 1.1e−1
}

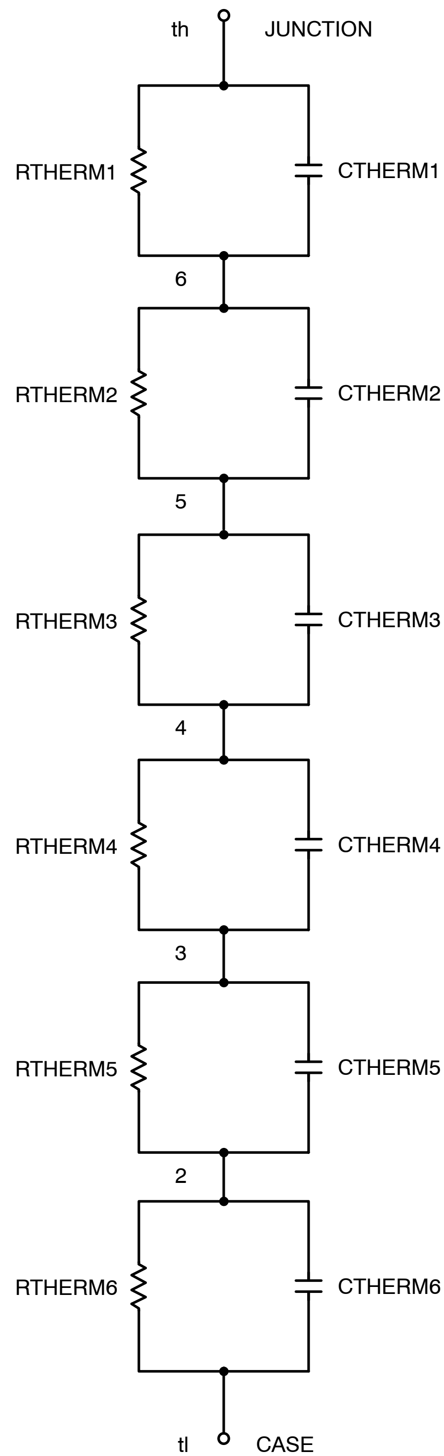


Figure 22. Thermal Model

PSPICE is a trademark of MicroSim Corporation.
Saber is a registered trademark of Sabremark Limited Partnership.

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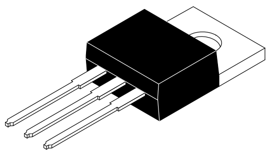
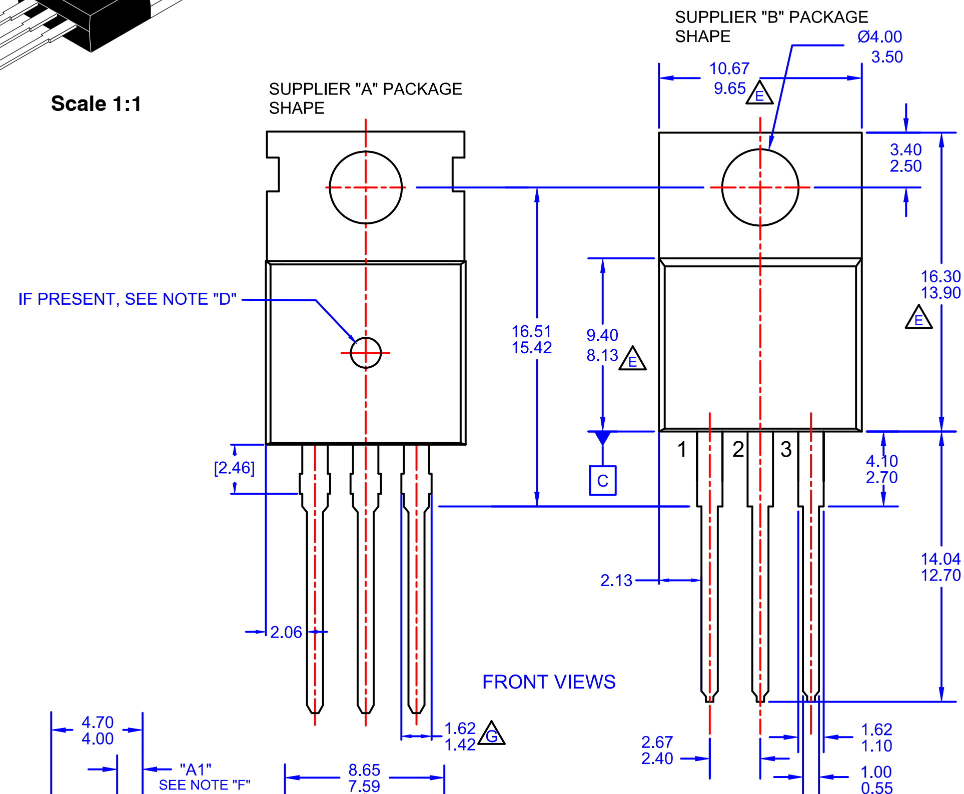
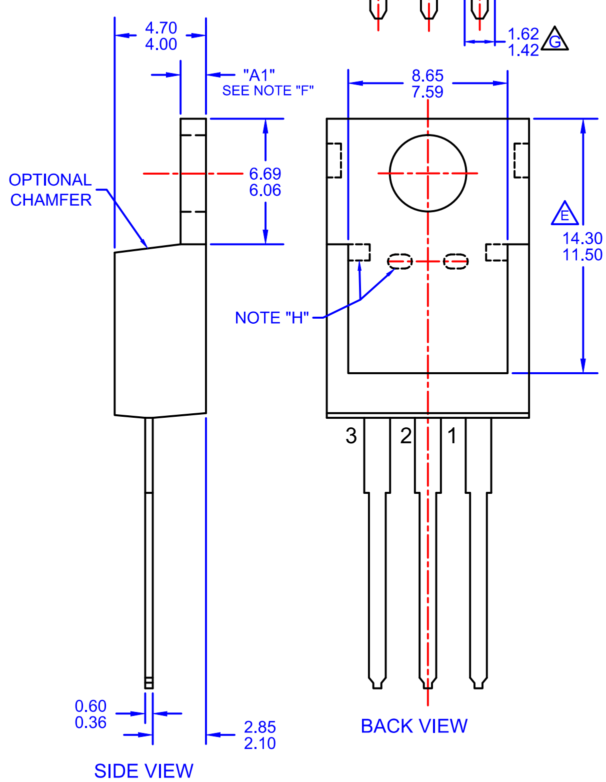


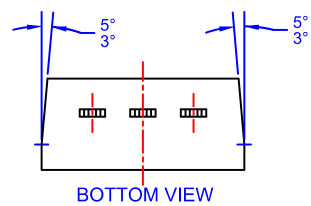
Scale 1:1

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017







NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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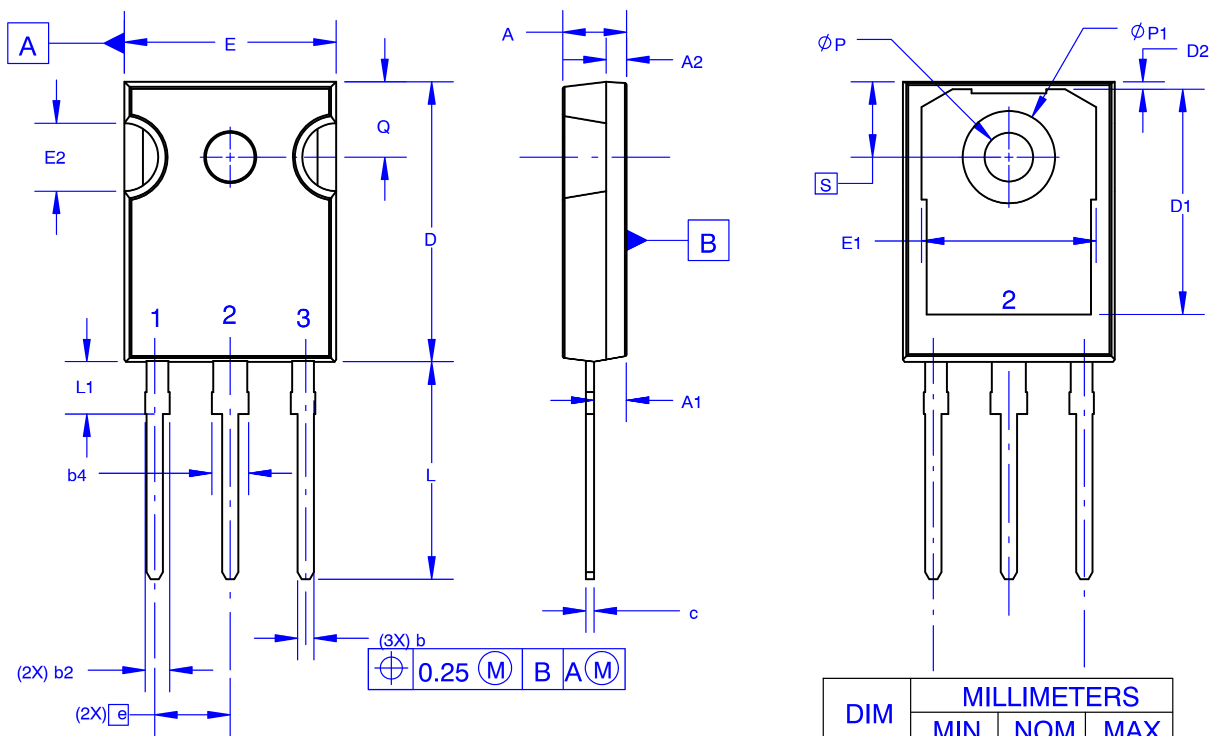
DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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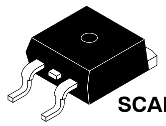
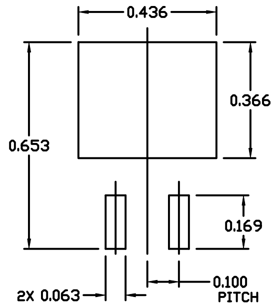
DESCRIPTION:	TO−247−3LD SHORT LEAD	PAGE 1 OF 1



SCALE 1:1

D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021

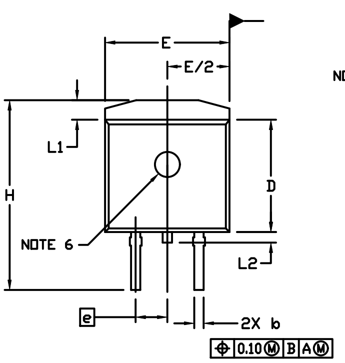


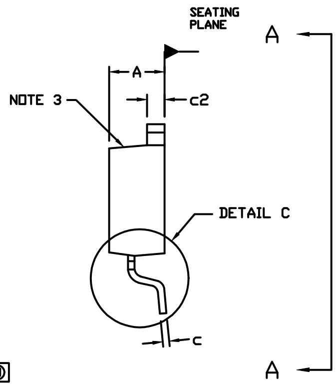
RECOMMENDED
MOUNTING FOOTPRINT

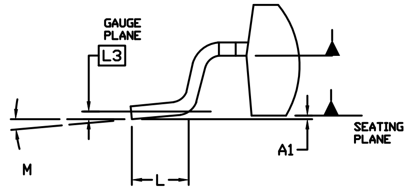
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

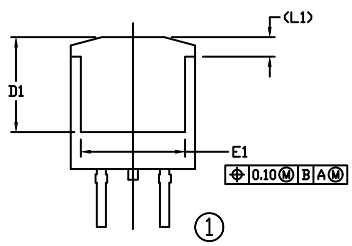
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°



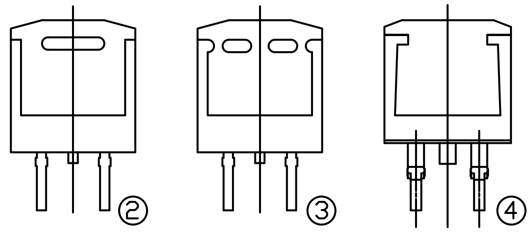




DETAIL C
TIP LEADFORM
ROTATED 90° CW

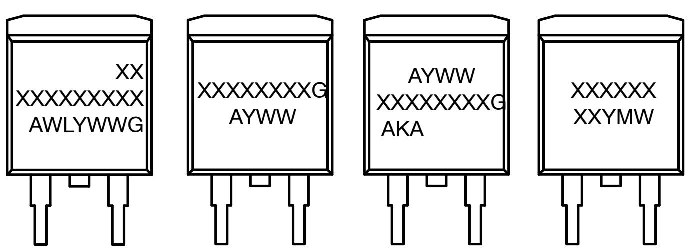


VIEW A−A



VIEW A−A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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