

MC74HC541A

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

The MC74HC541A is identical in pinout to the LS541. The device inputs are compatible with Standard CMOS outputs. External pull-up resistors make them compatible with LSTTL outputs.

The HC541A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC541A is similar in function to the HC540A, which has inverting outputs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

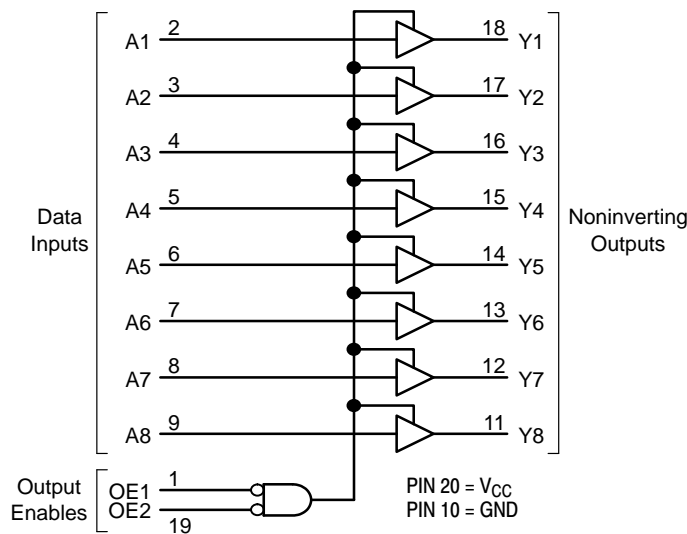
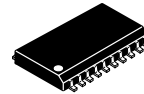


Figure 1. Logic Diagram



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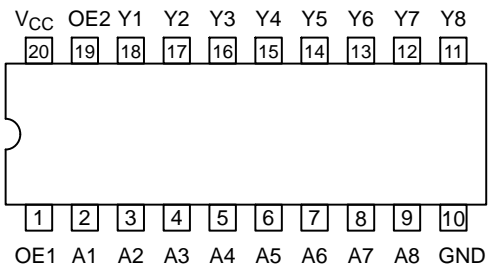


SOIC-20
DW SUFFIX
CASE 751D

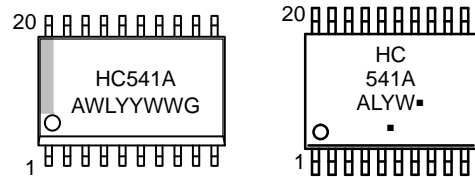


TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-20 TSSOP-20

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | | Output Y |
|--------|-----|---|----------|
| OE1 | OE2 | A | |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

X = Don't Care
Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74HC541A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_I | DC Input Voltage | $-0.5 \leq V_I \leq V_{CC} + 0.5$ | V |
| V_O | DC Output Voltage (Note 1) | $-0.5 \leq V_O \leq V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 35 | mA |
| I_O | DC Output Sink Current | ± 35 | mA |
| I_{CC} | DC Supply Current per Supply Pin | ± 75 | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 75 | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T_J | Junction Temperature under Bias | +150 | °C |
| θ_{JA} | Thermal Resistance | SOIC TSSOP 96 128 | °C/W |
| P_D | Power Dissipation in Still Air at 85°C | SOIC TSSOP 500 450 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F_R | Flammability Rating | Oxygen Index: 30% – 35% UL 94 V-0 @ 0.125 in | |
| V_{ESD} | ESD Withstand Voltage | Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) > 4000 > 300 > 1000 | V |
| $I_{Latchup}$ | Latchup Performance | Above V_{CC} and Below GND at 85°C (Note 5) | ± 300 mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------------|---------------------------------------------------------|-------------------------------------------------------------------------------|-------------|--------------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{IN} , V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature Range, All Package Types | -55 | +125 | °C |
| t_r , t_f | Input Rise/Fall Time (Figure 2) | $V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$ | 0 0 0 | 1000 500 400 ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

MC74HC541A

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|-------|--------|------|
| | | | | -55 to 25°C | ≤85°C | ≤125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = 0.1 V I _{OUT} ≤ 20 μA | 2.0 | 1.50 | 1.50 | 1.50 | V |
| | | | 3.0 | 2.10 | 2.10 | 2.10 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.20 | 4.20 | 4.20 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} = V _{CC} - 0.1 V I _{OUT} ≤ 20 μA | 2.0 | 0.50 | 0.50 | 0.50 | V |
| | | | 3.0 | 0.90 | 0.90 | 0.90 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.80 | 1.80 | 1.80 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} = V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{IN} = V _{IL} I _{OUT} ≤ 3.6 mA I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA | 3.0 | 2.48 | 2.34 | 2.20 | |
| | | | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | | 6.0 | 5.48 | 5.34 | 5.20 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IH} I _{OUT} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{IN} = V _{IH} I _{OUT} ≤ 3.6 mA I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA | 3.0 | 0.26 | 0.33 | 0.40 | |
| | | | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | | 6.0 | 0.26 | 0.33 | 0.40 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum 3-State Leakage Current | Output in High Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} = V _{CC} or GND I _{OUT} = 0 μA | 6.0 | 4 | 40 | 160 | μA |

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|----------------------------------------|---------------------------------------------------------------------------|----------------------------------------------------------------|------------------|-------|--------|------|
| | | | -55 to 25°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4) | 2.0 | 80 | 100 | 120 | ns |
| | | 3.0 | 30 | 40 | 55 | |
| | | 4.5 | 18 | 23 | 28 | |
| | | 6.0 | 15 | 20 | 25 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 45 | 60 | 75 | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 31 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 | 110 | 140 | 165 | ns |
| | | 3.0 | 45 | 60 | 75 | |
| | | 4.5 | 25 | 31 | 38 | |
| | | 6.0 | 21 | 26 | 31 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 2 and 4) | 2.0 | 60 | 75 | 90 | ns |
| | | 3.0 | 22 | 28 | 34 | |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{IN} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |
| C _{OUT} | Maximum 3-State Output Capacitance (High Impedance State Output) | | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Buffer) (Note 7) | Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V | | | pF | |
| | | 35 | | | | |

7. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

MC74HC541A

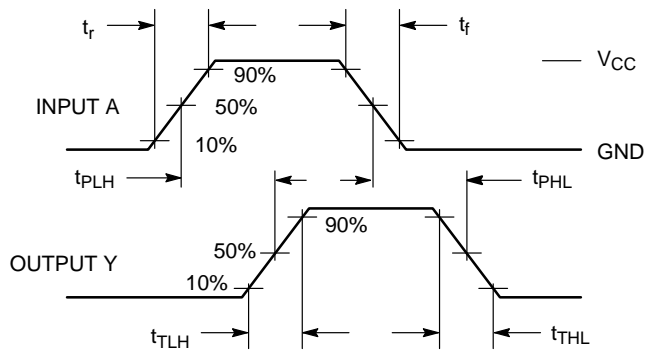


Figure 2. Switching Waveform

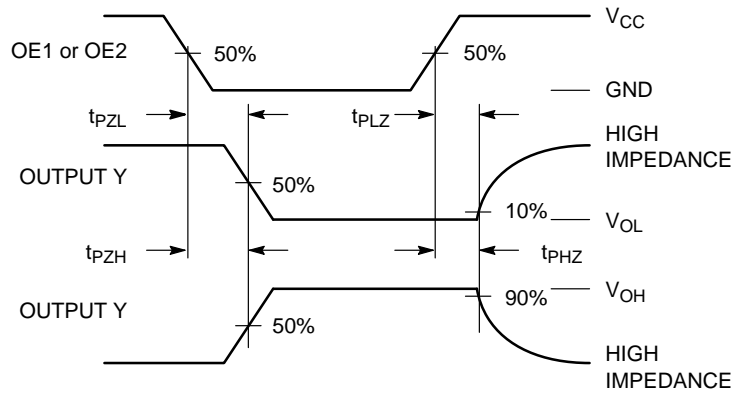
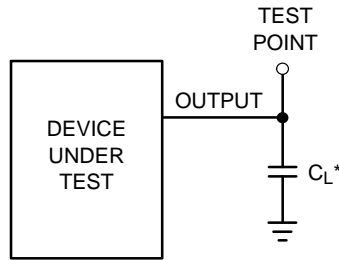
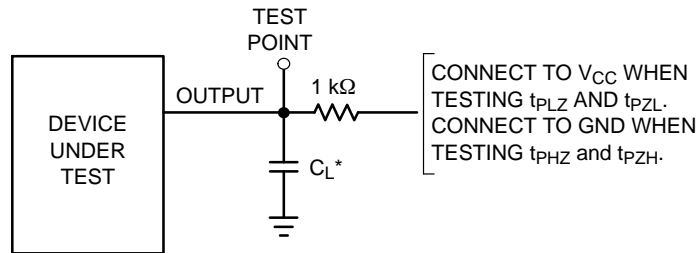


Figure 3. Switching Waveform



*Includes all probe and jig capacitance

Figure 4. Test Circuit



*Includes all probe and jig capacitance

Figure 5. Test Circuit

MC74HC541A

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)

Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

OE1, OE2 (PINS 1, 19)

Output enables (active-low). When a low voltage is applied to both of these pins, the outputs are enabled and the

device functions as a non-inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)

Device outputs. Depending upon the state of the output enable pins, these outputs are either non-inverting outputs or high-impedance outputs.

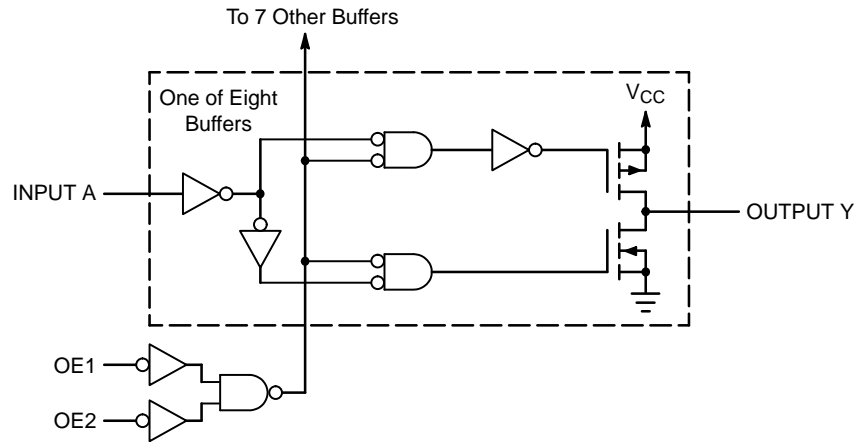


Figure 6. Logic Detail

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------------|---------------------------|------------------|
| MC74HC541ADWG | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail |
| MC74HC541ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| NLV74HC541ADWR2G* | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| MC74HC541ADTG | TSSOP-20 (Pb-Free) | 75 Units / Rail |
| MC74HC541ADTR2G | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |
| NLV74HC541ADTR2G* | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

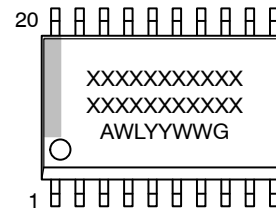
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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