

# MJD41C (NPN), MJD42C (PNP)

## Complementary Power Transistors

### DPAK for Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

#### Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Epoxy Meets UL 94 V-0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current – Continuous	$I_C$	6	Adc
Collector Current – Peak	$I_{CM}$	10	Adc
Base Current	$I_B$	2	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

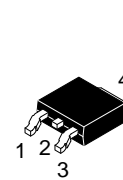
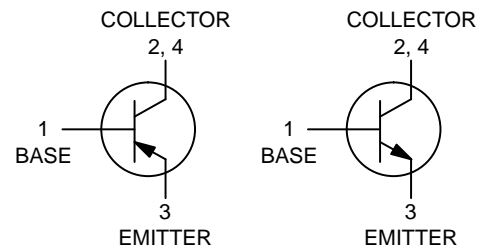


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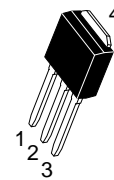
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### SILICON POWER TRANSISTORS 6 AMPERES 100 VOLTS, 20 WATTS

#### COMPLEMENTARY

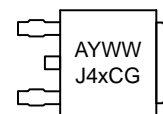


**DPAK  
CASE 369C  
STYLE 1**

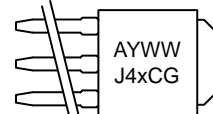


**IPAK  
CASE 369D  
STYLE 1**

#### MARKING DIAGRAMS



**DPAK**



**IPAK**

A = Assembly Location  
Y = Year  
WW = Work Week  
J4xC = Device Code  
x = 1 or 2  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MJD41C (NPN), MJD42C (PNP)

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	71.4	°C/W

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	100	–	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	50	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	$I_{CES}$	–	10	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	0.5	mAdc

### ON CHARACTERISTICS (Note 3)

DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 3\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	30 15	– 75	–
Collector-Emitter Saturation Voltage ( $I_C = 6\text{ Adc}$ , $I_B = 600\text{ mAdc}$ )	$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage ( $I_C = 6\text{ Adc}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	–	2	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product (Note 4) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	3	–	MHz
Small-Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	20	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4.  $f_T = |h_{fe}| \cdot f_{test}$ .

# MJD41C (NPN), MJD42C (PNP)

## TYPICAL CHARACTERISTICS

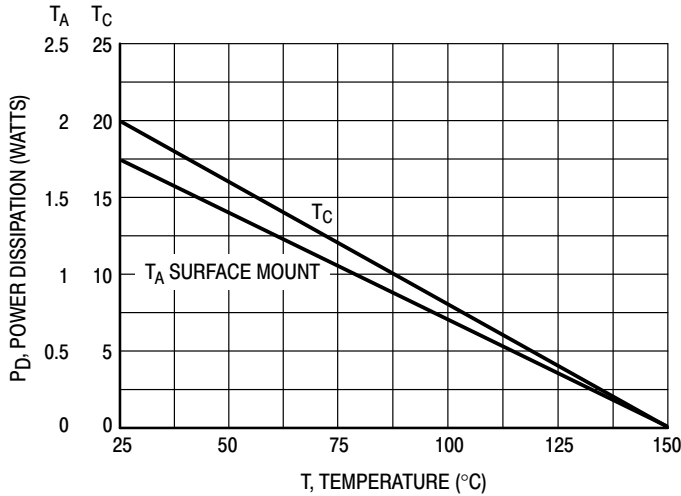


Figure 1. Power Derating

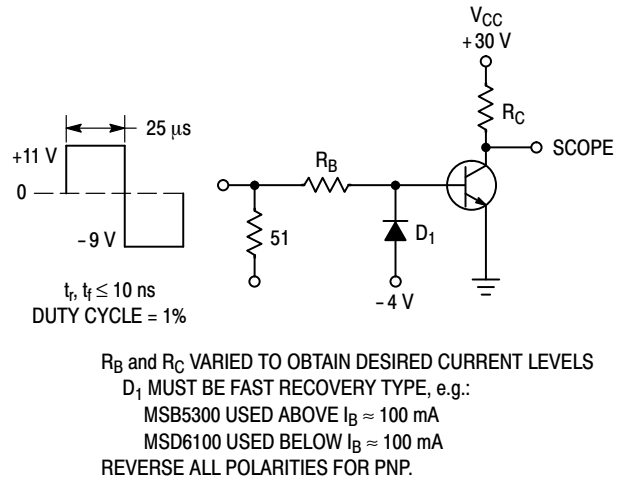


Figure 2. Switching Time Test Circuit

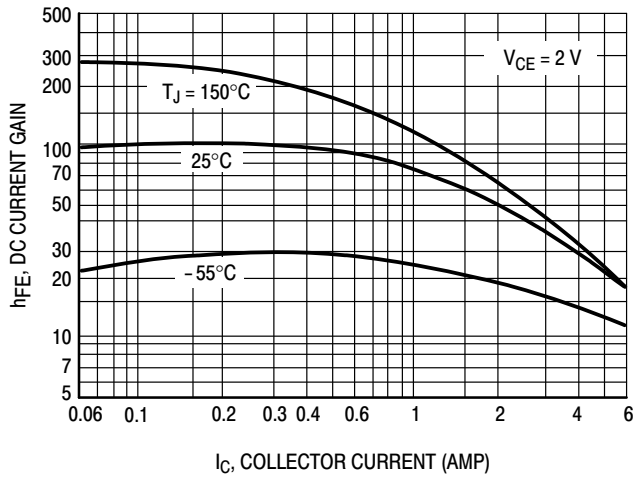


Figure 3. DC Current Gain

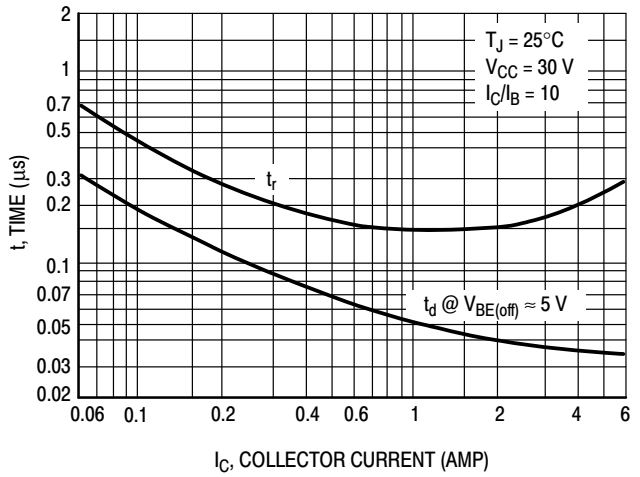


Figure 4. Turn-On Time

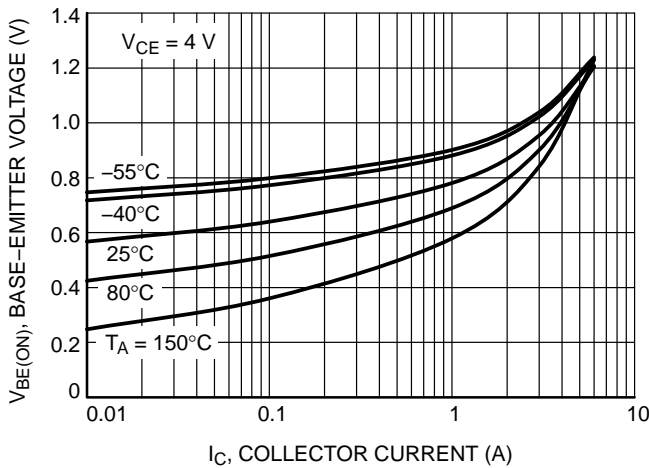


Figure 5. Base Emitter Voltage vs. Collector Current

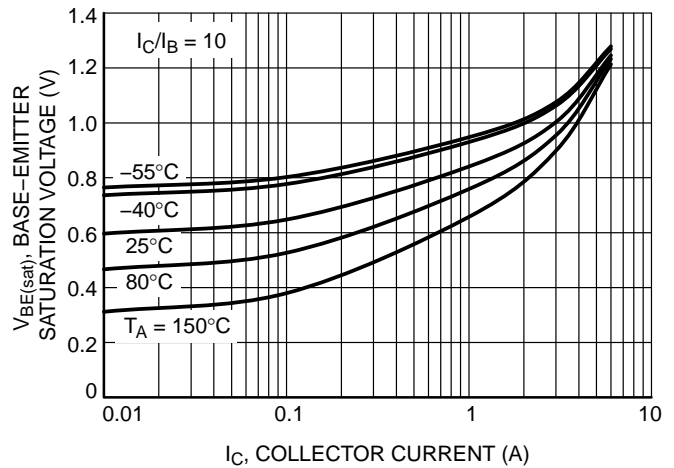


Figure 6. Base Emitter Saturation Voltage vs. Collector Current

# MJD41C (NPN), MJD42C (PNP)

## TYPICAL CHARACTERISTICS

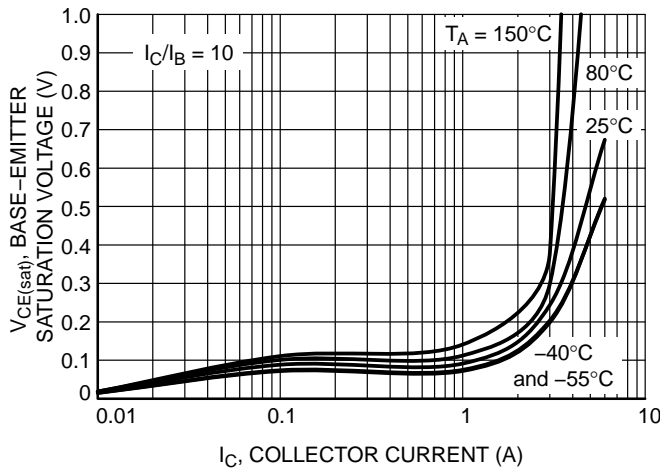


Figure 7. Collector Emitter Saturation Voltage vs. Collector Current

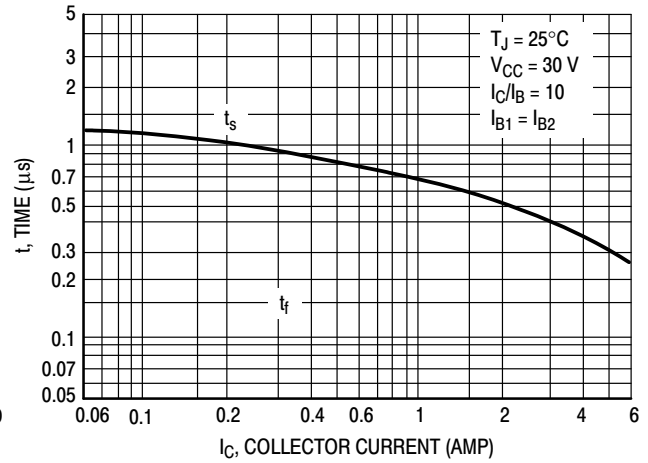


Figure 8. Turn-Off Time

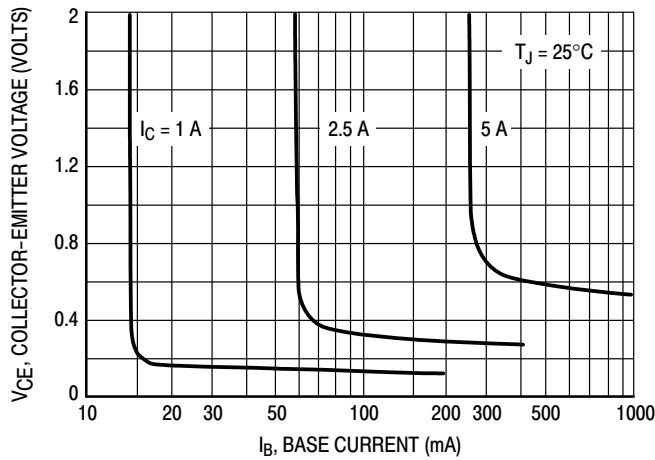


Figure 9. Collector Saturation Region

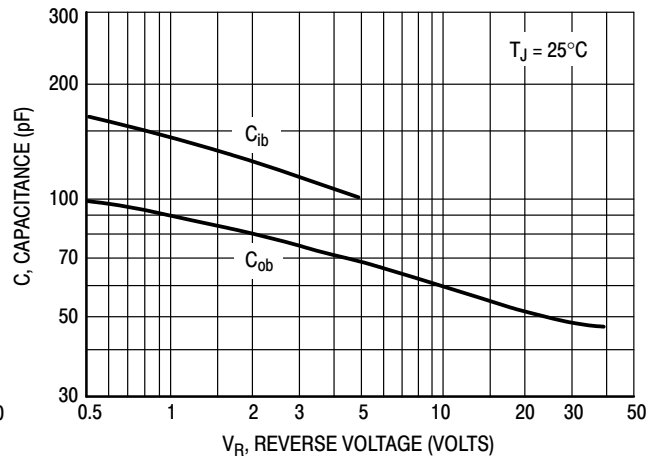


Figure 10. Capacitance

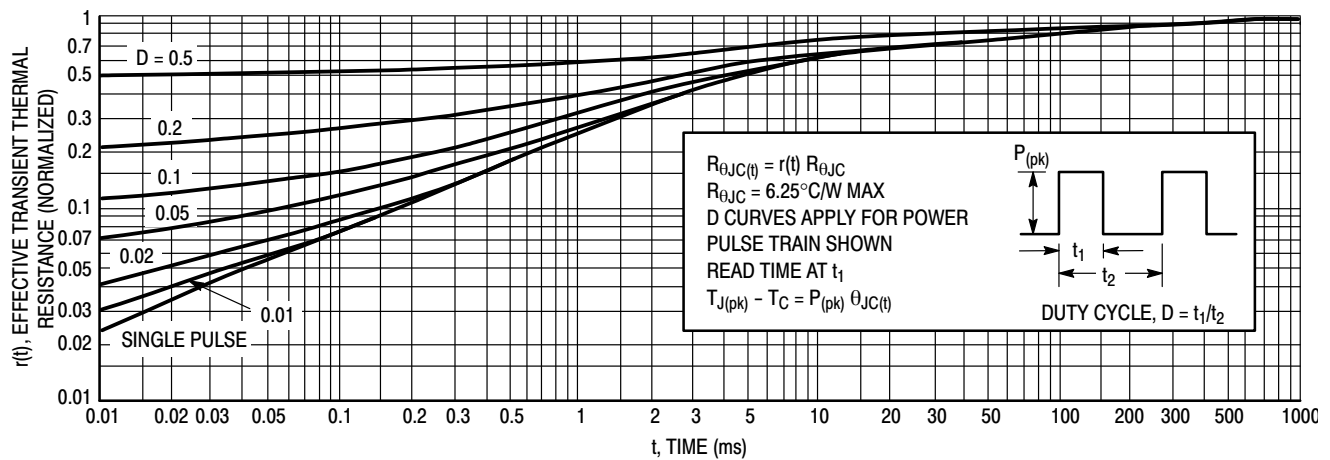
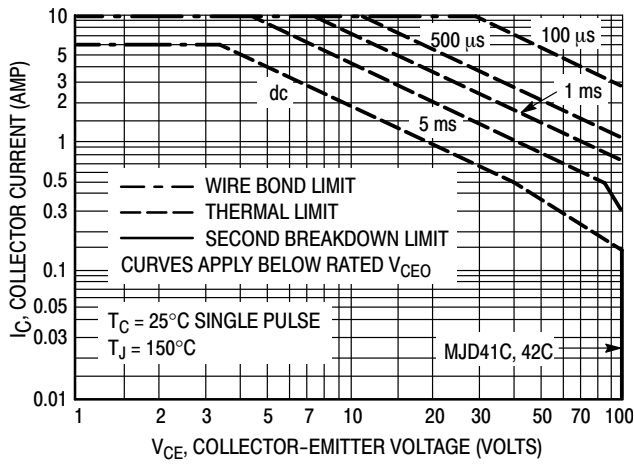


Figure 11. Thermal Response

## MJD41C (NPN), MJD42C (PNP)



**Figure 12. Maximum Forward Bias  
Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### ORDERING INFORMATION

Device	Package Type	Package	Shipping <sup>†</sup>
MJD41CRLG	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
MJD41CT4G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD41CT4G*	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
MJD42CG	DPAK (Pb-Free)	369C	75 Units / Rail
MJD42C1G	IPAK (Pb-Free)	369D	75 Units / Rail
MJD42CRLG	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
NJVMJD42CRLG*	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
MJD42CT4G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD42CT4G*	DPAK (Pb-Free)	369C	2,500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

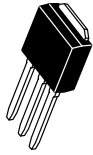
\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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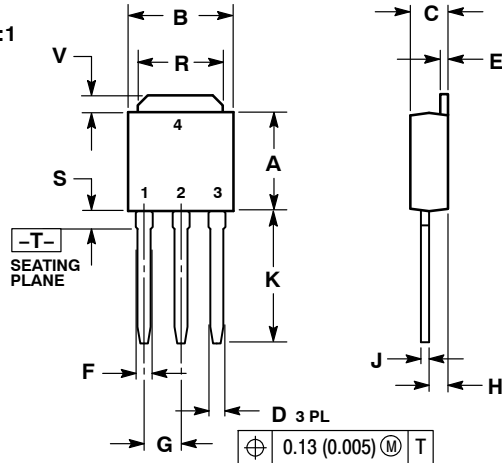
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



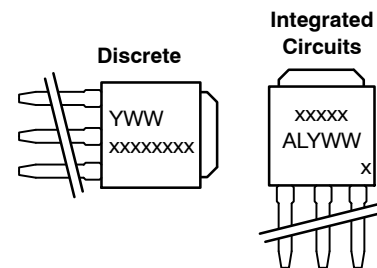
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

### MARKING DIAGRAMS

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

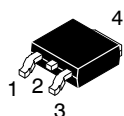


xxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

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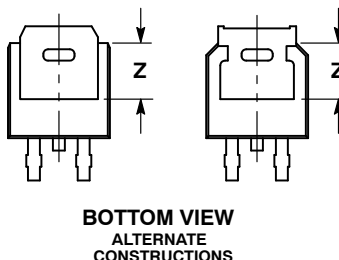
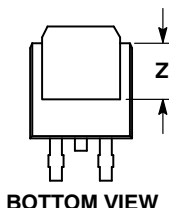
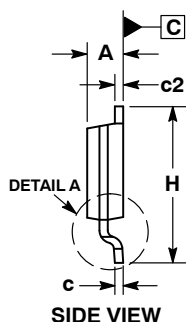
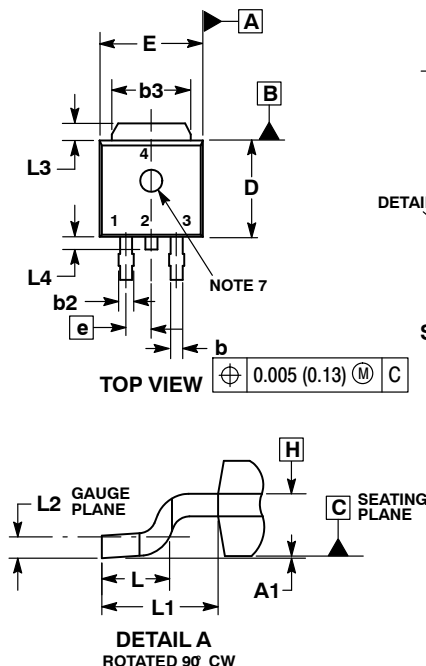
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

## DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015

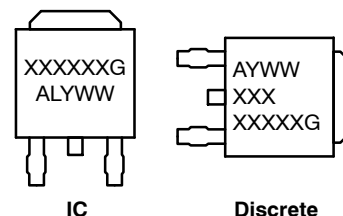


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

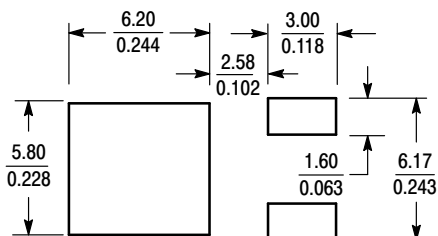


XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 8:  
PIN 1. N/C  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. RESISTOR ADJUST  
4. CATHODE
- STYLE 10:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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