

# MJL3281A (NPN) MJL1302A (PNP)

## Complementary Bipolar Power Transistors

### Features

- Exceptional Safe Operating Area
- NPN/PNP Gain Matching within 10% from 50 mA to 5 A
- Excellent Gain Linearity
- High BVCEO
- High Frequency
- These Devices are Pb-Free and are RoHS Compliant\*

### Benefits

- Reliable Performance at Higher Powers
- Symmetrical Characteristics in Complementary Configurations
- Accurate Reproduction of Input Signal
- Greater Dynamic Range
- High Amplifier Bandwidth

### Applications

- High-End Consumer Audio Products
  - ◆ Home Amplifiers
  - ◆ Home Receivers
- Professional Audio Amplifiers
  - ◆ Theater and Stadium Sound Systems
  - ◆ Public Address Systems (PAs)

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	260	Vdc
Collector-Base Voltage	V <sub>CBO</sub>	260	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	5.0	Vdc
Collector-Emitter Voltage - 1.5 V	V <sub>CEX</sub>	260	Vdc
Collector Current - Continuous	I <sub>C</sub>	15	Adc
Collector Current - Peak (Note 1)	I <sub>CM</sub>	25	Adc
Base Current - Continuous	I <sub>B</sub>	1.5	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate Above 25°C	P <sub>D</sub>	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 65 to +150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.625	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

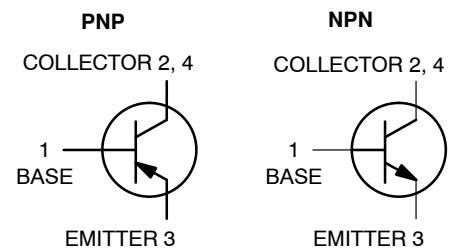
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



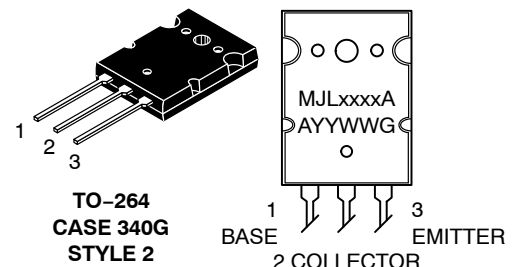
**ON Semiconductor®**

<http://onsemi.com>

**15 AMPERES  
COMPLEMENTARY  
SILICON POWER  
TRANSISTORS  
260 VOLTS  
200 WATTS**



### MARKING DIAGRAM



xxxx = 3281 or 1302  
A = Location Code  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
MJL3281AG	TO-264 (Pb-Free)	25 Units/Rail
MJL1302AG	TO-264 (Pb-Free)	25 Units/Rail

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## MJL3281A (NPN) MJL1302A (PNP)

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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#### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	260	–	Vdc
Collector Cutoff Current ( $V_{CB} = 260\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	50	$\mu\text{A dc}$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	5	$\mu\text{A dc}$

#### SECOND BREAKDOWN

Second Breakdown Collector with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive)) ( $V_{CE} = 100\text{ Vdc}$ , $t = 1\text{ s}$ (non-repetitive))	$I_{S/b}$	4 1	– –	A dc
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#### ON CHARACTERISTICS

DC Current Gain ( $I_C = 500\text{ mA dc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 1\text{ A dc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 3\text{ A dc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 5\text{ A dc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 8\text{ A dc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	75 75 75 75 45	150 150 150 150 –	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ A dc}$ , $I_B = 1\text{ A dc}$ )	$V_{CE(sat)}$	–	3	Vdc

#### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ( $I_C = 1\text{ A dc}$ , $V_{CE} = 5\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	30	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	–	600	pF

# MJL3281A (NPN) MJL1302A (PNP)

## TYPICAL CHARACTERISTICS

PNP MJL1302A

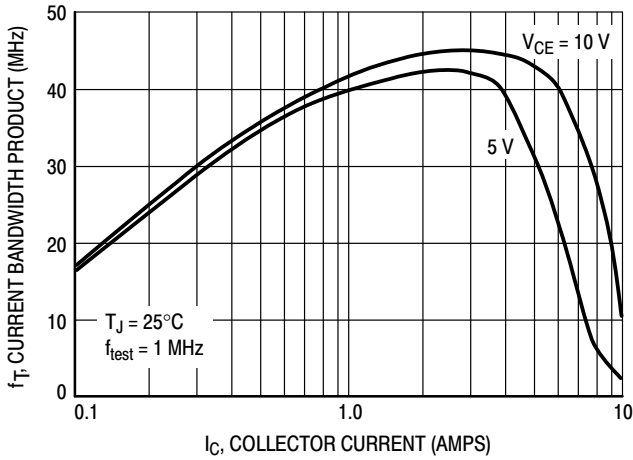


Figure 1. Typical Current Gain Bandwidth Product

NPN MJL3281A

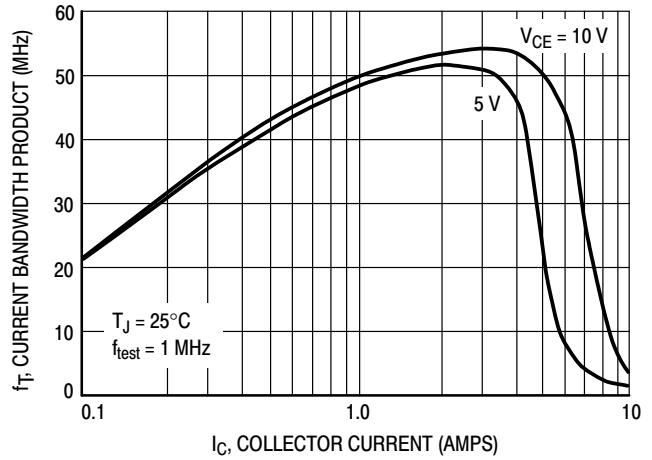


Figure 2. Typical Current Gain Bandwidth Product

PNP MJL1302A

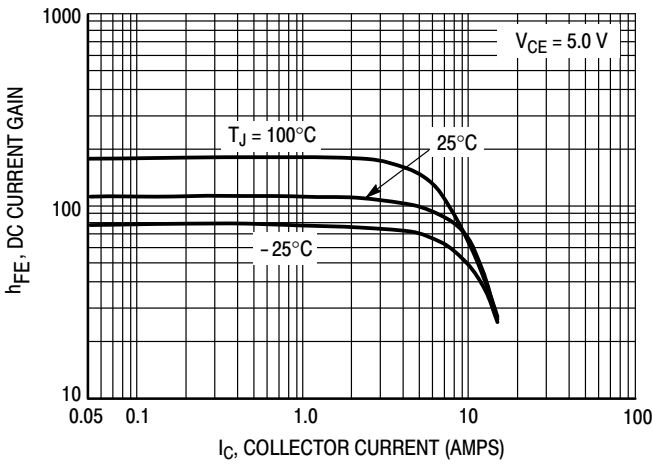


Figure 3. DC Current Gain

NPN MJL3281A

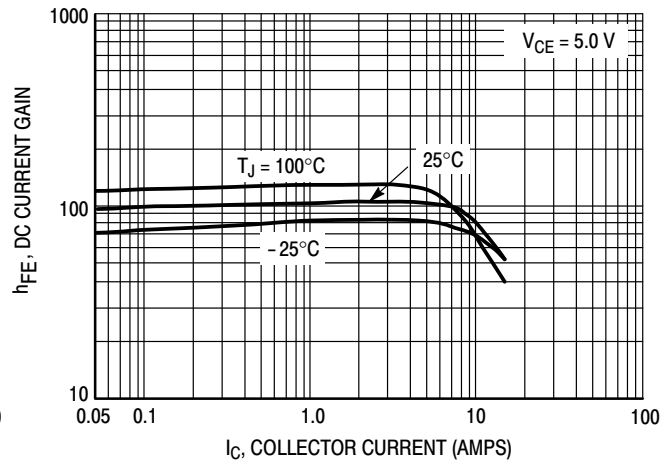


Figure 4. DC Current Gain

PNP MJL1302A

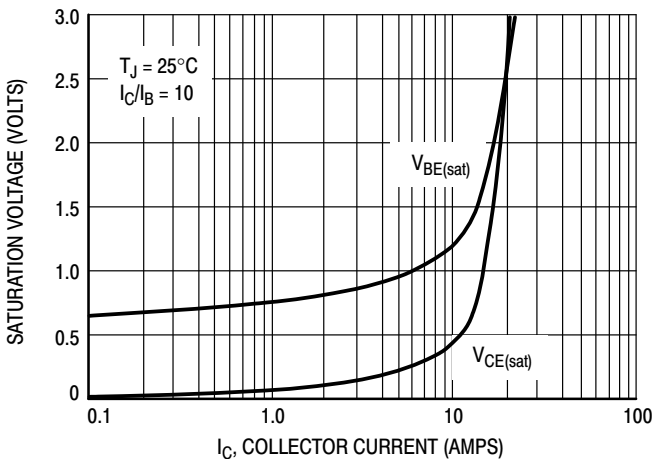


Figure 5. Typical Saturation Voltages

NPN MJL3281A

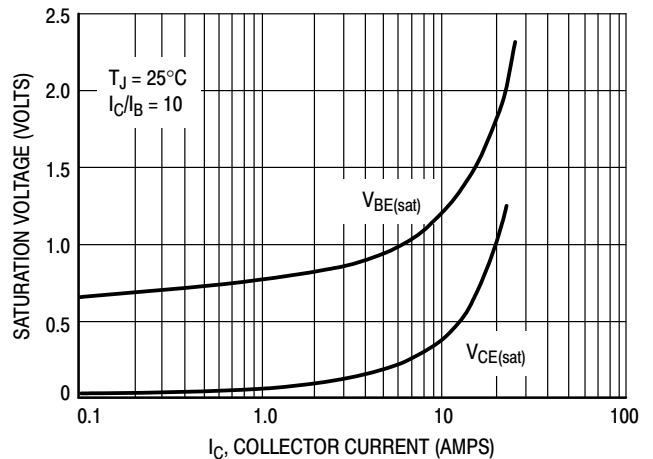
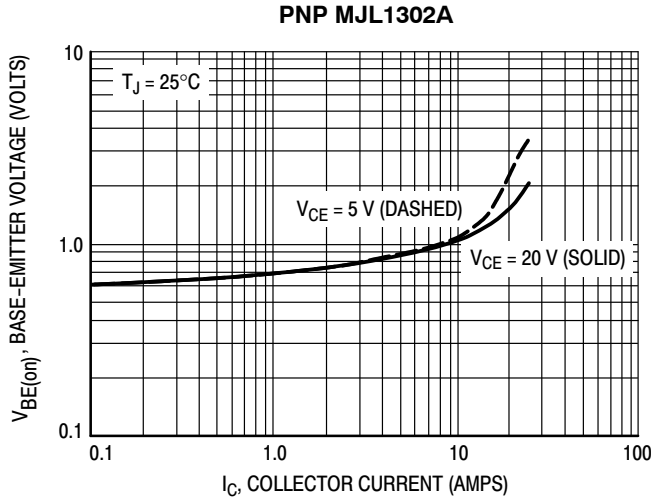


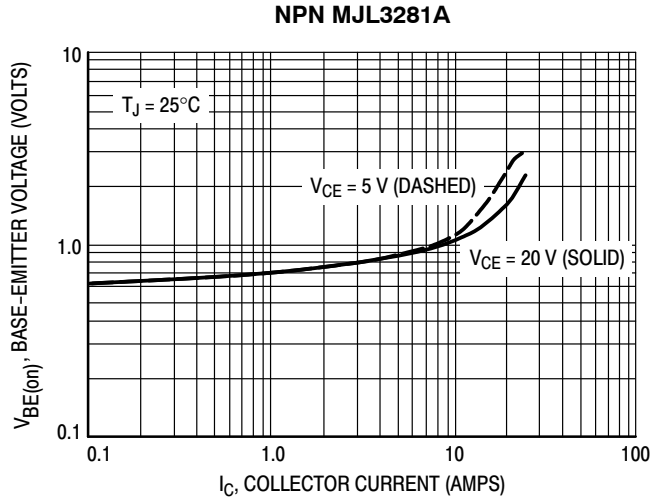
Figure 6. Typical Saturation Voltages

# MJL3281A (NPN) MJL1302A (PNP)

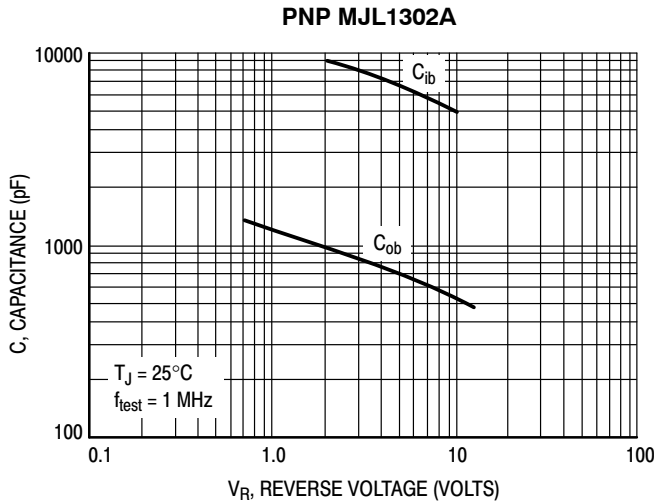
## TYPICAL CHARACTERISTICS



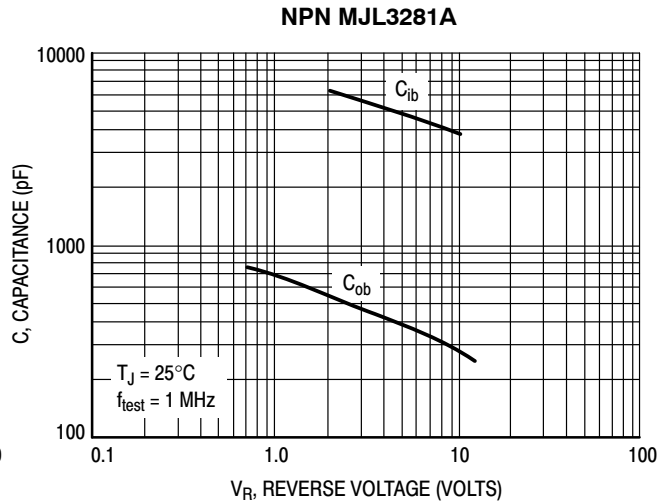
**Figure 7. Typical Base-Emitter Voltage**



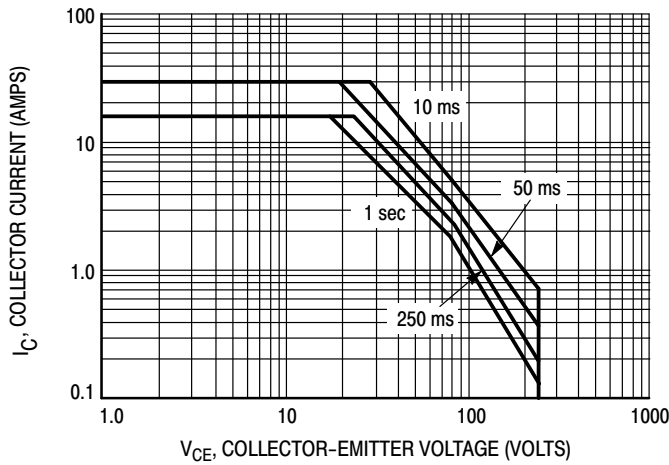
**Figure 8. Typical Base-Emitter Voltage**



**Figure 9. MJL1302A Typical Capacitance**



**Figure 10. MJL3281A Typical Capacitance**



**Figure 11. Active Region Safe Operating Area**

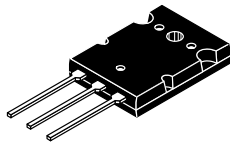
There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

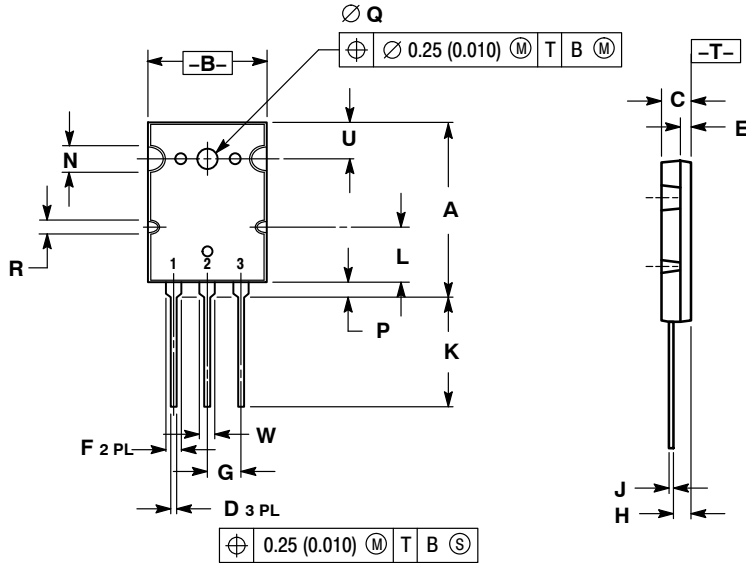
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TO-3BPL (TO-264)  
CASE 340G-02  
ISSUE J

DATE 17 DEC 2004

SCALE 1:2

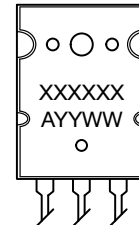


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.2 REF		0.411 REF	
N	4.35 REF		0.172 REF	
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.25 REF		0.089 REF	
U	6.3 REF		0.248 REF	
W	2.8	3.2	0.110	0.125

### GENERIC MARKING DIAGRAM\*

- |  |   |  |  |   |
|--|---|--|--|---|
| STYLE 1:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE | STYLE 2:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER | STYLE 3:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN | STYLE 4:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE | STYLE 5:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER |
|--|---|--|--|---|



- XXXXXX = Specific Device Code
- A = Location Code
- YY = Year
- WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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