

Octal D-Type Latch / 3-STATE Octal D-Type Flip-Flop

MM74HCT573/MM74HCT574

General Description

The MM74HCT573 octal D-type latches and MM74HCT574 octal D-type flip-flop advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic and pin-out compatible. The 3-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

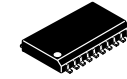
When the MM74HCT573 Latch Enable input is HIGH, the Q outputs will follow the D inputs. When the Latch Enable goes LOW, data at the D inputs will be retained at the outputs until Latch Enable returns HIGH again. When a high logic level is applied to the Output Control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74HCT574 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the Clock (CK) input. When a high logic level is applied to the Output Control (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

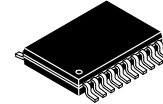
The MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

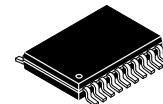
- TTL Input Characteristic Compatible
- Typical Propagation Delay: 17 ns
- Low Input Current: 1 μ A Maximum
- Low Quiescent Current: 160 μ A Maximum
- Compatible with Bus-oriented Systems
- Output Drive Capability: 15 LS-TTL Loads
- These are Pb-Free Devices



SOIC-20 WB
CASE 751D-05

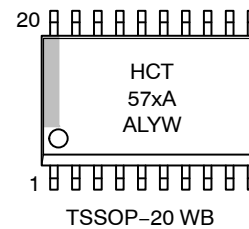
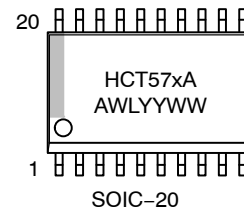


TSSOP20, 4.4x6.5
CASE 948AQ



TSSOP-20 WB
CASE 948E

MARKING DIAGRAMS



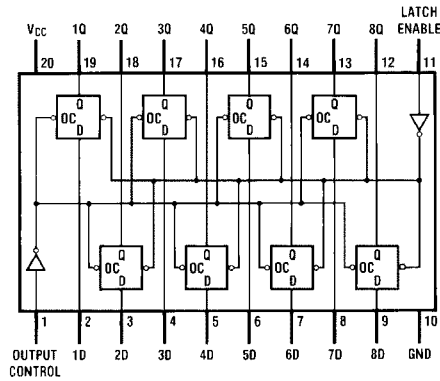
HCT57xA = Specific Device Code
x = 3 or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

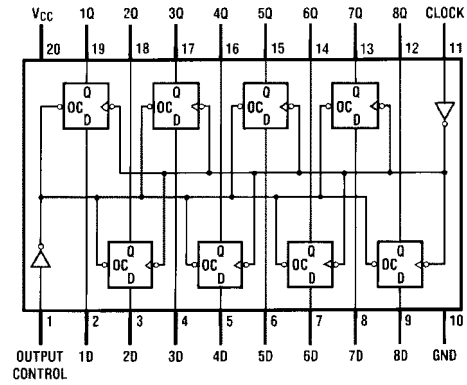
See detailed ordering and shipping information on page 7 of this data sheet.

MM74HCT573/MM74HCT574

Connection Diagrams



MM74HCT573
(Top View)



MM74HCT574
(Top View)

Figure 1. Pin Assignments for SOIC and TSSOP

Truth Tables

MM74HCT573

| Output Control | LE | Data | 373 Output |
|----------------|----|------|----------------|
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

NOTES: H = HIGH Level
 L = LOW Level
 Q₀ = Level of output before steady-state input conditions were established.
 Z = High Impedance State

MM74HCT574

| Output Control | Clock | Data | 374 Output |
|----------------|-------|------|----------------|
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

NOTES: H = HIGH Level
 L = LOW Level
 Q₀ = The level of the output before steady state input conditions were established.
 X = Don't Care
 Z = High Impedance State
 ↑ = Transition from LOW-to-HIGH

MM74HCT573/MM74HCT574

ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | | Rating |
|------------------|---|-------------------|--------------------------|
| V_{CC} | Supply Voltage | | -0.5 to +7.0 V |
| V_{IN} | DC Input Voltage | | -0.5 to $V_{CC} + 0.5$ V |
| V_{OUT} | DC Output Voltage | | -0.5 to $V_{CC} + 0.5$ V |
| I_{IK}, I_{OK} | Clamp Diode Current | | ± 20 mA |
| I_{OUT} | DC Output Current, per Pin | | ± 35 mA |
| I_{CC} | DC V_{CC} or GND Current, per Pin | | ± 70 mA |
| T_{STG} | Storage Temperature Range | | -65°C to +150°C |
| P_D | Power Dissipation | S.O. Package only | 500 mW |
| T_L | Lead Temperature (Soldering 10 Seconds) | | 260°C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|-----------------------------|-----|----------|------|
| V_{CC} | Supply Voltage | 4.5 | 5.5 | V |
| V_{IN}, V_{OUT} | DC Input or Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature Range | -55 | +125 | °C |
| t_r, t_f | Input Rise or Fall Times | | 500 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MM74HCT573/MM74HCT574

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise specified)

| Symbol | Parameter | Conditions | T _A = 25°C | | T _A = -40°C to 85°C | T _A = -55°C to 125°C | Unit |
|-----------------|--|---|-----------------------|-----------------------|-----------------------------------|------------------------------------|------|
| | | | Typ | Guaranteed Limits | | | |
| | | | | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | | - | 2.0 | 2.0 | 2.0 | V |
| V _{IL} | Maximum LOW Level Input Voltage | | - | 0.8 | 0.8 | 0.8 | V |
| V _{OH} | Minimum HIGH Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA | V _{CC} | V _{CC} - 0.1 | V _{CC} - 0.1 | V _{CC} - 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OUT} = 6.0 mA, V _{CC} = 4.5 V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OUT} = 7.2 mA, V _{CC} = 5.5 V | 5.7 | 4.98 | 4.84 | 4.7 | V |
| V _{OL} | Maximum LOW Level Voltage | V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA | 0 | 0.1 | 0.1 | 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OUT} = 6.0 mA, V _{CC} = 4.5 V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OUT} = 7.2 mA, V _{CC} = 5.5 V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| I _{IN} | Maximum Input Current | V _{IN} = V _{CC} or GND, V _{IH} or V _{IL} | - | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum 3-STATE Output Leakage Current | V _{OUT} = V _{CC} or GND, Enable = V _{IH} or V _{IL} | - | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND, I _{OUT} = 0 μA | - | 8.0 | 80 | 160 | μA |
| | | V _{IN} = 2.4 V or 0.5 V (Note 2) | - | 1.5 | 1.8 | 2.0 | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Measured per pin. All others tied to V_{CC} or ground.

MM74HCT573/MM74HCT574

AC ELECTRICAL CHARACTERISTICS

(MM74HCT573: $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $t_r = t_f = 6\text{ ns}$, unless otherwise specified)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|-----------------------|--|--|-----|------------------|------|
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Data to Output | $C_L = 45\text{ pF}$ | 17 | 27 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Latch Enable to Output | $C_L = 45\text{ pF}$ | 16 | 27 | ns |
| t_{PZH} , t_{PZL} | Maximum Enable Propagation Delay Control to Output | $C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 21 | 30 | ns |
| t_{PHZ} , t_{PLZ} | Maximum Disable Propagation Delay Control to Output | $C_L = 5\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 14 | 23 | ns |
| t_W | Minimum Clock Pulse Width | | – | 15 | ns |
| t_S | Minimum Setup Time Data to Clock | | – | 5 | ns |
| t_H | Minimum Hold Time Clock to Data | | – | 12 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(MM74HCT573: $V_{CC} = 5.0\text{ V} \pm 10\%$, $t_r = t_f = 6\text{ ns}$, unless otherwise specified)

| Symbol | Parameter | Conditions | $T_A = 25^\circ\text{C}$ | | $T_A = -40^\circ\text{C}$ to 85°C | $T_A = -55^\circ\text{C}$ to 125°C | Unit |
|-----------------------|--|--|--------------------------|-------------------|--|---|------|
| | | | Typ | Guaranteed Limits | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Data to Output | $C_L = 50\text{ pF}$ | 18 | 30 | 38 | 45 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Latch Enable to Output | $C_L = 50\text{ pF}$ | 17 | 30 | 44 | 53 | ns |
| t_{PZH} , t_{PZL} | Maximum Enable Propagation Delay Control to Output | $C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 22 | 30 | 38 | 45 | ns |
| t_{PHZ} , t_{PLZ} | Maximum Disable Propagation Delay Control to Output | $C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 15 | 30 | 38 | 45 | ns |
| t_{THL} , t_{TLH} | Maximum Output Rise and Fall Time | $C_L = 50\text{ pF}$ | 6 | 12 | 15 | 18 | ns |
| t_W | Minimum Clock Pulse Width | | – | 15 | 20 | 24 | ns |
| t_S | Minimum Setup Time Data to Clock | | 3 | 5 | 6 | 8 | ns |
| t_H | Minimum Hold Time Clock to Data | | 4 | 12 | 15 | 18 | ns |
| C_{IN} | Maximum Input Capacitance | | – | 10 | 10 | 10 | pF |
| C_{OUT} | Maximum Output Capacitance | | – | 20 | 20 | 20 | pF |
| C_{PD} | Power Dissipation Capacitance (Note 3) | $OC = V_{CC}$ | – | 5 | – | – | pF |
| | | $OC = GND$ | – | 52 | – | – | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC}^2 f + I_{CC}$.

MM74HCT573/MM74HCT574

AC ELECTRICAL CHARACTERISTICS

(MM74HCT574: $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $t_r = t_f = 6\text{ ns}$)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|-----------------------|---|--|-----|------------------|------|
| f_{MAX} | Maximum Clock Frequency | | 60 | 33 | MHz |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay to Output | $C_L = 45\text{ pF}$ | 17 | 27 | ns |
| t_{PZH} , t_{PZL} | Maximum Enable Propagation Delay Control to Output | $C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 19 | 28 | ns |
| t_{PHZ} , t_{PLZ} | Maximum Disable Propagation Delay Control to Output | $C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 14 | 25 | ns |
| t_W | Minimum Clock Pulse Width | | - | 15 | ns |
| t_S | Minimum Setup Time Data to Clock | | - | 12 | ns |
| t_H | Minimum Hold Time Clock to Data | | - | 5 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(MM74HCT574: $V_{CC} = 5.0\text{ V} \pm 10\%$, $t_r = t_f = 6\text{ ns}$, unless otherwise specified)

| Symbol | Parameter | Conditions | $T_A = 25^\circ\text{C}$ | | $T_A = -40^\circ\text{C}$ to 85°C | $T_A = -55^\circ\text{C}$ to 125°C | Unit |
|-----------------------|---|--|--------------------------|-------------------|--|---|------|
| | | | Typ | Guaranteed Limits | | | |
| f_{MAX} | Maximum Clock Frequency | | - | 33 | 28 | 23 | MHz |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay Clock to Output | $C_L = 50\text{ pF}$ | 18 | 30 | 38 | 45 | ns |
| t_{PZH} , t_{PZL} | Maximum Enable Propagation Delay Control to Output | $C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 22 | 30 | 38 | 45 | ns |
| t_{PHZ} , t_{PLZ} | Maximum Disable Propagation Delay Control to Output | $C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$ | 15 | 30 | 38 | 45 | ns |
| t_{THL} , t_{TLH} | Maximum Output Rise and Fall Time | $C_L = 50\text{ pF}$ | 6 | 12 | 15 | 18 | ns |
| t_W | Minimum Clock Pulse Width | | - | 15 | 20 | 24 | ns |
| t_S | Minimum Setup Time Data to Clock | | 6 | 12 | 15 | 18 | ns |
| t_H | Minimum Hold Time Clock to Data | | 1 | 5 | 6 | 8 | ns |
| C_{IN} | Maximum Input Capacitance | | - | 10 | 10 | 10 | pF |
| C_{OUT} | Maximum Output Capacitance | | - | 20 | 20 | 20 | pF |
| C_{PD} | Power Dissipation Capacitance (Note 4) | $OC = V_{CC}$ | 5 | - | - | - | pF |
| | | $OC = GND$ | 58 | - | - | - | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC}^2 f + I_{CC}$.

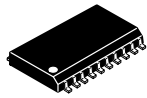
MM74HCT573/MM74HCT574

ORDERING INFORMATION

| Part Number | Package | Shipping† |
|----------------|---|--------------------------|
| MM74HCT573WMX | SOIC-20 WB, Case 751D-05 (Pb-Free and Halide-Free) | 1000 Units / Tape & Reel |
| MM74HCT573MTC | TSSOP-20 WB, Case 948E (Pb-Free) | 75 Units / Tube |
| MM74HCT573MTCX | | 2500 Units / Tape & Reel |
| MM74HCT574WM | SOIC-20 WB, Case 751D-05 (Pb-Free and Halide-Free) | 38 Units / Tube |
| MM74HCT574WMX | | 1000 Units / Tape & Reel |
| MM74HCT574MTC | TSSOP-20 WB, Case 948E (Pb-Free) | 75 Units / Tube |
| MM74HCT574MTCX | TSSOP20, Case 948AQ-01 (Pb-Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

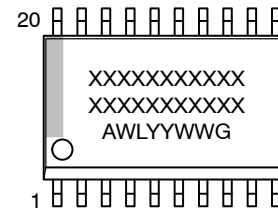
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | TSSOP-20 WB | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

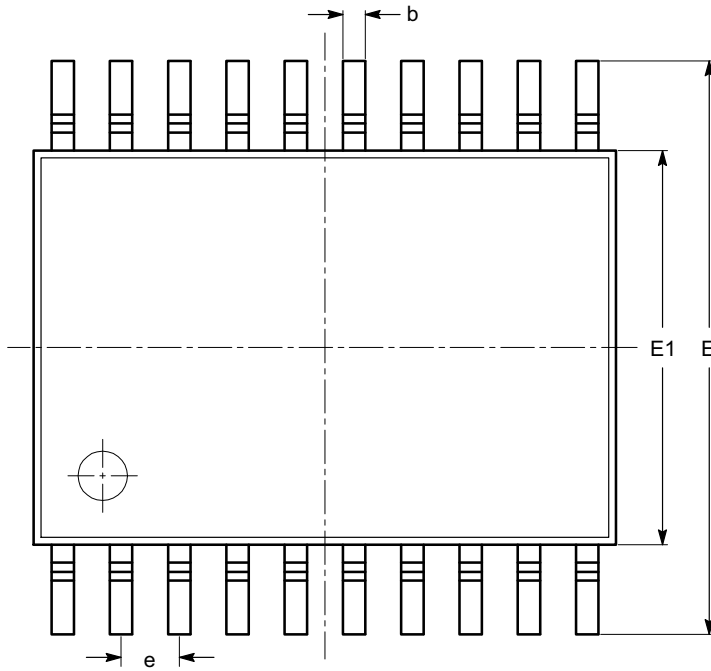
PACKAGE DIMENSIONS

ON Semiconductor®



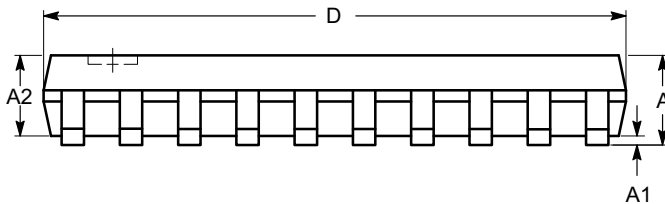
TSSOP20, 4.4x6.5
CASE 948AQ-01
ISSUE A

DATE 19 MAR 2009

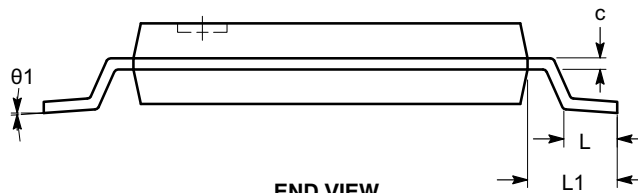


| SYMBOL | MIN | NOM | MAX |
|----------|----------|------|------|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| θ | 0° | | 8° |

TOP VIEW



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

| | | |
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| DESCRIPTION: | TSSOP20, 4.4X6.5 | PAGE 1 OF 1 |

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