

# MOSFET - Power, Single N-Channel, D<sup>2</sup>PAK7

## 150 V, 7 mΩ, 121 A

### NTBGS6D5N15MC

#### Features

- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

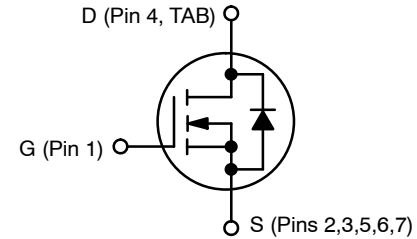
#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	150	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	121	A
			P <sub>D</sub>	238	W
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	15	A
			P <sub>D</sub>	3.7	W
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	1800	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	198	A
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L</sub> = 60 A <sub>pk</sub> , L = 0.1 mH)			E <sub>AS</sub>	180	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

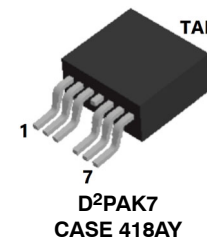
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>	I <sub>D MAX</sub>
150 V	7 mΩ @ 10 V	121 A
	8.7 mΩ @ 8 V	



N-CHANNEL MOSFET



#### MARKING DIAGRAM

AYWWZZ
NTBG
S6D5N15
°

NTBGS6D5N15 = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Number

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTBGS6D5N15MC	D <sup>2</sup> PAK7 (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTBGS6D5N15MC

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.6	°C/W
Junction-to-Ambient – Steady State (Note 1, 2)	$R_{\theta JA}$	40	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		59.62		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 379\ \mu\text{A}$	2.5	3.5	4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-9.53		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 69\text{ A}$		5.5	7	m $\Omega$
		$V_{GS} = 8\text{ V}, I_D = 34\text{ A}$		5.9	8.7	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 60.5\text{ A}$		88		S
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		1.1		$\Omega$

### CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}, f = 1\text{ MHz}$		4745		pF
Output Capacitance	$C_{OSS}$			1370		
Reverse Transfer Capacitance	$C_{RSS}$			10.3		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 69\text{ A}$		57		nC
Threshold Gate Charge	$Q_{G(TH)}$			16		
Gate-to-Source Charge	$Q_{GS}$			27		
Gate-to-Drain Charge	$Q_{GD}$			7		
Output Charge	$Q_{OSS}$		$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}$		171	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 69\text{ A}, R_G = 6\ \Omega$		34		ns
Rise Time	$t_r$			75		
Turn-Off Delay Time	$t_{d(OFF)}$			39		
Fall Time	$t_f$			6		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 69\text{ A}$	$T_J = 25^\circ\text{C}$		0.92	1.2	V
			$T_J = 125^\circ\text{C}$		0.82		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 69\text{ A}$		74		ns	
Charge Time	$t_a$			53			
Discharge Time	$t_b$			22			
Reverse Recovery Charge	$Q_{RR}$			141			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

# NTBGS6D5N15MC

## TYPICAL CHARACTERISTICS

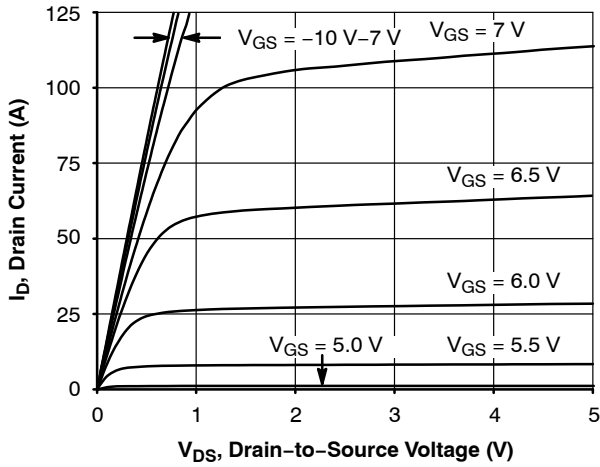


Figure 1. On-Region Characteristics

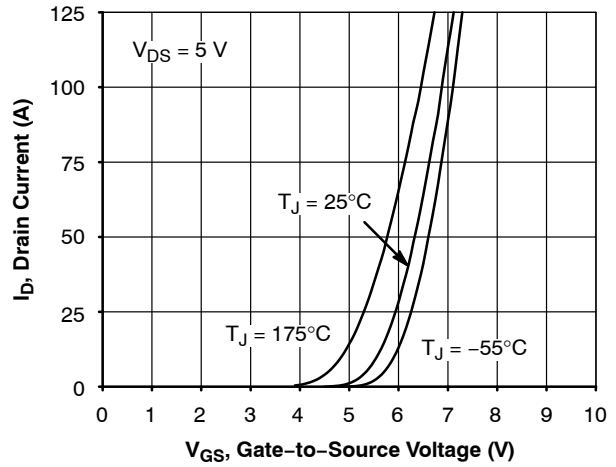


Figure 2. Transfer Characteristics

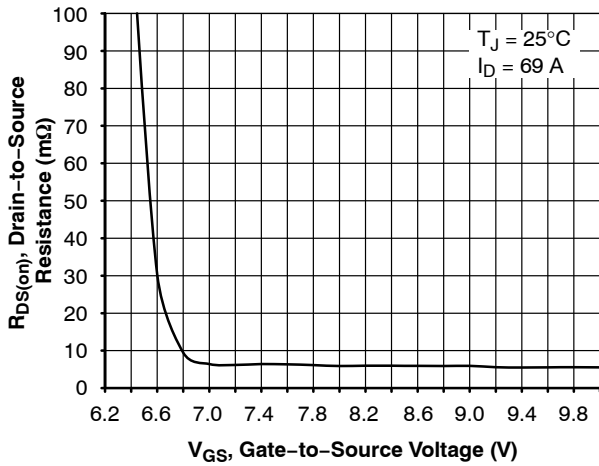


Figure 3. On-Resistance vs. Gate-to-Source Voltage

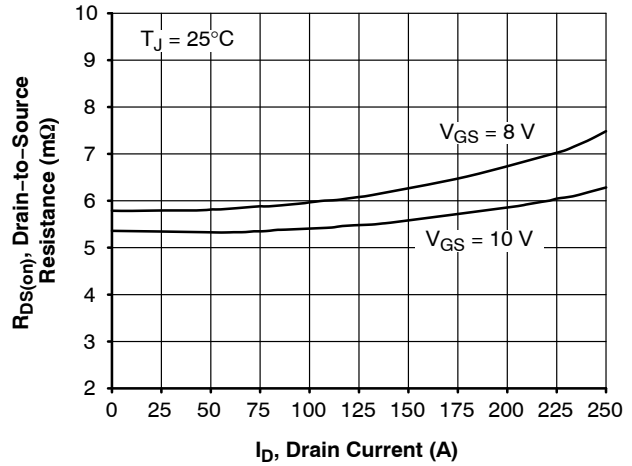


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

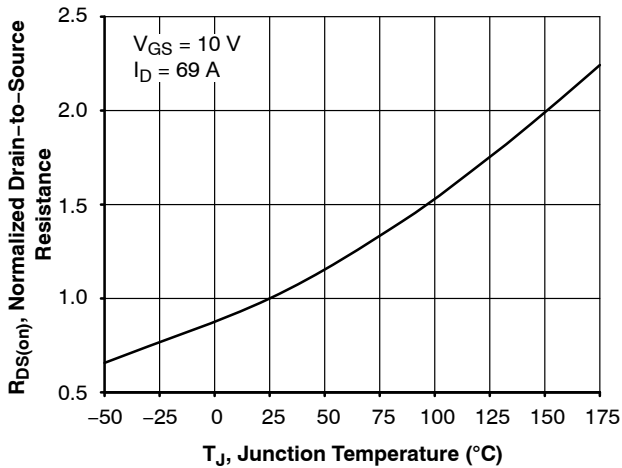


Figure 5. On-Resistance Variation vs. Temperature

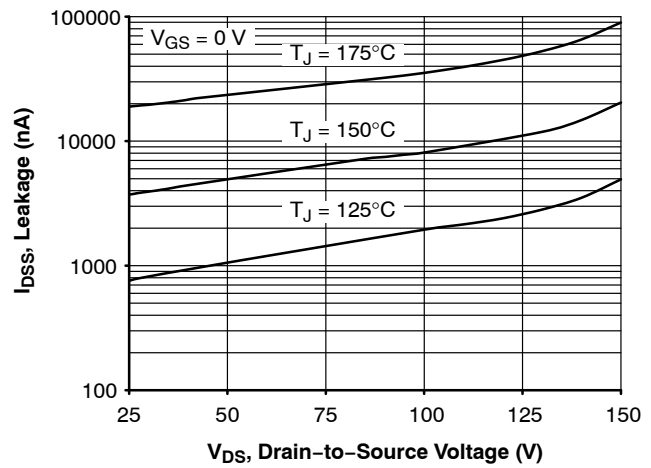


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS (Continued)

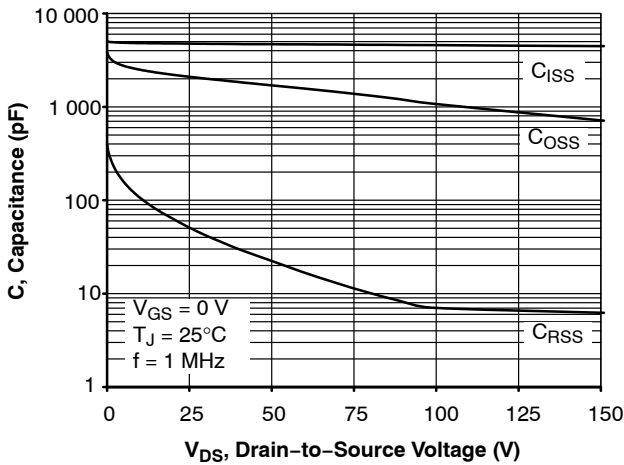


Figure 7. Capacitance Variation

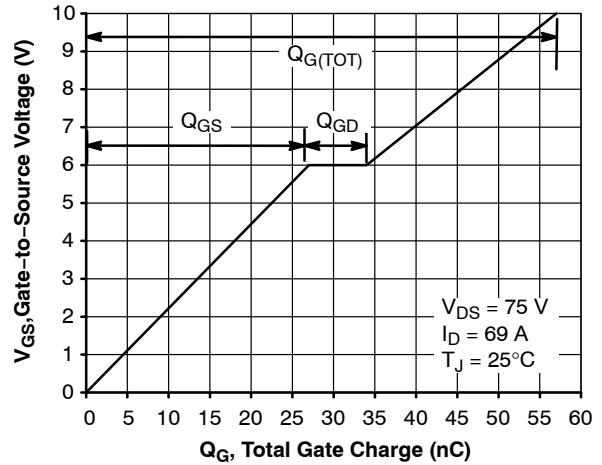


Figure 8. Gate-to-Source vs. Total Charge

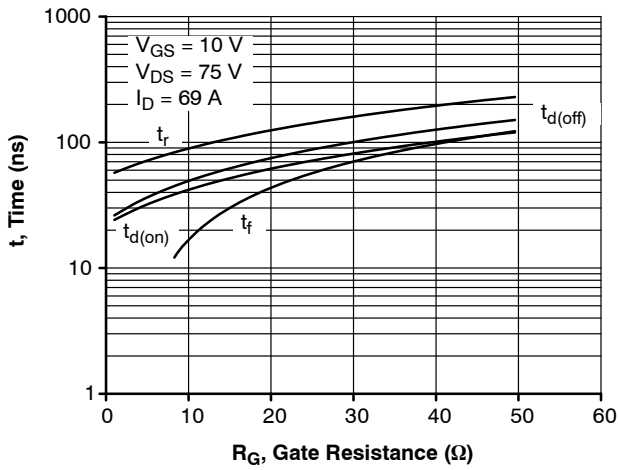


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

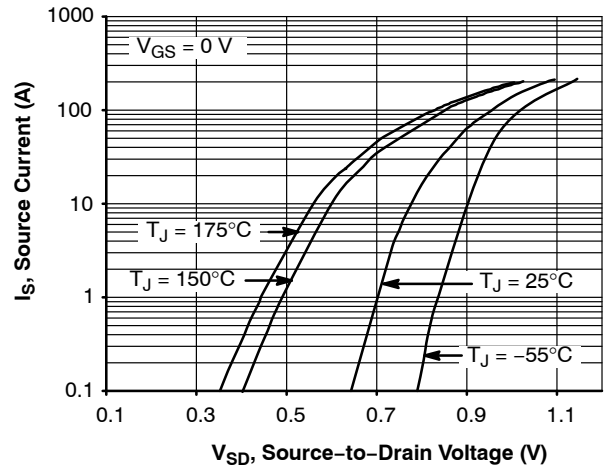


Figure 10. Diode Forward Voltage vs. Current

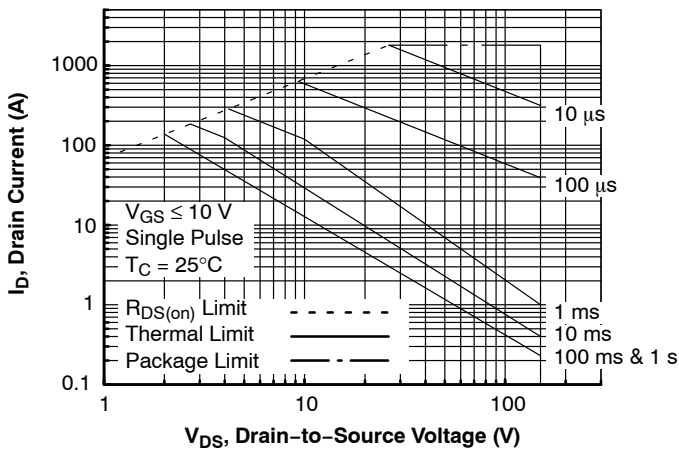


Figure 11. Maximum Rated Forward Biased Safe Operating Area

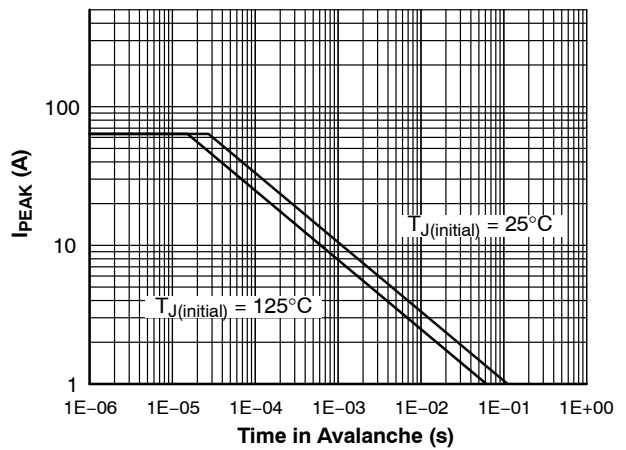


Figure 12. Maximum Drain Current vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS (Continued)

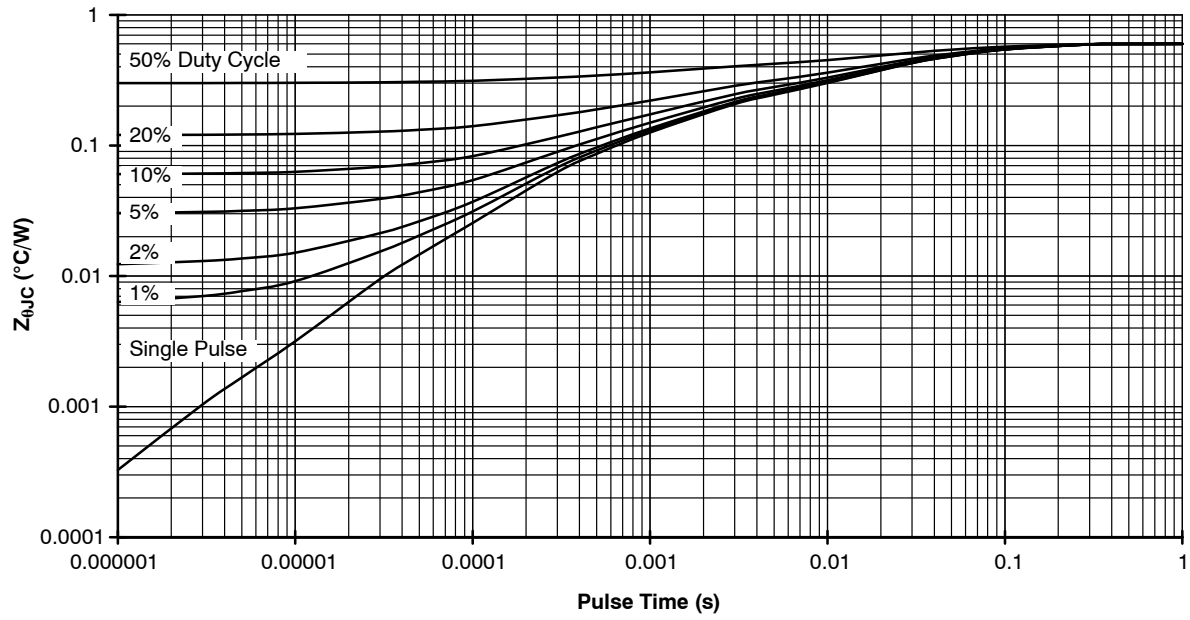


Figure 13. Thermal Response

# MECHANICAL CASE OUTLINE

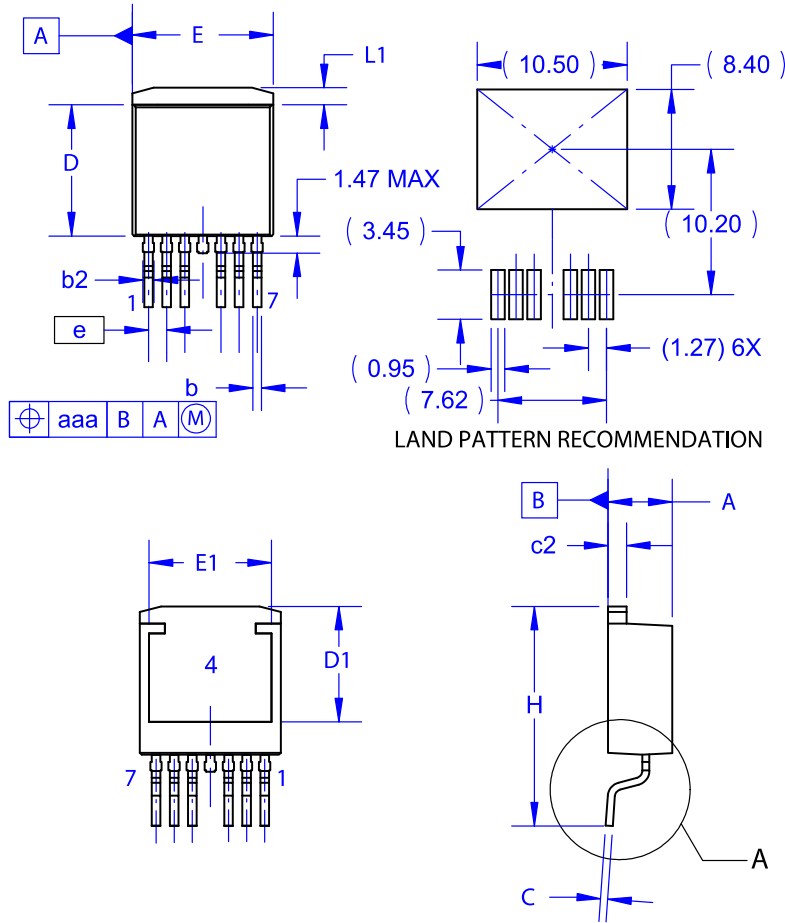
## PACKAGE DIMENSIONS

ON Semiconductor®



### D2PAK7 (TO-263 7 LD) CASE 418AY ISSUE C

DATE 15 JUL 2019

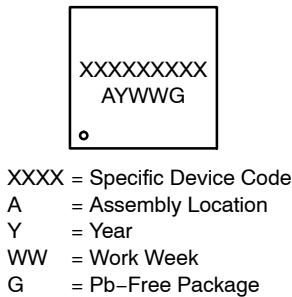


**NOTES:**

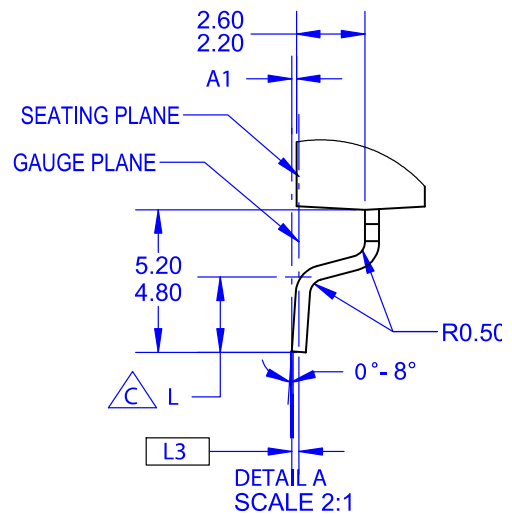
- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- F. LAND PATTERN RECOMMENDATION PER IPC-TO127P1524X465-8N.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.70	0.80	0.90
b	0.50	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	7.70	~	~
E	9.70	9.90	10.20
E1	8.38	8.58	8.78
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

**GENERIC MARKING DIAGRAM\***



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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