

NVMYS7D3N04CL

MOSFET – Power, Single N-Channel

40 V, 7.3 mΩ, 52 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- LFPK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DS} | 40 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 52 | A |
| | | $T_C = 100^\circ\text{C}$ | 29 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3) | Steady State | $T_C = 25^\circ\text{C}$ | P_D 38 | W |
| | | $T_C = 100^\circ\text{C}$ | 12 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 17 | A |
| | | $T_A = 100^\circ\text{C}$ | 12 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 3.8 | W |
| | | $T_A = 100^\circ\text{C}$ | 1.9 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 269 | A | |
| Operating Junction and Storage Temperature | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 31 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 2.9 \text{ A}$) | E_{AS} | 65 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|--------------------|
| Junction-to-Case – Steady State (Note 3) | $R_{\theta JC}$ | 4.0 | $^\circ\text{C/W}$ |
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 39 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

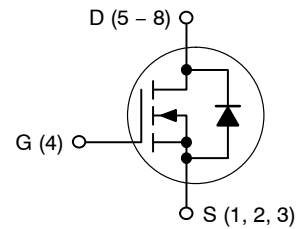


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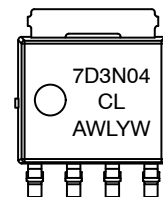
| $V_{(BR)DSS}$ | $R_{DS(on) MAX}$ | $I_D MAX$ |
|---------------|------------------|-----------|
| 40 V | 7.3 mΩ @ 10 V | 52 A |
| | 12 mΩ @ 4.5 V | |

N-Channel



LFPK4
CASE 760AB

MARKING DIAGRAM



7D3N04CL = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMYS7D3N04CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|--------------------------------------|--|------------------------|----|-----|-------|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 40 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 25 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 40 V | T _J = 25°C | | 10 | μA |
| | | | T _J = 125°C | | 250 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|-------------------------------|---------------------|--|-----|-----|-----|----|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 30 μA | 1.2 | | 2.0 | V |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 10 A | | 6.1 | 7.3 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 10 A | | 9.7 | 12 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 10 A | | 33 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|--|---|-----|----|----|
| Input Capacitance | C _{iss} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V | | 860 | | pF |
| Output Capacitance | C _{oss} | | | 360 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 15 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 32 V, I _D = 10 A | | 7.0 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | V _{GS} = 10 V, V _{DS} = 32 V, I _D = 10 A | | 1.8 | | nC |
| Gate-to-Source Charge | Q _{GS} | | | 3.3 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 2.5 | | |
| Total Gate Charge | Q _{G(TOT)} | | V _{GS} = 10 V, V _{DS} = 32 V, I _D = 10 A | | 16 | |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|---------------------|---------------------|---|--|-----|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 10 V, V _{DS} = 32 V, I _D = 10 A, R _G = 1 Ω | | 8.0 | | ns |
| Rise Time | t _r | | | 24 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 29 | | |
| Fall Time | t _f | | | 6.0 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|-----------------|--|------------------------|----|------|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 10 A | T _J = 25°C | | 0.84 | 1.2 | V |
| | | | T _J = 125°C | | 0.71 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 10 A | | 24 | | ns | |
| Charge Time | t _a | | | 11 | | | |
| Discharge Time | t _b | | | 12 | | | |
| Reverse Recovery Charge | Q _{RR} | | | 11 | | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

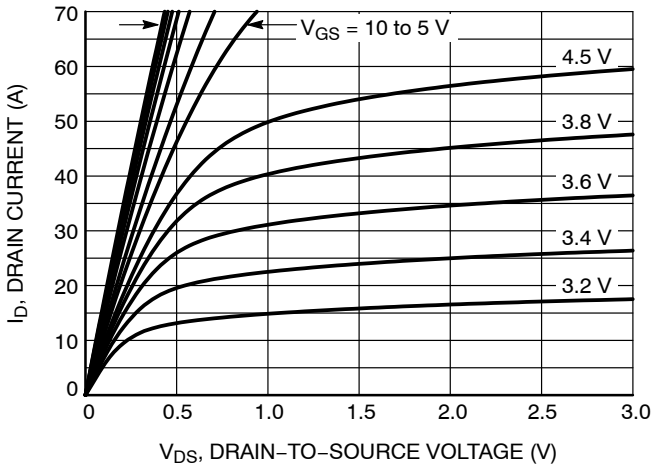


Figure 1. On-Region Characteristics

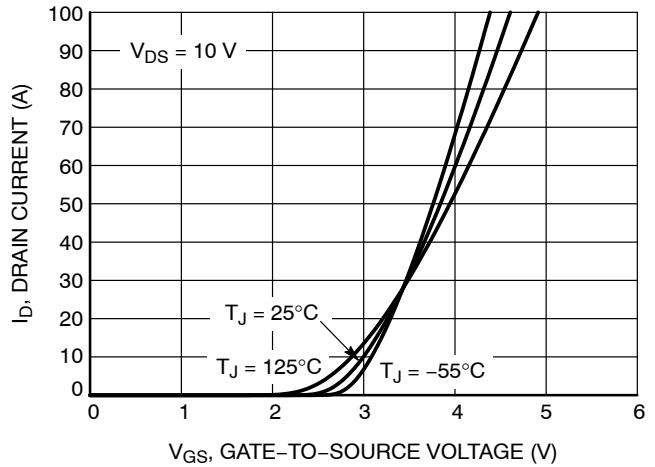


Figure 2. Transfer Characteristics

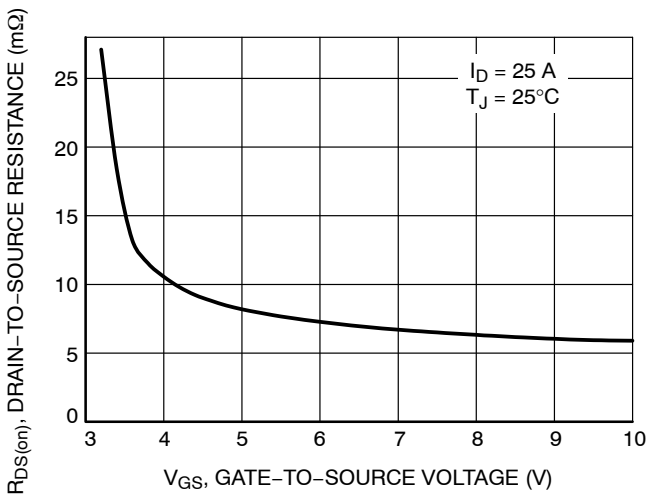


Figure 3. On-Resistance vs. Gate-to-Source Voltage

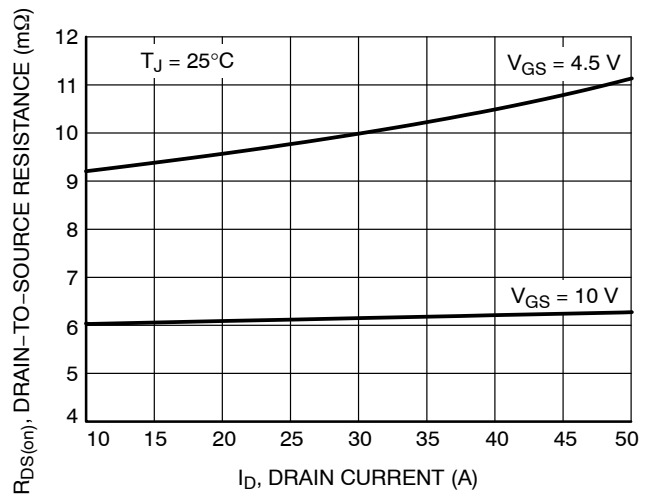


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

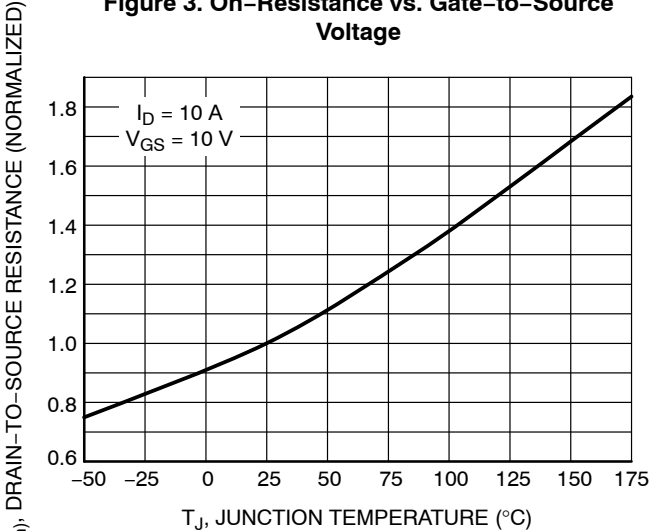


Figure 5. On-Resistance Variation with Temperature

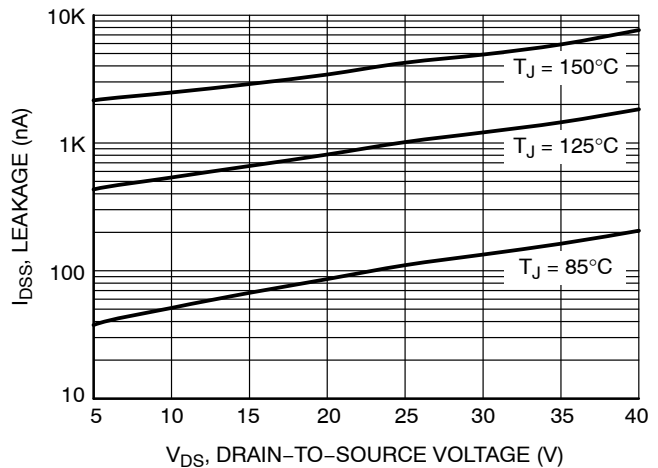


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

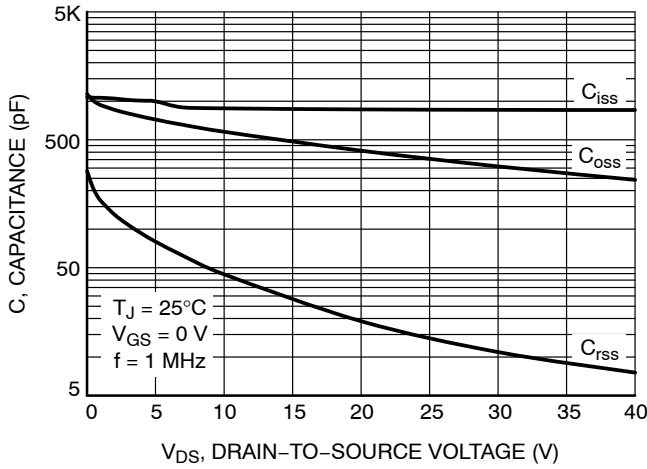


Figure 7. Capacitance Variation

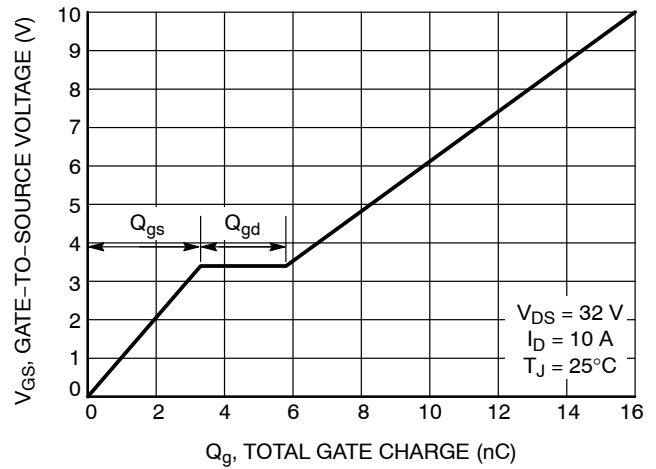


Figure 8. Gate-to-Source vs. Total Charge

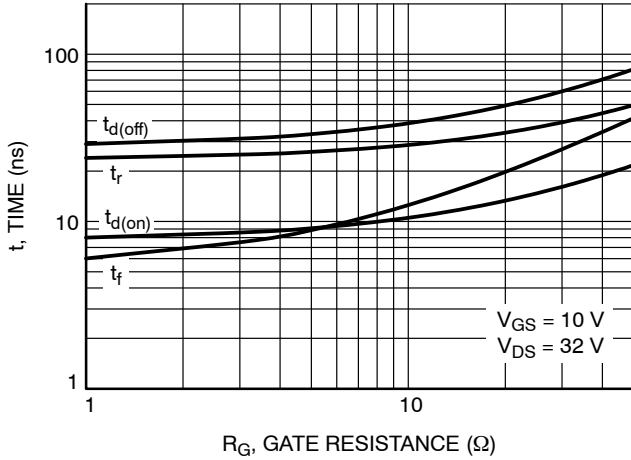


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

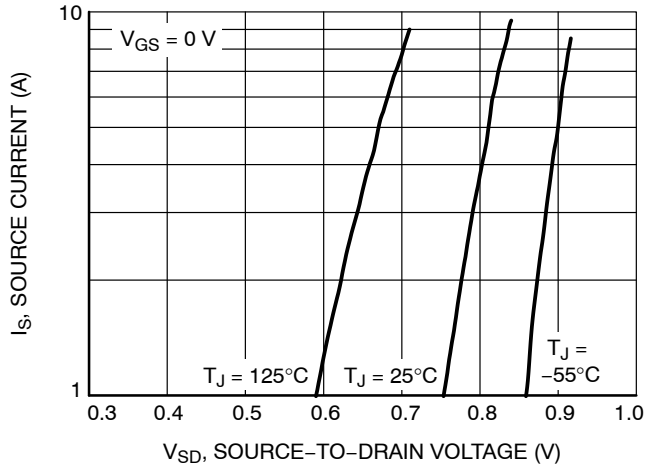


Figure 10. Diode Forward Voltage vs. Current

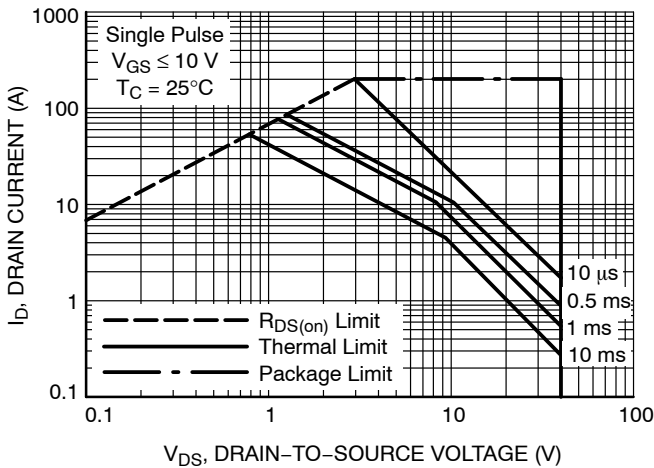


Figure 11. Maximum Rated Forward Biased Safe Operating Area

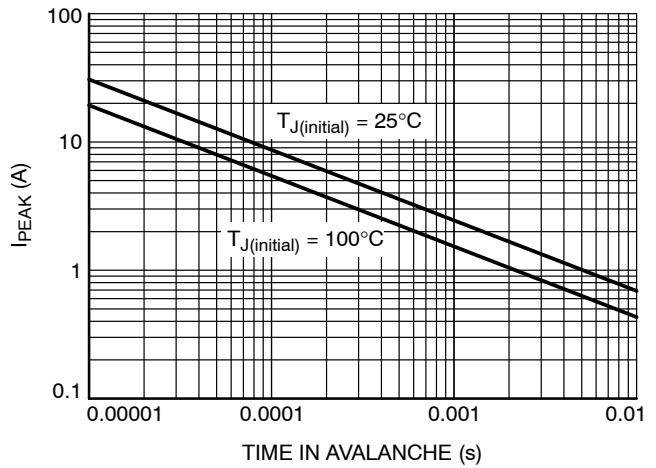


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

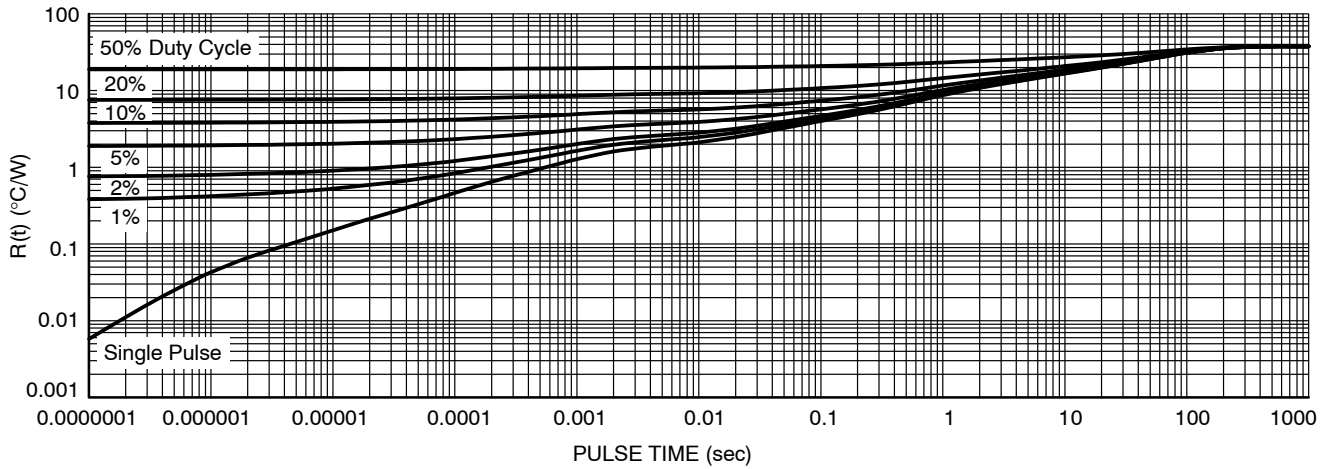


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|------------------|----------|---------------------|-----------------------|
| NVMYS7D3N04CLTWG | 7D3N04CL | LFPAK4 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

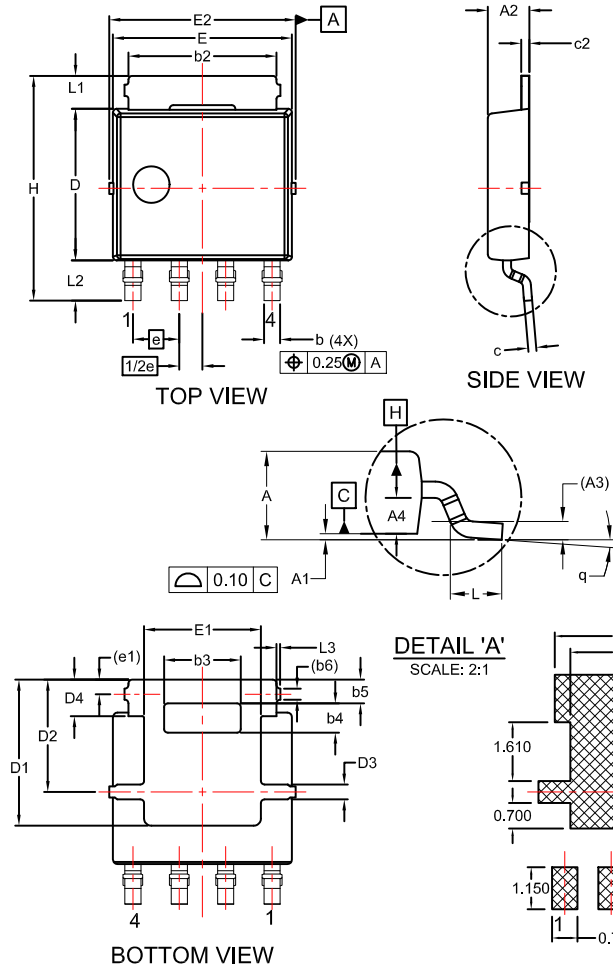
PACKAGE DIMENSIONS

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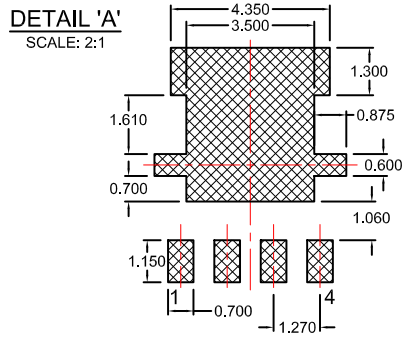
LFPAK4 5x6 CASE 760AB ISSUE C

DATE 19 NOV 2019



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
 4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

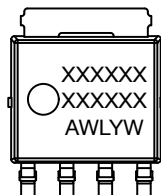
| UNIT IN MILLIMETER | | | |
|--------------------|-----------|------|------|
| DIM | MIN | NOM | MAX |
| A | 1.10 | 1.20 | 1.30 |
| A1 | 0.00 | 0.08 | 0.15 |
| A2 | 1.10 | 1.15 | 1.20 |
| A3 | 0.25 REF | | |
| A4 | 0.45 | 0.50 | 0.55 |
| b | 0.40 | 0.45 | 0.50 |
| b2 | 3.80 | 4.10 | 4.40 |
| b3 | 2.00 | 2.10 | 2.20 |
| b4 | 0.70 | 0.80 | 0.90 |
| b5 | 0.55 | 0.65 | 0.75 |
| b6 | 0.31 REF | | |
| c | 0.19 | 0.22 | 0.25 |
| c2 | 0.19 | 0.22 | 0.25 |
| D | 4.05 | 4.15 | 4.25 |
| D1 | 3.80 | 4.00 | 4.20 |
| D2 | 3.00 | 3.10 | 3.20 |
| D3 | 0.30 | 0.40 | 0.50 |
| D4 | 0.90 | 1.00 | 1.10 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 3.10 | 3.20 | 3.30 |
| E2 | 5.00 | 5.15 | 5.30 |
| e | 1.27 BSC | | |
| 1/2e | 0.635 BSC | | |
| e1 | 0.40 REF | | |
| H | 6.00 | 6.15 | 6.30 |
| L | 0.40 | 0.65 | 0.85 |
| L1 | 0.80 | 0.90 | 1.00 |
| L2 | 0.90 | 1.10 | 1.30 |
| L3 | 0.00 | 0.10 | 0.20 |
| q | 0° | 4° | 8° |



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

| | | |
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| DESCRIPTION: | LFPAK4 5x6 | PAGE 1 OF 1 |

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